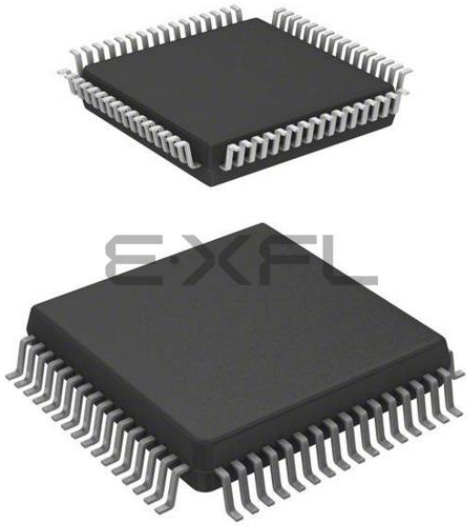

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8/300L
Core Size	8-Bit
Speed	10MHz
Connectivity	SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38104hv

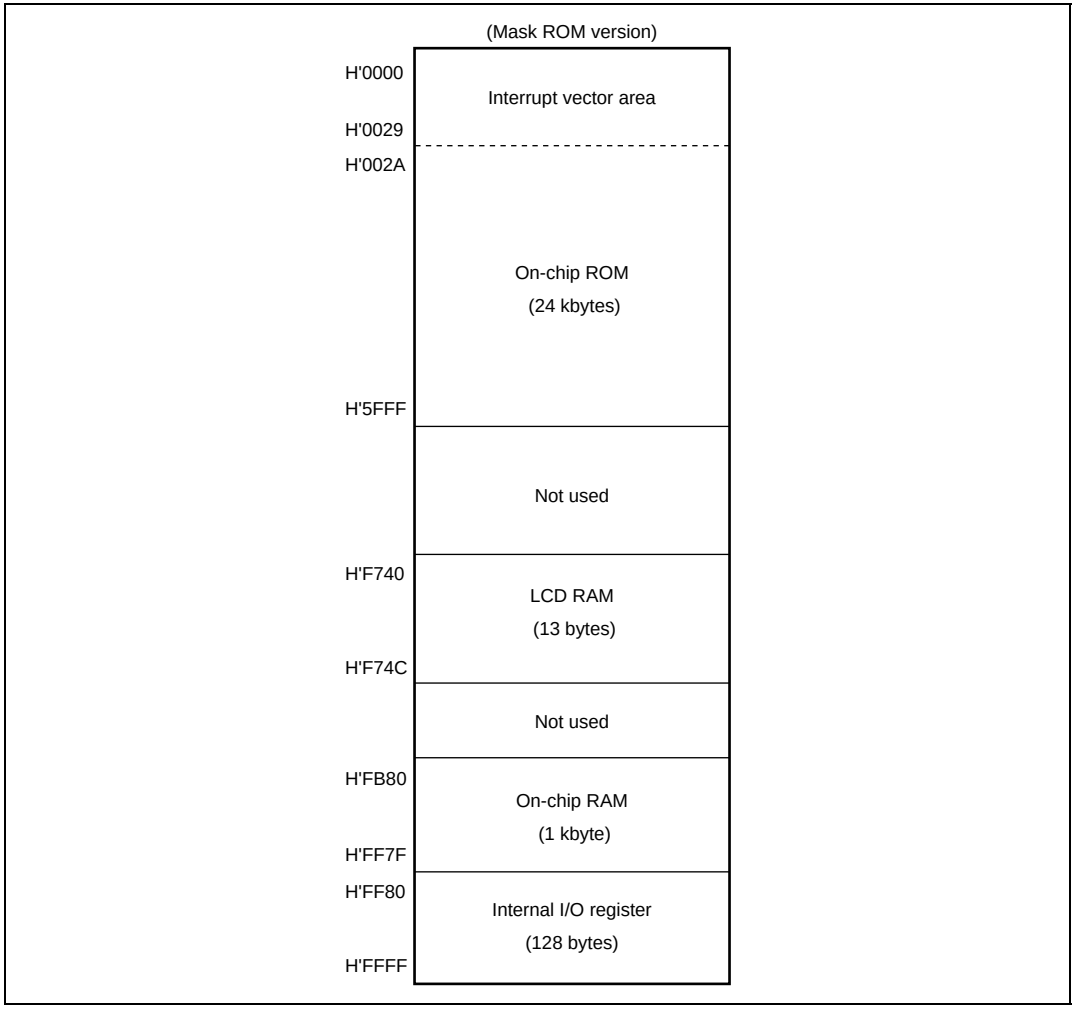
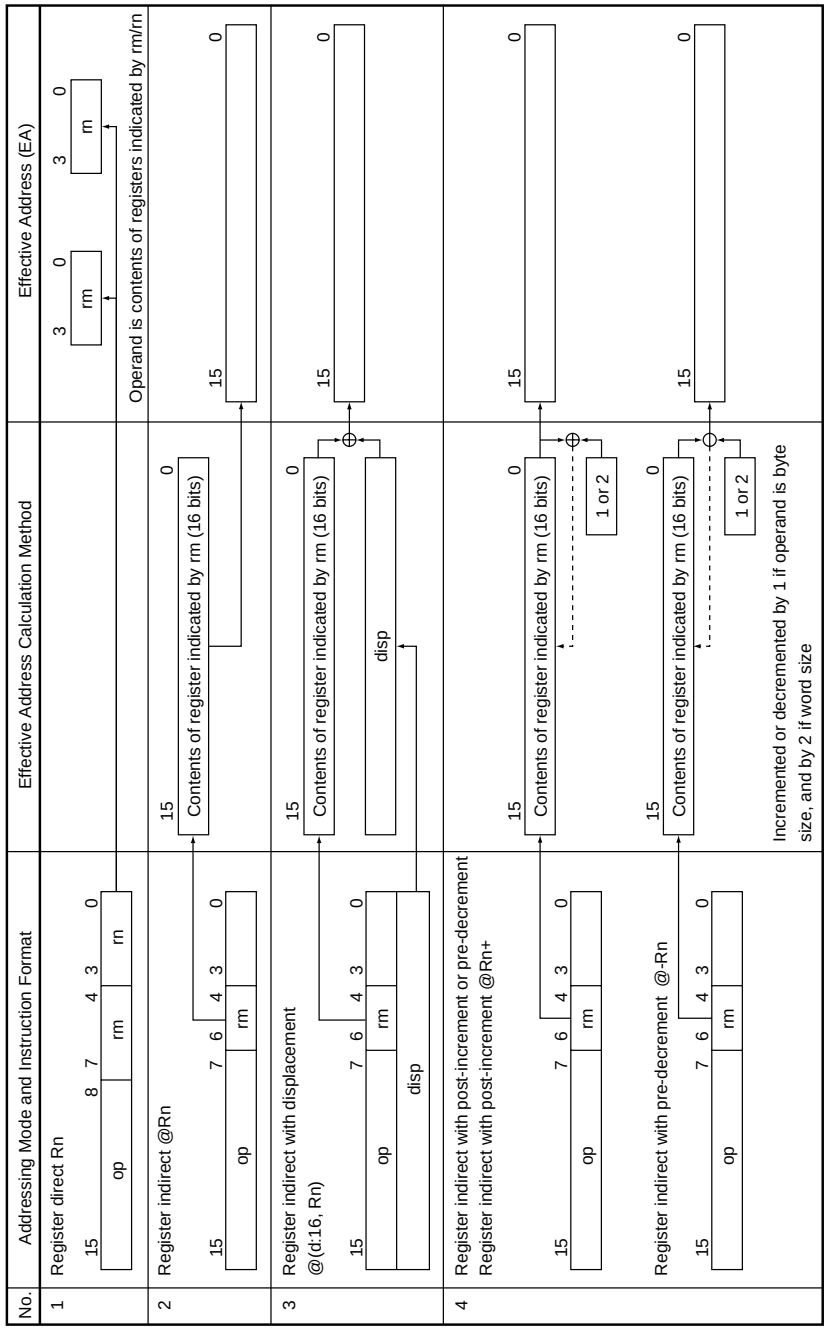
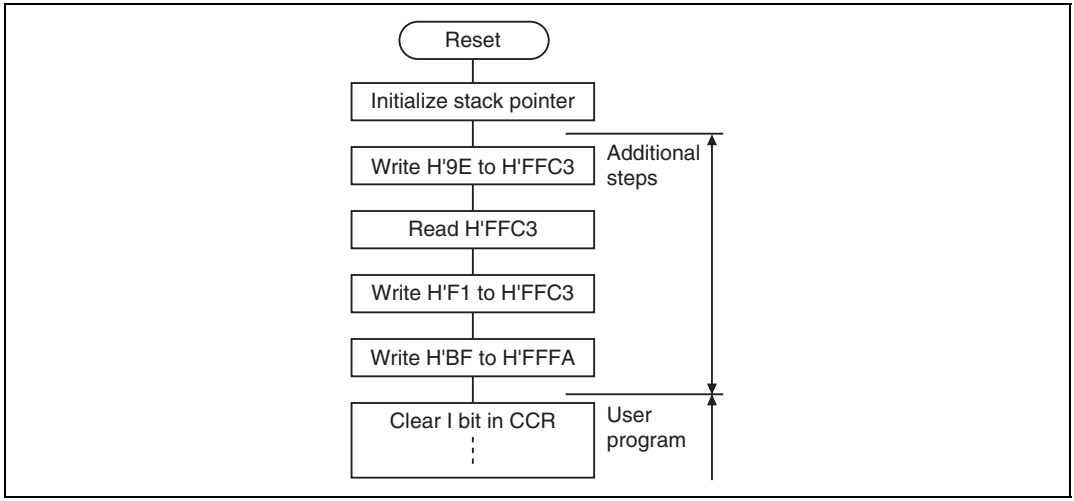


Figure 2.1(5) H8/38003, H8/38103 Memory Map

Table 2.12 Effective Address Calculation



No.	Addressing Mode and Instruction Format	Effective Address Calculation Method	Effective Address (EA)
5	Absolute address @aa:8 15 8 7 0 op abs @aa:16 15 0 op abs		15 8 7 0 H'FF 15 0
6	Immediate #xx:8 15 8 7 0 op IMM #xx:16 15 0 op IMM		Operand is 1- or 2-byte immediate data
7	Program-counter relative@ (d: 8, PC) 15 8 7 0 op disp	15 0 PC contents Sign extension disp	15 0


Reset
Initialize stack pointer
Write H'9E to H'FFC3
Read H'FFC3
Write H'F1 to H'FFC3
Write H'BF to H'FFFA
Clear I bit in CCR
Additional steps
User program

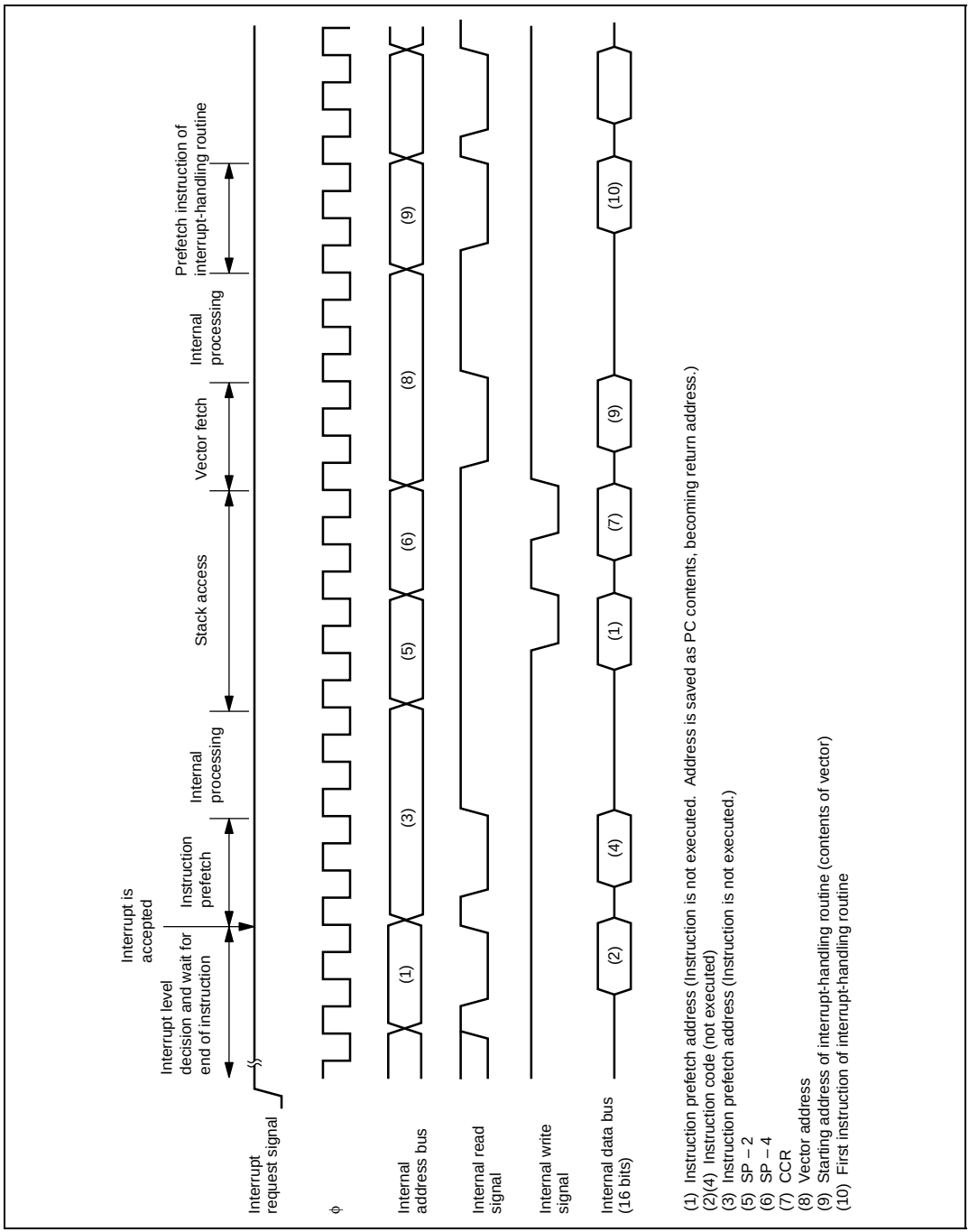
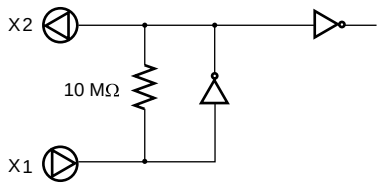


Figure 3.3 Interrupt Sequence

4.4 Subclock Generator

Figure 4.8 shows a block diagram of the subclock generator. Note that on the H8/38104 Group the subclock oscillator can be disabled by programs by setting the SUBSTP bit in the OSCCR register. The register setting to disable the subclock oscillator should be made in the active mode. When restoring operation of the subclock oscillator after it has been disabled using the OSCCR register, it is necessary to wait for the oscillation stabilization time (typ = 8s) to elapse before using the subclock.



Note : Resistance is a reference value.

Figure 4.8 Block Diagram of Subclock Generator

8. The maximum number of repetitions of the program/program-verify sequence of the same bit is 1,000.

8.1.6 Pin Functions

The port 3 pin functions are shown below.

- P37/AEVL pin

The pin function depends on the combination of bit AEVL in PMR3 and bit PCR37 in PCR3.

AEVL	0		1
PCR37	0	1	*
Pin Function	P37 input pin	P37 output pin	AEVL input pin

Legend: *: Don't care.

- P36/AEVH pin

The pin function depends on the combination of bit AEVH in PMR3 and bit PCR36 in PCR3.

AEVH	0		1
PCR36	0	1	*
Pin Function	P36 input pin	P36 output pin	AEVH input pin

Legend: *: Don't care.

- P35 to P33 pins

The pin function depends on the corresponding bit in PCR3.

(n = 5 to 3)

PCR3n	0	1
Pin Function	P3n input pin	P3n output pin

- P32/TMOFH pin

The pin function depends on the combination of bit TMOFH in PMR3 and bit PCR32 in PCR3.

TMOFH	0		1
PCR32	0	1	*
Pin Function	P32 input pin	P32 output pin	TMOFH output pin

Legend: *: Don't care.

8.5.2 Port Control Register 7 (PCR7)

PCR7 controls whether each of the port 7 pins functions as an input pin or output pin.

Bit	Bit Name	Initial Value	R/W	Description
7	PCR77	0	W	Setting a PCR7 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR7 and in PDR7 are valid only when the corresponding pin is designated by the SGS3 to SGS0 bits in LPCR as a general I/O pin.
6	PCR76	0	W	
5	PCR75	0	W	
4	PCR74	0	W	
3	PCR73	0	W	PCR7 is a write-only register. Bits 7 to 0 are always read as 1.
2	PCR72	0	W	
1	PCR71	0	W	
0	PCR70	0	W	

8.5.3 Pin Functions

The port 7 pin functions are shown below.

- P77/SEG24 to P74/SEG21 pins

The pin function depends on the combination of bit PCR7n in PCR7 and bits SGS3 to SGS0 in LPCR.

(n = 7 to 4)

SGS3 to SGS0	Other than B'0110, B'0111, B'1000, B'1001, B'1010, B'1011, B'1100, B'1101		B'0110, B'0111, B'1000, B'1001, B'1010, B'1011, B'1100, B'1101
PCR7n	0	1	*
Pin Function	P7n input pin	P7n output pin	SEGn+17 output pin

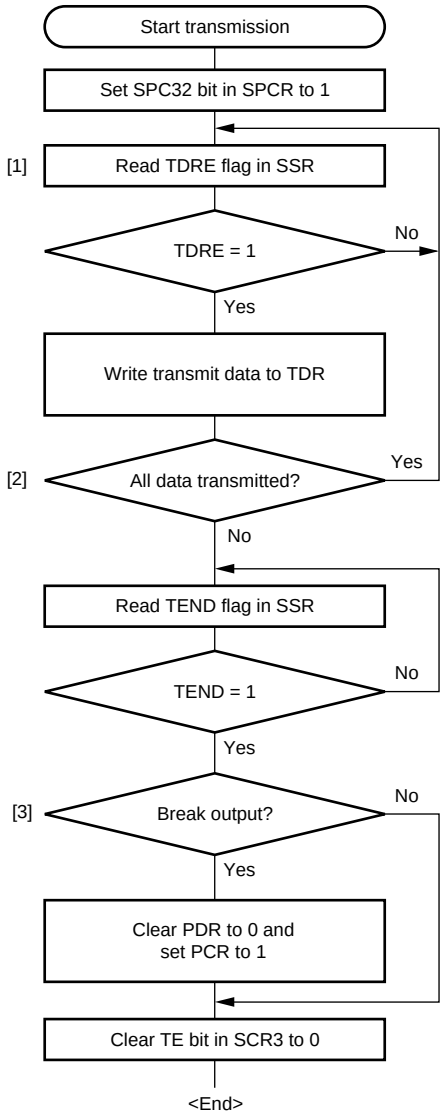
Legend: *: Don't care.

8.10 Usage Notes

8.10.1 How to Handle Unused Pin

If an I/O pin not used by the user system is floating, pull it up or down.

- If an unused pin is an input pin, handle it in one of the following ways:
  - Pull it up to Vcc with an on-chip pull-up MOS.
  - Pull it up to Vcc with an external resistor of approximately 100 kΩ.
  - Pull it down to Vss with an external resistor of approximately 100 kΩ.
  - For a pin also used by the A/D converter, pull it up to AVcc.
- If an unused pin is an output pin, handle it in one of the following ways:
  - Set the output of the unused pin to high and pull it up to Vcc with an on-chip pull-up MOS.
  - Set the output of the unused pin to high and pull it up to Vcc with an external resistor of approximately 100 kΩ.
  - Set the output of the unused pin to low and pull it down to GND with an external resistor of approximately 100 kΩ.



[1] Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR. When data is written to TDR, the TDRE flag is automaticaly cleared to 0. (After the TE bit is set to 1, one frame of 1 is output, then transmission is possible.)

[2] To continue serial transmission, read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR. When data is written to TDR, the TDRE flag is automaticaly cleared to 0.

[3] To output a break in serial transmission, after setting PCR to 1 and PDR to 0, clear the TE bit in SCR3 to 0.

Figure 10.6 Sample Serial Transmission Flowchart (Asynchronous Mode)

13.4.2 Relationship between LCD RAM and Display

The relationship between the LCD RAM and the display segments differs according to the duty cycle. LCD RAM maps for the different duty cycles are shown in figures 13.3 to 13.6.

After setting the registers required for display, data is written to the part corresponding to the duty using the same kind of instruction as for ordinary RAM, and display is started automatically when turned on. Word- or byte-access instructions can be used for RAM setting.

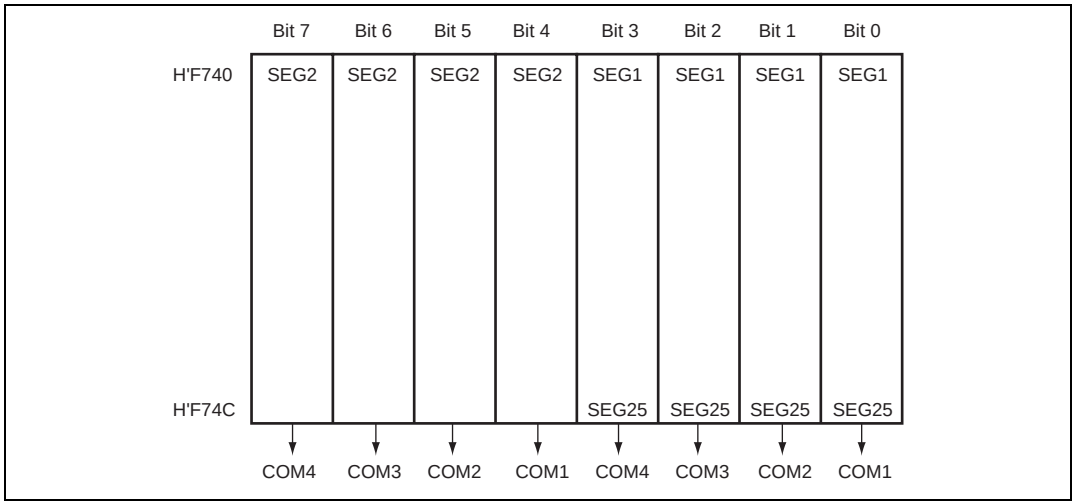


Figure 13.3 LCD RAM Map (1/4 Duty)

Section 14 Power-On Reset and Low-Voltage Detection Circuits (H8/38104 Group Only)

This LSI can include a power-on reset circuit.

The low-voltage detection circuit consists of two circuits: LVDI (interrupt by low voltage detect) and LVDR (reset by low voltage detect) circuits.

This circuit is used to prevent abnormal operation (runaway execution) from occurring due to the power supply voltage fall and to recreate the state before the power supply voltage fall when the power supply voltage rises again.

Even if the power supply voltage falls, the unstable state when the power supply voltage falls below the guaranteed operating voltage can be removed by entering standby mode* when exceeding the guaranteed operating voltage and during normal operation. Thus, system stability can be improved. If the power supply voltage falls more, the reset state is automatically entered. If the power supply voltage rises again, the reset state is held for a specified period, then active mode is automatically entered.

Figure 14.1 is a block diagram of the power-on reset circuit and the low-voltage detection circuit.

Note: * The voltage maintained in standby mode is the same as the RAM data maintenance voltage (V_{RAM}). See section 17.6.2, DC Characteristics, for information on maintenance voltage electrical characteristics.

14.1 Features

- Power-on reset circuit

  Uses an external capacitor to generate an internal reset signal when power is first supplied.
- Low-voltage detection circuit

  LVDR: Monitors the power-supply voltage, and generates an internal reset signal when the voltage falls below a specified value.

  LVDI: Monitors the power-supply voltage, and generates an interrupt when the voltage falls below or rises above respective specified values.

  Two pairs of detection levels for reset generation voltage are available: when only the LVDR circuit is used, or when the LVDI and LVDR circuits are both used.

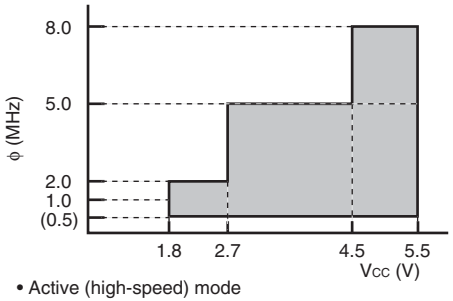
  In addition, power supply rise/drop detection voltages and a detection voltage reference voltage may be input from an external source, allowing the detection level to be set freely by the user.

16.2 Register Bits

Register bit names of the on-chip peripheral modules are described below.

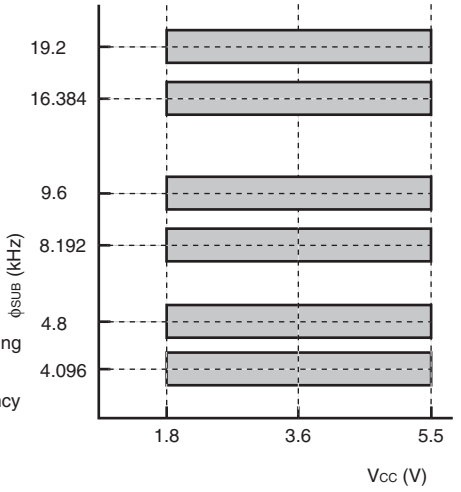
Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
FLMCR1	—	SWE	ESU	PSU	EV	PV	E	P	ROM
FLMCR2	FLER	—	—	—	—	—	—	—	
FLPWCR	PDWND	—	—	—	—	—	—	—	
EBR	—	—	—	EB4	EB3	EB2	EB1	EB0	
FENR	FLSHE	—	—	—	—	—	—	—	
LVDCR*4	LVDE	—	VINTDSEL	VINTUSEL	LVDSL	LVDRE	LVDDE	LVDUE	Low-voltage detect circuit
LVDSR*4	OVF	—	—	—	VREFSEL	—	LVDDF	LVDUF	
ECPWCRH	ECPWCRH7	ECPWCRH6	ECPWCRH5	ECPWCRH4	ECPWCRH3	ECPWCRH2	ECPWCRH1	ECPWCRH0	AEC*1
ECPWCRL	ECPWCRL7	ECPWCRL6	ECPWCRL5	ECPWCRL4	ECPWCRL3	ECPWCRL2	ECPWCRL1	ECPWCRL0	
ECPWDRH	ECPWDRH7	ECPWDRH6	ECPWDRH5	ECPWDRH4	ECPWDRH3	ECPWDRH2	ECPWDRH1	ECPWDRH0	
ECPWDRL	ECPWDRL7	ECPWDRL6	ECPWDRL5	ECPWDRL4	ECPWDRL3	ECPWDRL2	ECPWDRL1	ECPWDRL0	
WEGR	WKEGS7	WKEGS6	WKEGS5	WKEGS4	WKEGS3	WKEGS2	WKEGS1	WKEGS0	Interrupts
SPCR	—	—	SPC32	—	SCINV3	SCINV2	—	—	SCI3
AEGSR	AHEGS1	AHEGS0	ALEGS1	ALEGS0	AIEGS1	AIEGS0	ECPWME	—	AEC*1
ECCR	ACKH1	ACKH0	ACKL1	ACKL0	PWCK2	PWCK1	PWCK0	—	
ECCSR	OVH	OVL	—	CH2	CUEH	CUEL	CRCH	CRCL	
ECH	ECH7	ECH6	ECH5	ECH4	ECH3	ECH2	ECH1	ECH0	
ECL	ECL7	ECL6	ECL5	ECL4	ECL3	ECL2	ECL1	ECL0	
SMR	COM	CHR	PE	PM	STOP	MP	CKS1	CKS0	SCI3
BRR	BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR0	
SCR3	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
TDR	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0	
SSR	TDRE	RDRF	OER	FER	PER	TEND	MPBR	MPBT	
RDR	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0	
TMA	—	—	—	—	TMA3	TMA2	TMA1	TMA0	Timer A
TCA	TCA7	TCA6	TCA5	TCA4	TCA3	TCA2	TCA1	TCA0	
TCSRW	B6WI	TCWE	B4WI	TCSRWE	B2WI	WDON	BOWI	WRST	WDT*2
TCW	TCW7	TCW6	TCW5	TCW4	TCW3	TCW2	TCW1	TCW0	

Power Supply Voltage and Operating Frequency Range

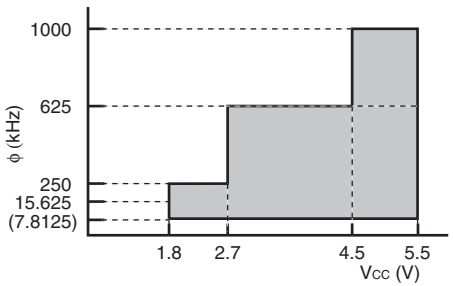


- Active (high-speed) mode
- Sleep (high-speed) mode (except CPU)

Note 1: The values in parentheses is the minimum operating frequency when an external clock is input. When using a resonator, the minimum operating frequency (φ) is 1 MHz.



- Subactive mode
- Subsleep mode (except CPU)
- Watch mode (except CPU)



- Active (medium-speed) mode
- Sleep (medium-speed) mode (except A/D converter)

Note 2: The values in parentheses is the minimum operating frequency when an external clock is input. When using a resonator, the minimum operating frequency (φ) is 15.625 kHz.

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	LCD Power Supply	Oscillator Pins
Active (high-speed) mode (I_{OPE1})	V_{CC}	Only CPU operates	V_{CC}	Stops	System clock: crystal resonator
Active (medium-speed) mode (I_{OPE2})					Subclock: Pin X1 = GND
Sleep mode	V_{CC}	Only timers operate	V_{CC}	Stops	
Subactive mode	V_{CC}	Only CPU operates	V_{CC}	Stops	System clock: crystal resonator
Subsleep mode	V_{CC}	Only timers operate CPU stops	V_{CC}	Stops	Subclock: crystal resonator
Watch mode	V_{CC}	Only clock time base operates CPU stops	V_{CC}	Stops	
Standby mode	V_{CC}	CPU and timers both stop	V_{CC}	Stops	System clock: crystal resonator Subclock: Pin X1 = GND

Notes: 4. Except current which flows to the pull-up MOS or output buffer
5. When the PIOFF bit in the port mode register 9 is 0
6. When the PIOFF bit in the port mode register 9 is 1

17.4.2 DC Characteristics

Table 17.8 lists the DC characteristics.

Table 17.8 DC Characteristics

One of following conditions is applied unless otherwise specified.

Condition A (F-ZTAT version): V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V

Condition B (F-ZTAT version): V_{CC} = 2.2 V to 3.6 V, AV_{CC} = 2.2 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V

Condition C (Mask ROM version): V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V

				Values				
Item	**Symbol**	**Applicable Pins**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**	**Notes**
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{WKP0}$ to $\overline{WKP7}$, $\overline{IRQ0}$, AEVL, AEVH, SCK32		V_{CC} × 0.9	—	V_{CC} + 0.3	V	
		$\overline{IRQ1}$		V_{CC} × 0.9	—	AV_{CC} + 0.3	V	
		RXD32		V_{CC} × 0.8	—	V_{CC} + 0.3	V	
		OSC1		V_{CC} × 0.9	—	V_{CC} + 0.3	V	
		X1	V_{CC} = 1.8 V to 5.5 V	V_{CC} × 0.9	—	V_{CC} + 0.3	V	
		P31 to P37, P40 to P43, P50 to P57, P60 to P67, P70 to P77, P80, PA0 to PA3		V_{CC} × 0.8	—	V_{CC} + 0.3	V	
		PB0 to PB3		V_{CC} × 0.8	—	AV_{CC} + 0.3	V	
		IRQAEC, P95*5		V_{CC} × 0.9	—	V_{CC} + 0.3	V	

17.6.5 LCD Characteristics

Table 17.20 shows the LCD characteristics.

Table 17.20 LCD Characteristics

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Reference Figure
				Min	Typ	Max		
Segment driver step-down voltage	V_{DS}	SEG_1 to SEG_{25}	I_D = 2 µA V1 = 2.7 V to 5.5 V	—	—	0.6	V	*1
Common driver step-down voltage	V_{DC}	COM_1 to COM_4	I_D = 2 µA V1 = 2.7 V to 5.5 V	—	—	0.3	V	*1
LCD power supply split-resistance	R_{LCD}		Between V1 and V_{SS}	1.5	3.0	7.0	MΩ	
Liquid crystal display voltage	V_{LCD}	V_1		2.7	—	5.5	V	*2

Notes: 1. The voltage step-down from power supply pins V1, V2, V3, and V_{SS} to each segment pin or common pin.

2. When the liquid crystal display voltage is supplied from an external power supply, ensure that the following relationship is maintained: $V_{CC} \geq V1 \geq V2 \geq V3 \geq V_{SS}$.

Mnemonic		Operand Size	Addressing Modes/Instruction Length (bytes)								Operation	Condition Code						Number of Execution States
			#xx:8/16	Rn	@Rn	@(d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	—		I	H	N	Z	V	C	
JMP	JMP @Rn	—		2								PC←Rn16	—	—	—	—	—	—	4
	JMP @aa:16	—						4				PC← aa:16	—	—	—	—	—	—	6
	JMP @@aa:8	—								2		PC←@aa:8	—	—	—	—	—	—	8
BSR	BSR d:8	—							2			SP-2→SP PC→@SP PC←PC+d:8	—	—	—	—	—	—	6
JSR	JSR @Rn	—		2								SP-2→SP PC→@SP PC←Rn16	—	—	—	—	—	—	6
	JSR @aa:16	—						4				SP-2→SP PC→@SP PC←aa:16	—	—	—	—	—	—	8
	JSR @@aa:8	—								2		SP-2→SP PC→@SP PC←@aa:8	—	—	—	—	—	—	8
RTS	RTS	—									2	PC←@SP SP+2→SP	—	—	—	—	—	—	8
RTE	RTE	—									2	CCR←@SP SP+2→SP PC←@SP SP+2→SP	↕	↕	↕	↕	↕	↕	10

Table D.3 Product Code Lineup of H8/38002S Group

Product Type			Part No.	Model Marking	Package (Package Code)
H8/38002S	Mask ROM version	Regular product	HD64338002SH	38002 (***) H	64-pin QFP (FP-64A)
			HD64338002SFZ	38002 (***)	64-pin LQFP (FP-64K)
			HD64338002SFT	38002 (***) FT	64-pin QFP (TNP-64B)
		Product with wide-range temperature specifications	HD64338002SHW	38002 (***) H	64-pin QFP (FP-64A)
			HD64338002SFZW	38002 (***)	64-pin LQFP (FP-64K)
			HD64338002SFTW	38002 (***) FT	64-pin QFP (TNP-64B)
H8/38001S	Mask ROM version	Regular product	HD64338001SH	38001 (***) H	64-pin QFP (FP-64A)
			HD64338001SFZ	38001 (***)	64-pin LQFP (FP-64K)
			HD64338001SFT	38001 (***) FT	64-pin QFP (TNP-64B)
		Product with wide-range temperature specifications	HD64338001SHW	38001 (***) H	64-pin QFP (FP-64A)
			HD64338001SFZW	38001 (***)	64-pin LQFP (FP-64K)
			HD64338001SFTW	38001 (***) FT	64-pin QFP (TNP-64B)
H8/38000S	Mask ROM version	Regular product	HD64338000SH	38000 (***) H	64-pin QFP (FP-64A)
			HD64338000SFZ	38000 (***)	64-pin LQFP (FP-64K)
			HD64338000SFT	38000 (***) FT	64-pin QFP (TNP-64B)
		Product with wide-range temperature specifications	HD64338000SHW	38000 (***) H	64-pin QFP (FP-64A)
			HD64338000SFZW	38000 (***)	64-pin LQFP (FP-64K)
			HD64338000SFTW	38000 (***) FT	64-pin QFP (TNP-64B)

Legend:

(***): ROM code