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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	39
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6473802fpv

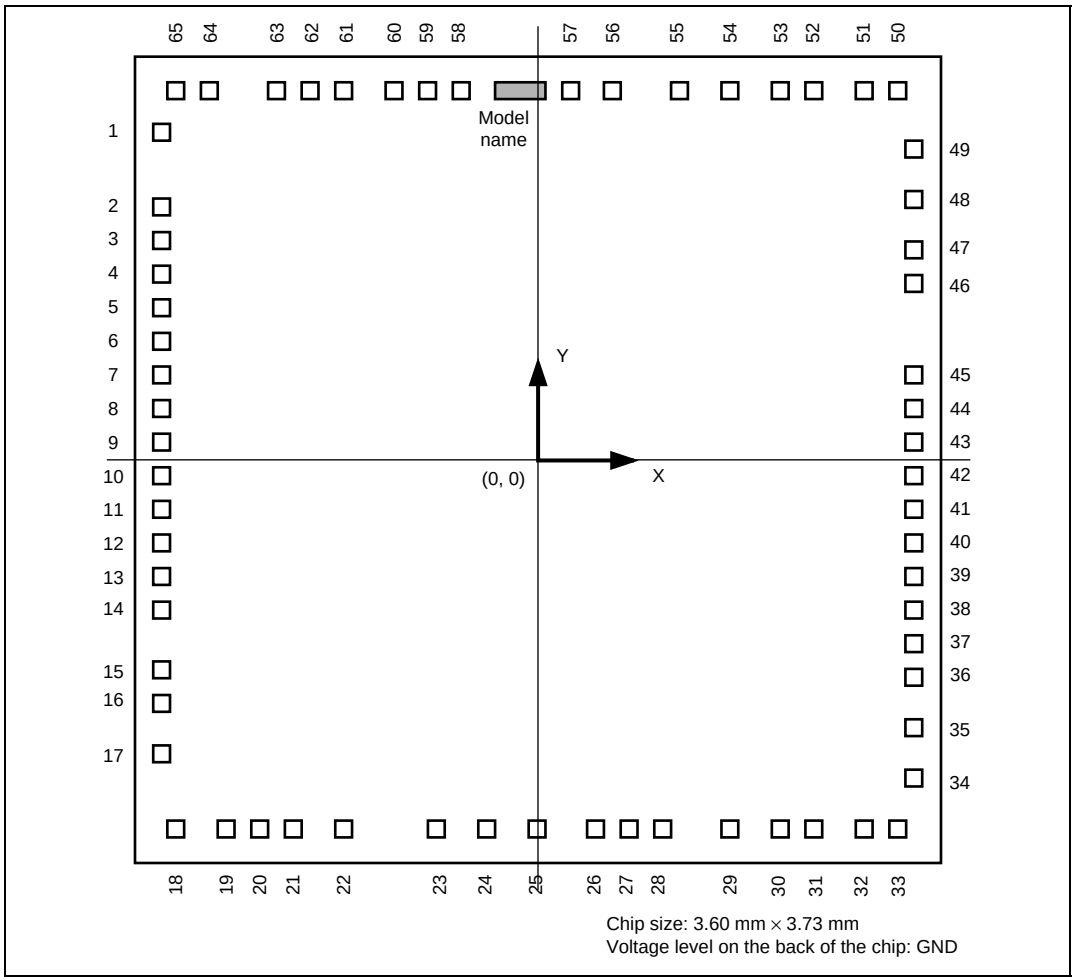

Figure 1.7 Pad Arrangement of HCD6433802, HCD6433801, and HCD6433800 (Top View)

2.5.2 Arithmetic Operations Instructions

Table 2.4 describes the arithmetic operations instructions.

Table 2.4 Arithmetic Operations Instructions

Instruction	Size*	Function
ADD SUB	B/W	Rd ± Rs → Rd, Rd + #IMM → Rd Performs addition or subtraction on data in two general registers, or addition on immediate data and data in a general register. Immediate data cannot be subtracted from data in a general register. Word data can be added or subtracted only when both words are in general registers.
ADDX SUBX	B	Rd ± Rs ± C → Rd, Rd ± #IMM ± C → Rd Performs addition or subtraction with carry on byte data in two general registers, or addition or subtraction with carry on immediate data and data in a general register.
INC DEC	B	Rd ± 1 → Rd Increments or decrements a general register by 1.
ADDS SUBS	W	Rd ± 1 → Rd, Rd ± 2 → Rd Adds or subtracts 1 or 2 to or from a general register.
DAA DAS	B	Rd (decimal adjust) → Rd Decimal-adjusts an addition or subtraction result in a general register by referring to the CCR to produce 4-bit BCD data.
MULXU	B	Rd × Rs → Rd Performs 8-bit × 8-bit unsigned multiplication on data in two general registers, providing a 16-bit result.
DIVXU	B	Rd ÷ Rs → Rd Performs 16-bit ÷ 8-bit unsigned division on data in two general registers, providing an 8-bit quotient and 8-bit remainder.
CMP	B/W	Rd – Rs, Rd – #IMM Compares data in a general register with data in another general register or with immediate data, and sets CCR bits according to the result. Word data can be compared only between two general registers.
NEG	B	0 – Rd → Rd Obtains the two's complement (arithmetic complement) of data in a general register.

Note: * Refers to the operand size.
B: Byte
W: Word

2.5.3 Logic Operations Instructions

Table 2.5 describes the logic operations instructions.

Table 2.5 Logic Operations Instructions

Instruction	Size*	Function
AND	B	Rd ∧ Rs → Rd, Rd ∧ #IMM → Rd Performs a logical AND operation on a general register and another general register or immediate data.
OR	B	Rd ∨ Rs → Rd, Rd ∨ #IMM → Rd Performs a logical OR operation on a general register and another general register or immediate data.
XOR	B	Rd ⊕ Rs → Rd, Rd ⊕ #IMM → Rd Performs a logical exclusive OR operation on a general register and another general register or immediate data.
NOT	B	¬ (Rd) → (Rd) Obtains the one's complement (logical complement) of general register contents.

Note: * Refers to the operand size.
B: Byte

2.5.4 Shift Instructions

Table 2.6 describes the shift instructions.

Table 2.6 Shift Instructions

Instruction	Size*	Function
SHAL SHAR	B	Rd (shift) → Rd Performs an arithmetic shift on general register contents.
SHLL SHLR	B	Rd (shift) → Rd Performs a logical shift on general register contents.
ROTL ROTR	B	Rd (rotate) → Rd Rotates general register contents.
ROTXL ROTXR	B	Rd (rotate) → Rd Rotates general register contents through the carry flag.

Note: * Refers to the operand size.
B: Byte

BCLR instruction executed

```
BCLR    #1,     @PCR3
```

The BCLR instruction is executed for PCR3.

After executing BCLR

	P37	**P36**	**P35**	**P34**	**P33**	**P32**	**P31**	—
Input/output	Output	Output	Output	Output	Output	Output	Input	—
Pin state	Low level	High level	Low level	Low level	Low level	Low level	High level	—
PCR3	1	1	1	1	1	1	0	1
PDR3	1	0	0	0	0	0	0	1

Description on operation

When the BCLR instruction is executed, first the CPU reads PCR3. Since PCR3 is a write-only register, the CPU reads a value of H'FF, even though the PCR3 value is actually H'3F.

Next, the CPU clears bit 1 in the read data to 0, changing the data to H'FD.

Finally, H'FD is written to PCR3 and BCLR instruction execution ends.

As a result of this operation, bit 1 in PCR3 becomes 0, making P31 an input port. However, bits 7 and 6 in PCR3 change to 1, so that P37 and P36 change from input pins to output pins. To prevent this problem, store a copy of the PCR3 data in a work area in memory and manipulate data of the bit in the work area, then write this data to PCR3.

Prior to executing BCLR

```
MOV.B   #3F,   R0L
MOV.B   R0L,   @RAM0
MOV.B   R0L,   @PCR3
```

The PCR3 value (H'3F) is written to a work area in memory (RAM0) as well as to PCR3.

In the above example, an IRQ0 interrupt occurs while the AND.B instruction is executed. Since not only the original target IRRI1, but also IRRI0 is cleared to 0, the IRQ0 interrupt becomes invalid.

3.5.4 Notes on Rewriting Port Mode Registers

When a port mode register is rewritten to switch the functions of external interrupt pins, IRQAEC, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$, and $\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$, the interrupt request flag may be set to 1.

When switching a pin function, mask the interrupt before setting the bit in the port mode register. After accessing the port mode register, execute at least one instruction (e.g., NOP), then clear the interrupt request flag from 1 to 0.

Table 3.3 lists the interrupt request flags which are set to 1 and the conditions.

Table 3.3 Conditions under which Interrupt Request Flag Is Set to 1

Interrupt Request Flags Set to 1		Conditions
IRR1	IRREC2	When the edge designated by AIEGS1 and AIEGS0 in AEGSR is input while IENEC2 in IENRI is set to 1.
	IRRI1	When IRQ1 bit in PMRB is changed from 0 to 1 while pin $\overline{\text{IRQ1}}$ is low and IEG1 bit in IEGR = 0.
		When IRQ1 bit in PMRB is changed from 1 to 0 while pin $\overline{\text{IRQ1}}$ is low and IEG1 bit in IEGR = 1.
	IRRI0	When IRQ0 bit in PMR2 is changed from 0 to 1 while pin $\overline{\text{IRQ0}}$ is low and IEG0 bit in IEGR = 0.
		When IRQ0 bit in PMR2 is changed from 1 to 0 while pin $\overline{\text{IRQ0}}$ is low and IEG0 bit in IEGR = 1.

Section 4 Clock Pulse Generators

4.1 Features

Clock oscillator circuitry (CPG: clock pulse generator) is provided on-chip, including both a system clock pulse generator and a subclock pulse generator. In the H8/38104 Group, the system clock pulse generator includes an on-chip oscillator. The system clock pulse generator consists of a system clock oscillator and system clock dividers. The subclock pulse generator consists of a subclock oscillator and a subclock divider.

Figure 4.1 shows a block diagram of the clock pulse generators of the H8/3802, H8/38004 and H8/38002S Group. Figure 4.2 shows a block diagram of the clock pulse generators of the H8/38104 Group.

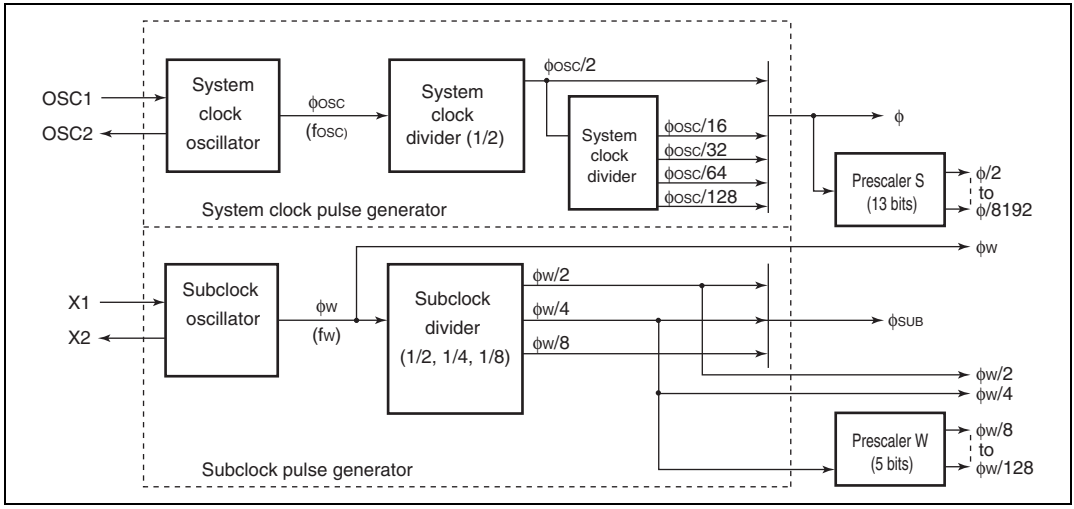

Figure 4.1 Block Diagram of Clock Pulse Generators (H8/3802, H8/38004, H8/38002S Group)

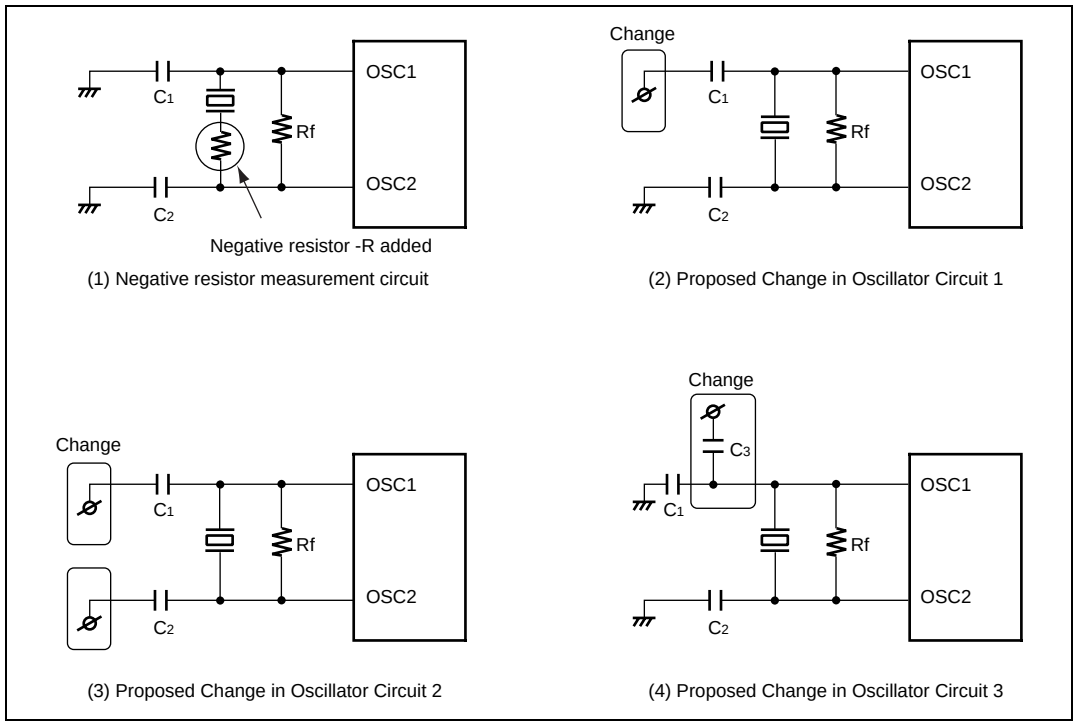

Figure 4.14 Negative Resistor Measurement and Proposed Changes in Circuit

4.6.2 Notes on Board Design

When using a crystal resonator (ceramic resonator), place the resonator and its load capacitors as close as possible to the OSC1 and OSC2 pins. Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 4.15).

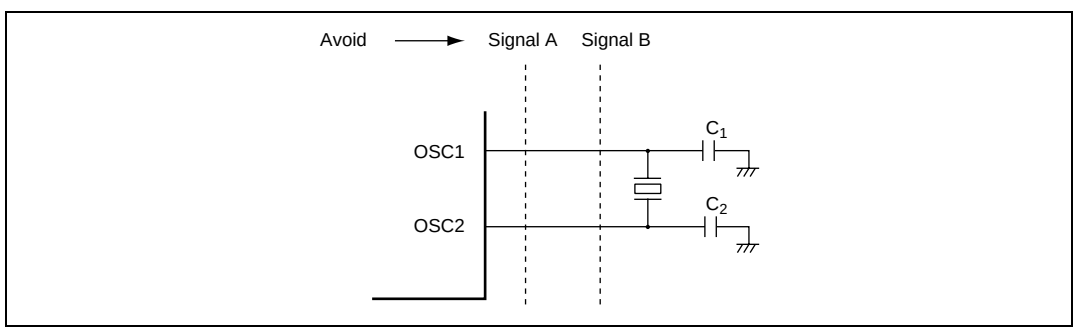

Figure 4.15 Example of Incorrect Board Design

6.6.1 Flash Memory Control Register 1 (FLMCR1)

FLMCR1 is a register that makes the flash memory change to program mode, program-verify mode, erase mode, or erase-verify mode. For details on register setting, refer to section 6.8, Flash Memory Programming/Erasing.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0.
6	SWE	0	R/W	Software Write Enable When this bit is set to 1, flash memory programming/erasing is enabled. When this bit is cleared to 0, flash memory programming/erasing is invalid. Other FLMCR1 bits and all EBR bits cannot be set.
5	ESU	0	R/W	Erase Setup When this bit is set to 1, the flash memory changes to the erase setup state. When it is cleared to 0, the erase setup state is cancelled. Set this bit to 1 before setting the E bit to 1 in FLMCR1.
4	PSU	0	R/W	Program Setup When this bit is set to 1, the flash memory changes to the program setup state. When it is cleared to 0, the program setup state is cancelled. Set this bit to 1 before setting the P bit in FLMCR1.
3	EV	0	R/W	Erase-Verify When this bit is set to 1, the flash memory changes to erase-verify mode. When it is cleared to 0, erase-verify mode is cancelled.
2	PV	0	R/W	Program-Verify When this bit is set to 1, the flash memory changes to program-verify mode. When it is cleared to 0, program-verify mode is cancelled.
1	E	0	R/W	Erase When this bit is set to 1, and while the SWE = 1 and ESU = 1 bits are 1, the flash memory changes to erase mode. When it is cleared to 0, erase mode is cancelled.
0	P	0	R/W	Program When this bit is set to 1, and while the SWE = 1 and PSU = 1 bits are 1, the flash memory changes to program mode. When it is cleared to 0, program mode is cancelled.

Note: Bits SWE, PSU, EV, PV, E, and P should not be set at the same time.

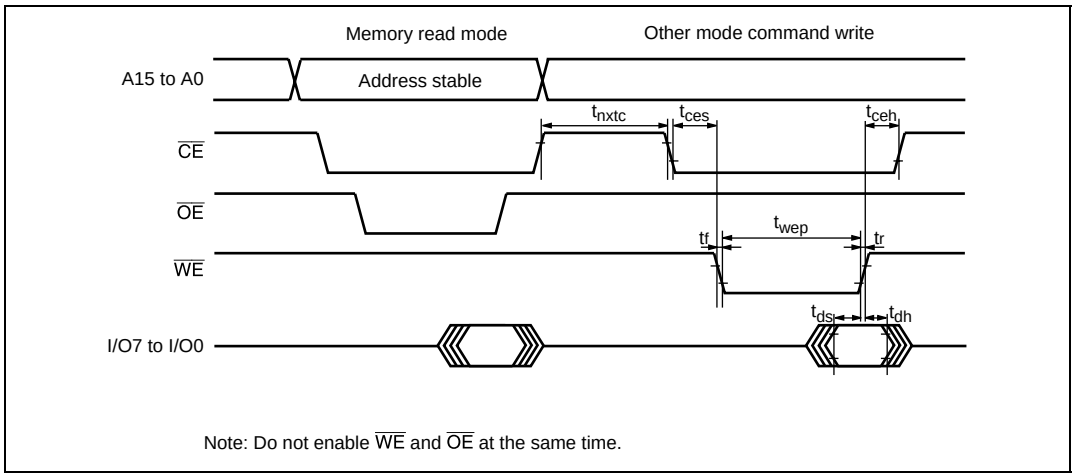

Figure 6.14 Timing Waveforms in Transition from Memory Read Mode to Another Mode

Table 6.14 AC Characteristics in Memory Read Mode

(Conditions: V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V, Ta = 25°C ±5°C)

Item	Symbol	Min	Max	Unit	Test Condition
Access time	t_{acc}	—	20	µs	Figures 6.15 and 6.16
$\overline{CE}$ output delay time	t_{ce}	—	150	ns	
$\overline{OE}$ output delay time	t_{oe}	—	150	ns	
Output disable delay time	t_{df}	—	100	ns	
Data output hold time	t_{oh}	5	—	ns	

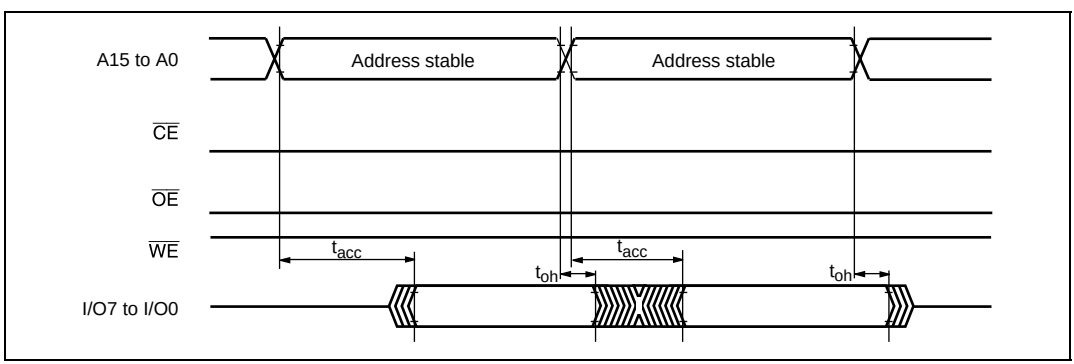

Figure 6.15 Timing Waveforms in $\overline{CE}$ and $\overline{OE}$ Enable State Read

8.7.1 Port Data Register 9 (PDR9)

PDR9 is a register that stores data of port 9.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 1	—	Reserved The initial value should not be changed.
5	P95	1	R/W	If PDR9 is read, the values stored in PDR9 are read.
4	P94*	1	R/W	
3	P93	1	R/W	
2	P92	1	R/W	
1	P91	1	R/W	
0	P90	1	R/W	

Note: * There is no pin 94, and its function is not implemented, on the H8/38104 Group. However, the register is read/write enabled.

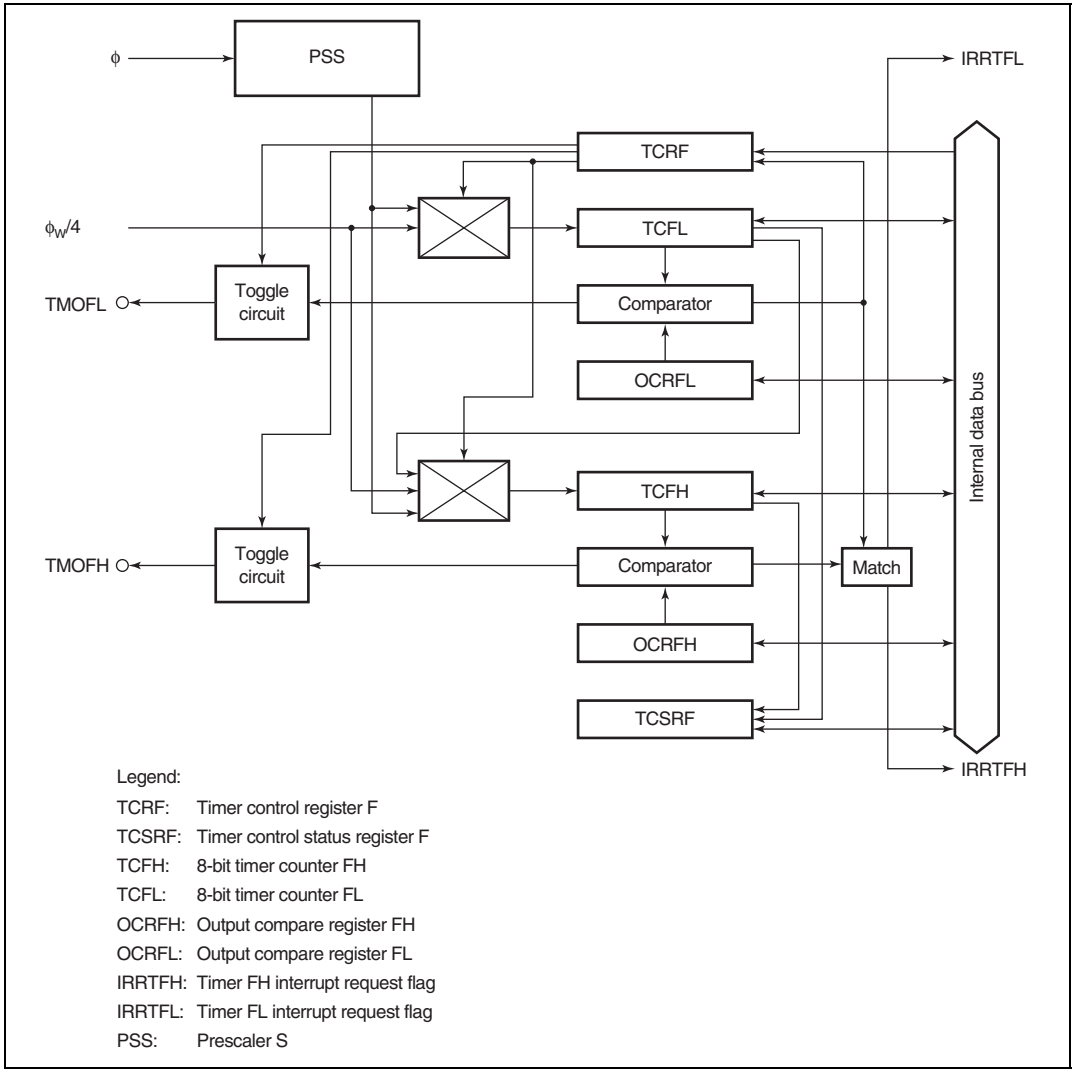

Figure 9.2 Block Diagram of Timer F

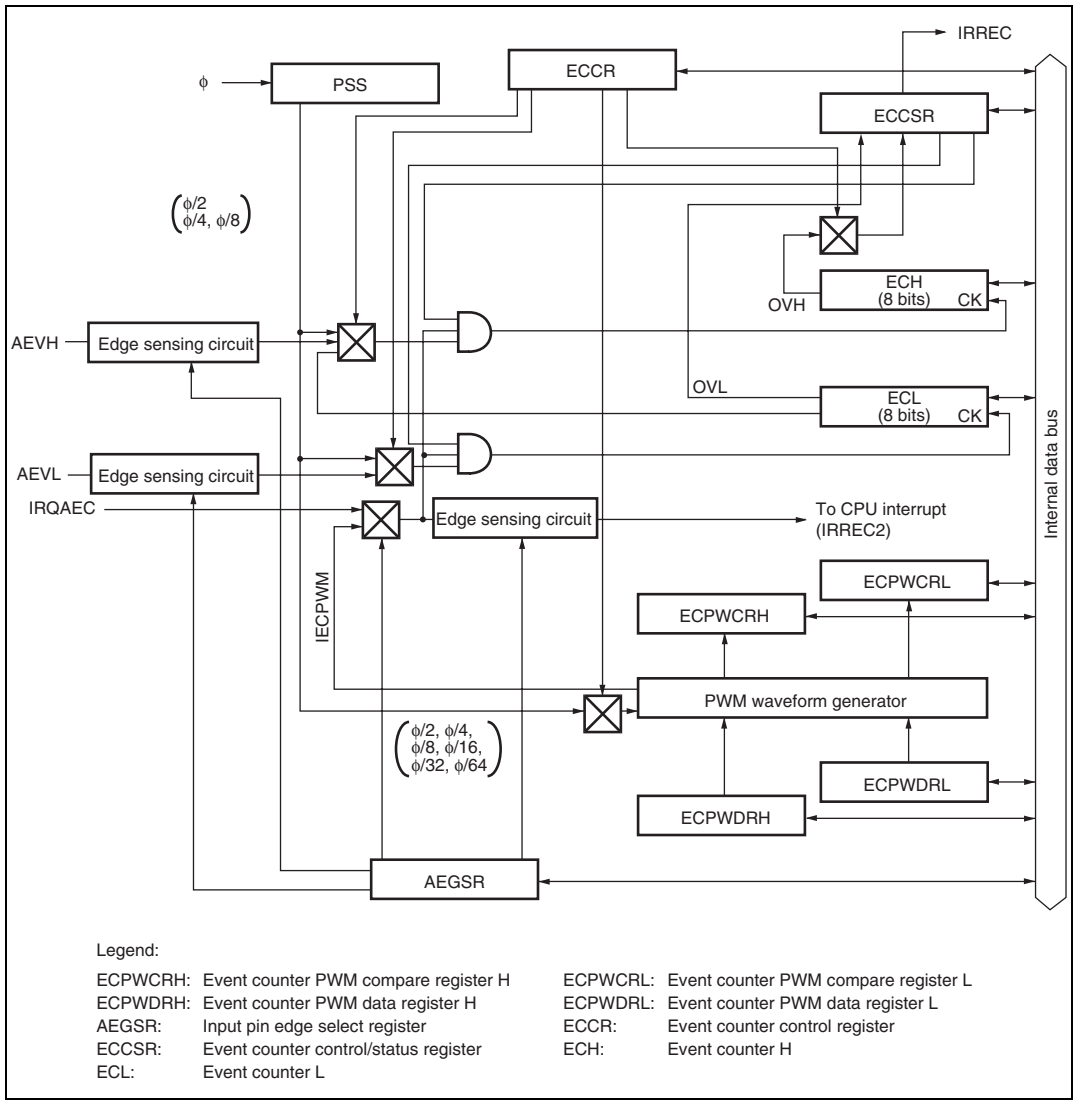

Figure 9.7 Block Diagram of Asynchronous Event Counter

Event Counter PWM Data Register H (ECPWDRH): ECPWDRH controls data of the event counter PWM waveform generator.

Bit	Bit Name	Initial Value	R/W	Description
7	ECPWDRH7	0	W	Data control of event counter PWM waveform generator
6	ECPWDRH6	0	W	
5	ECPWDRH5	0	W	
4	ECPWDRH4	0	W	
3	ECPWDRH3	0	W	
2	ECPWDRH2	0	W	
1	ECPWDRH1	0	W	
0	ECPWDRH0	0	W	

Notes: When ECPWME in AEGSR is 1, the event counter PWM is operating and therefore ECPWDRH should not be modified.

When changing the data, the event counter PWM must be halted by clearing ECPWME to 0 in AEGSR before modifying ECPWDRH.

Event Counter PWM Data Register L (ECPWDRL): ECPWDRL controls data of the event counter PWM waveform generator.

Bit	Bit Name	Initial Value	R/W	Description
7	ECPWDRL7	0	W	Data control of event counter PWM waveform generator
6	ECPWDRL6	0	W	
5	ECPWDRL5	0	W	
4	ECPWDRL4	0	W	
3	ECPWDRL3	0	W	
2	ECPWDRL2	0	W	
1	ECPWDRL1	0	W	
0	ECPWDRL0	0	W	

Notes: When ECPWME in AEGSR is 1, the event counter PWM is operating and therefore ECPWDRL should not be modified.

When changing the data, the event counter PWM must be halted by clearing ECPWME to 0 in AEGSR before modifying ECPWDRL.

10.4.3 Data Transmission

Figure 10.5 shows an example of operation for transmission in asynchronous mode. In transmission, the SCI3 operates as described below.

1. The SCI3 monitors the TDRE flag in SSR. If the flag is cleared to 0, the SCI3 recognizes that data has been written to TDR, and transfers the data from TDR to TSR.
2. After transferring data from TDR to TSR, the SCI3 sets the TDRE flag to 1 and starts transmission. If the TIE bit is set to 1 at this time, a TXI interrupt request is generated. Continuous transmission is possible because the TXI interrupt routine writes next transmit data to TDR before transmission of the current transmit data has been completed.
3. The SCI3 checks the TDRE flag at the timing for sending the stop bit.
4. If the TDRE flag is 0, the data is transferred from TDR to TSR, the stop bit is sent, and then serial transmission of the next frame is started.
5. If the TDRE flag is 1, the TEND flag in SSR is set to 1, the stop bit is sent, and then the "mark state" is entered, in which 1 is output. If the TEIE bit in SCR3 is set to 1 at this time, a TEI interrupt request is generated.
6. Figure 10.6 shows a sample flowchart for transmission in asynchronous mode.

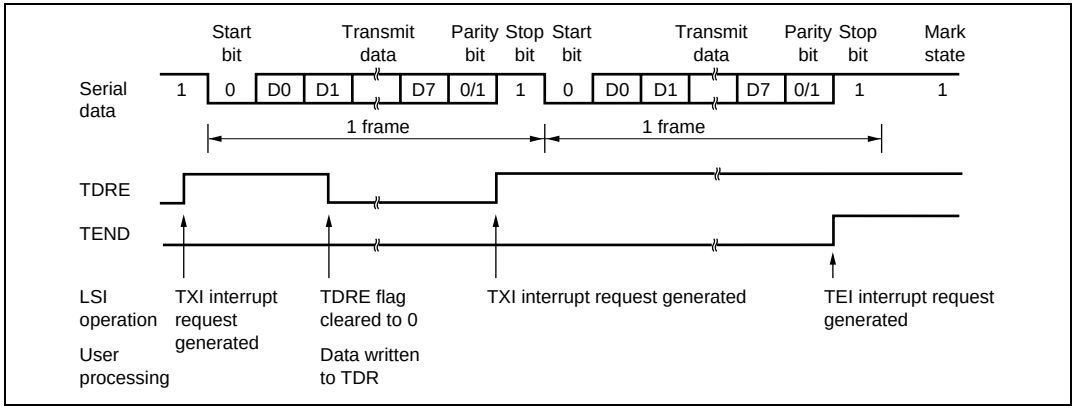

Figure 10.5 Example SCI3 Operation in Transmission in Asynchronous Mode (8-Bit Data, Parity, One Stop Bit)

transmitter is initialized regardless of the current transmission state, the TXD32 pin becomes an I/O port, and 0 is output from the TXD32 pin.

10.7.3 Receive Error Flags and Transmit Operations (Clocked Synchronous Mode Only)

Transmission cannot be started when a receive error flag (OER, PER, or FER) is set to 1, even if the TDRE flag is cleared to 0. Be sure to clear the receive error flags to 0 before starting transmission. Note also that receive error flags cannot be cleared to 0 even if the RE bit is cleared to 0.

10.7.4 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI3 operates on a basic clock with a frequency of 16 times the transfer rate. In reception, the SCI3 samples the falling edge of the start bit using the basic clock, and performs internal synchronization. Receive data is latched internally at the rising edge of the 8th pulse of the basic clock as shown in figure 10.16.

Thus, the reception margin in asynchronous mode is given by formula (1) below.

$$M = \left\{ \left(0.5 - \frac{1}{2N}\right) - \frac{D - 0.5}{N} - (L - 0.5)\,F \right\} \times 100(\%)$$

... Formula (1)

Where N : Ratio of bit rate to clock (N = 16)
D : Clock duty (D = 0.5 to 1.0)
L : Frame length (L = 9 to 12)
F : Absolute value of clock rate deviation

Assuming values of F (absolute value of clock rate deviation) = 0 and D (clock duty) = 0.5 in formula (1), the reception margin can be given by the formula.

$M = \{0.5 - 1/(2 \times 16)\} \times 100\ [\%] = 46.875\%$

However, this is only the computed value, and a margin of 20% to 30% should be allowed for in system design.

Section 11 10-Bit PWM

This LSI has a two-channel 10-bit PWM. The PWM with a low-path filter connected can be used as a D/A converter. Figure 11.1(1) shows a block diagram of the 10-bit PWM of the H8/3802 Group, H8/38004 Group and H8/38002S Group. Figure 11.1(2) shows a block diagram of the 10-bit PWM of the H8/38104 Group.

11.1 Features

- Choice of four conversion periods

  A conversion period of 4096/ϕ with a minimum modulation width of 4/ϕ, a conversion period of 2048/ϕ with a minimum modulation width of 2/ϕ, a conversion period of 1024/ϕ with a minimum modulation width of 1/ϕ, or a conversion period of 512/ϕ with a minimum modulation width of 1/2ϕ can be selected.
- Pulse division method for less ripple
- Use of module standby mode enables this module to be placed in standby mode independently when not used. (For details, refer to section 5.4, Module Standby Function.)
- On the H8/38104 Group it is possible to select between two types of PWM output: pulse-division 10-bit PWM and event counter PWM (PWM incorporating AEC). (The H8/3802 Group, H8/38004 Group and H8/38002S Group can only produce 10-bit PWM output.) Refer to section 9.4, Asynchronous Event Counter (AEC), for information on event counter PWM.

Figures 13.1(1) and 13.1(2) show a block diagram of the LCD controller/driver.

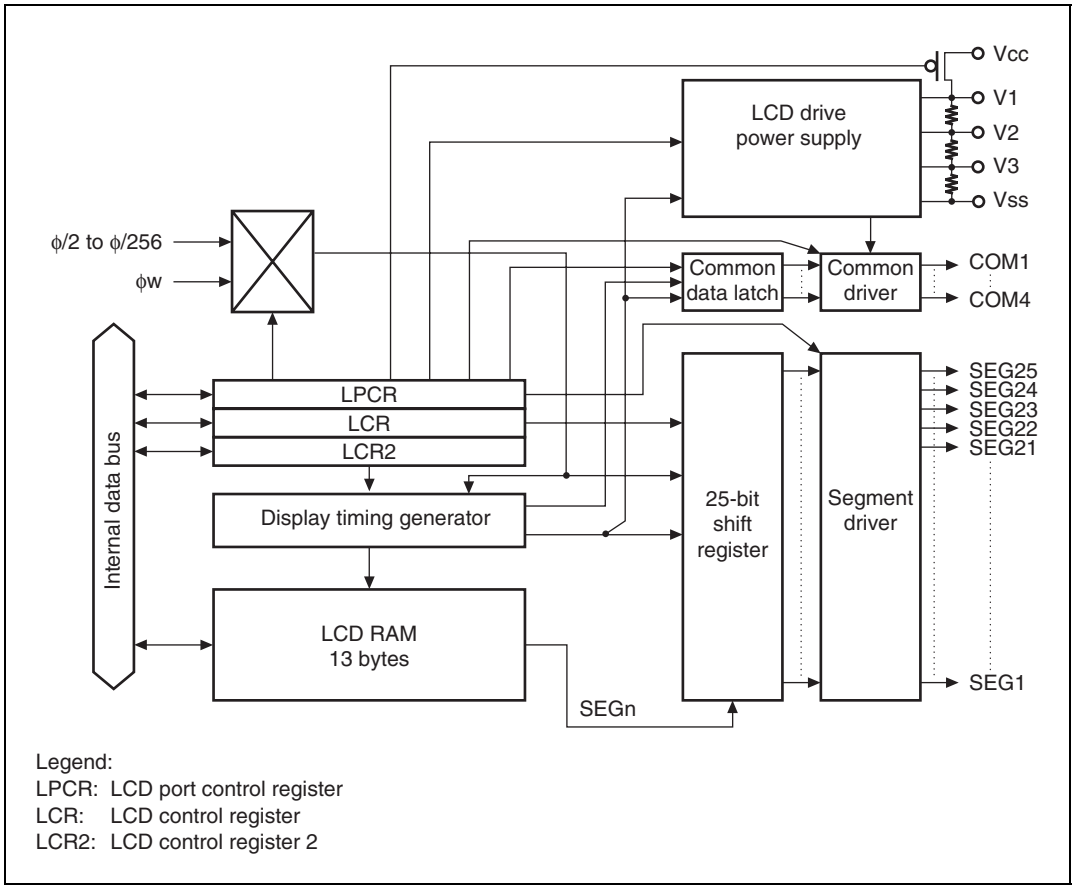

Figure 13.1(1) Block Diagram of LCD Controller/Driver (H8/3802 Group, H8/38004 Group, H8/38002S Group)

Register Name	Abbre-viation	Bit No	Address	Module Name	Data Bus Width	Access State
Transmit data register	TDR	8	H'FFAB	SCI3	8	3
Serial status register	SSR	8	H'FFAC	SCI3	8	3
Receive data register	RDR	8	H'FFAD	SCI3	8	3
Timer mode register A	TMA	8	H'FFB0	Timer A	8	2
Timer counter A	TCA	8	H'FFB1	Timer A	8	2
Timer control/status register W	TCSRW	8	H'FFB2	WDT*2	8	2
Timer counter W	TCW	8	H'FFB3	WDT*2	8	2
Timer control register F	TCRF	8	H'FFB6	Timer F	8	2
Timer control status register F	TCSRF	8	H'FFB7	Timer F	8	2
8-bit timer counter FH	TCFH	8	H'FFB8	Timer F	8	2
8-bit timer counter FL	TCFL	8	H'FFB9	Timer F	8	2
Output compare register FH	OCRFH	8	H'FFBA	Timer F	8	2
Output compare register FL	OCRFL	8	H'FFBB	Timer F	8	2
LCD port control register	LPCR	8	H'FFC0	LCD*3	8	2
LCD control register	LCR	8	H'FFC1	LCD*3	8	2
LCD control register 2	LCR2	8	H'FFC2	LCD*3	8	2
Low-voltage detection counter*4	LVDCNT	8	H'FFC3	LVD	8	2
A/D result register H	ADRRH	8	H'FFC4	A/D converter	8	2
A/D result register L	ADRRL	8	H'FFC5	A/D converter	8	2
A/D mode register	AMR	8	H'FFC6	A/D converter	8	2
A/D start register	ADSR	8	H'FFC7	A/D converter	8	2
Port mode register 2	PMR2	8	H'FFC9	I/O port	8	2
Port mode register 3	PMR3	8	H'FFCA	I/O port	8	2
Port mode register 5	PMR5	8	H'FFCC	I/O port	8	2
PWM2 control register	PWCR2	8	H'FFCD	10-bit PWM	8	2
PWM2 data register U	PWDRU2	8	H'FFCE	10-bit PWM	8	2
PWM2 data register L	PWDRL2	8	H'FFCF	10-bit PWM	8	2
PWM1 control register	PWCR1	8	H'FFD0	10-bit PWM	8	2
PWM1 data register U	PWDRU1	8	H'FFD1	10-bit PWM	8	2
PWM1 data register L	PWDRL1	8	H'FFD2	10-bit PWM	8	2
Port data register 3	PDR3	8	H'FFD6	I/O port	8	2
Port data register 4	PDR4	8	H'FFD7	I/O port	8	2