Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	16MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	39
Program Memory Size	16KB (16K x 8)
Program Memory Type	PROM
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b SAR
Oscillator Type	External, Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6473802hv

Figures

Section 1 Overview

Section 2 CPU

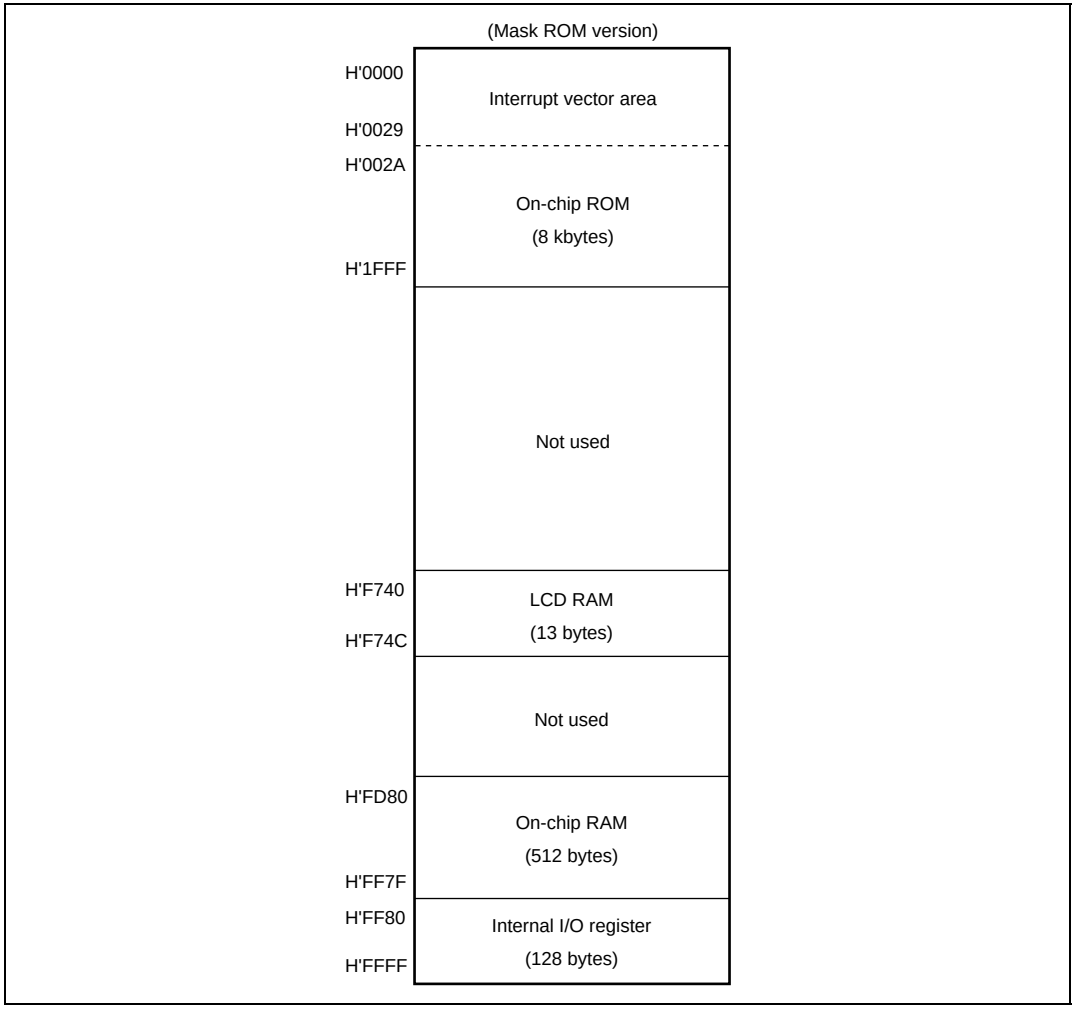


Figure 2.1(9) H8/38000, H8/38000S, H8/38100 Memory Map

2.5 Instruction Set

The H8/300L CPU can use a total of 55 instructions, which are grouped by function in table 2.1.

Table 2.1 Instruction Set

Function	Instructions	Number
Data transfer	MOV, PUSH*1, POP*1	1
Arithmetic operations	ADD, SUB, ADDX, SUBX, INC, DEC, ADDS, SUBS, DAA, DAS, MULXU, DIVXU, CMP, NEG	14
Logic operations	AND, OR, XOR, NOT	4
Shift	SHAL, SHAR, SHLL, SHLR, ROTL, ROTR, ROTXL, ROTXR	8
Bit manipulation	BSET, BCLR, BNOT, BTST, BAND, BIAND, BOR, BIOR, BXOR, BIXOR, BLD, BILD, BST, BIST	14
Branch	Bcc*2, JMP, BSR, JSR, RTS	5
System control	RTE, SLEEP, LDC, STC, ANDC, ORC, XORC, NOP	8
Block data transfer	EEPMOV	1
		Total: 55

Notes: 1. PUSH Rn is equivalent to MOV.W Rn, @–SP.
POP Rn is equivalent to MOV.W @SP+, Rn. The same applies to the machine language.
2. Bcc is the general name for conditional branch instructions.

Tables 2.3 to 2.10 summarize the instructions in each functional category. The notation used in tables 2.3 to 2.10 is defined below.

BCLR instruction executed

```
BCLR    #1,     @PCR3
```

The BCLR instruction is executed for PCR3.

After executing BCLR

	P37	**P36**	**P35**	**P34**	**P33**	**P32**	**P31**	—
Input/output	Output	Output	Output	Output	Output	Output	Input	—
Pin state	Low level	High level	Low level	Low level	Low level	Low level	High level	—
PCR3	1	1	1	1	1	1	0	1
PDR3	1	0	0	0	0	0	0	1

Description on operation

When the BCLR instruction is executed, first the CPU reads PCR3. Since PCR3 is a write-only register, the CPU reads a value of H'FF, even though the PCR3 value is actually H'3F.

Next, the CPU clears bit 1 in the read data to 0, changing the data to H'FD.

Finally, H'FD is written to PCR3 and BCLR instruction execution ends.

As a result of this operation, bit 1 in PCR3 becomes 0, making P31 an input port. However, bits 7 and 6 in PCR3 change to 1, so that P37 and P36 change from input pins to output pins. To prevent this problem, store a copy of the PCR3 data in a work area in memory and manipulate data of the bit in the work area, then write this data to PCR3.

Prior to executing BCLR

```
MOV.B   #3F,   R0L
MOV.B   R0L,   @RAM0
MOV.B   R0L,   @PCR3
```

The PCR3 value (H'3F) is written to a work area in memory (RAM0) as well as to PCR3.

	P37	P36	P35	P34	P33	P32	P31	—
Input/output	Input	Input	Output	Output	Output	Output	Output	—
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	—
PCR3	0	0	1	1	1	1	1	1
PDR3	1	0	0	0	0	0	0	1
RAM0	0	0	1	1	1	1	1	1

BCLR instruction executed

```
BCLR   #1,    @RAM0
```

The BCLR instructions executed for the PCR3 work area (RAM0).

After executing BCLR

```
MOV.B   @RAM0, R0L
MOV.B   R0L,  @PCR3
```

The work area (RAM0) value is written to PCR3.

	P37	P36	P35	P34	P33	P32	P31	—
Input/output	Input	Input	Output	Output	Output	Output	Output	—
Pin state	Low level	High level	Low level	Low level	Low level	Low level	High level	—
PCR3	0	0	1	1	1	1	0	1
PDR3	1	0	0	0	0	0	0	1
RAM0	0	0	1	1	1	1	0	1

The following is an example in assembler.

```
  .ORG  H'0000
  .DATA.W      INIT
  .ORG  H'0100
INIT:
 MOV.W  #H'FF80:16,SP

 MOV.B  #H'9E:8,R0L
 MOV.B  R0L,@H'FFC3:8
 MOV.B  @H'FFC3:8,R0L
 MOV.B  #H'F1:8,R0L
 MOV.B  R0L,@H'FFC3:8
 MOV.B  #H'BF:8,R0L
 MOV.B  R0L,@H'FFFA:8
 ANDC.B #H'7F:8,CCR       ; user program
```

The following is an example in C.

```
   void powerON_Reset(void)
   {
   // ----------------------------------------------------
            unsigned char dummy;
            *((volatile unsigned char *)0xffc3)= 0x9e;
            dummy = *((volatile unsigned char *)0xffc3);
            *((volatile unsigned char *)0xffc3)= 0xf1;
            *((volatile unsigned char *)0xfffa)= 0xbf;
   // ----------------------------------------------------
            set_imask_ccr(0);       // clear I bit
                                    // user program
   }
```

On the mask ROM version of the product, user programs may be used as is (including the additional steps described above) or without the additional steps.

3.1 Exception Sources and Vector Address

Table 3.1 shows the vector addresses and priority of each exception handling. When more than one interrupt is requested, handling is performed from the interrupt with the highest priority.

Table 5.2 Transition Mode after SLEEP Instruction Execution and Interrupt Handling

LSON	MSON	SSBY	TMA3	DTON	Transition Mode after SLEEP Instruction Execution	Transition Mode due to Interrupt
0	0	0	X	0	Sleep (high-speed) mode	Active (high-speed) mode
0	1	0	X	0	Sleep (medium-speed) mode	Active (medium-speed) mode
1	X	0	1	0	Subsleep mode	Subactive mode
0	X	1	0	0	Standby mode	Active mode
X	X	1	1	0	Watch mode	Active mode, subactive mode
0	0	0	X	1	Active (high-speed) mode	—
0	1	0	X	1	Active (medium-speed) mode	—
0	1	1	1	1	Active (medium-speed) mode	—
1	X	1	1	1	Subactive mode (direct transition)	—
0	0	1	1	1	Active (high-speed) mode (direct transition)	—

Legend: X: Don’t care.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
5	SPC32	0	R/W	P42/TXD32 Pin Function Switch This bit selects whether pin P42/TXD32 is used as P42 or as TXD32. 0: P42 I/O pin 1: TXD32 output pin* Note: * Set the TE bit in SCR3 after setting this bit to 1.
4	—	—	W	Reserved The write value should always be 0.
3	SCINV3	0	R/W	TXD32 Pin Output Data Inversion Switch This bit selects whether or not the logic level of the TXD32 pin output data is inverted. 0: TXD32 output data is not inverted 1: TXD32 output data is inverted
2	SCINV2	0	R/W	RXD32 Pin Input Data Inversion Switch This bit selects whether or not the logic level of the RXD32 pin input data is inverted. 0: RXD32 input data is not inverted 1: RXD32 input data is inverted
1, 0	—	—	W	Reserved The write value should always be 0.

Note: When the serial port control register is modified, the data being input or output up to that point is inverted immediately after the modification, and an invalid data change is input or output. When modifying the serial port control register, modification must be made in a state in which data changes are invalidated.

9.3.2 Input/Output Pins

Table 9.3 shows the pin configuration of the timer F.

Table 9.3 Pin Configuration

Name	Abbreviation	I/O	Function
Timer FH output	TMOFH	Output	Timer FH toggle output pin
Timer FL output	TMOFL	Output	Timer FL toggle output pin

9.3.3 Register Descriptions

The timer F has the following registers.

- Timer counters FH and FL (TCFH,TCFL)
- Output compare registers FH and FL (OCRFH, OCRFL)
- Timer control register F (TCRF)
- Timer control status register F (TCSRF)

Timer Counters FH and FL (TCFH, TCFL): TCF is a 16-bit read/write up-counter configured by cascaded connection of 8-bit timer counters TCFH and TCFL. In addition to the use of TCF as a 16-bit counter with TCFH as the upper 8 bits and TCFL as the lower 8 bits, TCFH and TCFL can also be used as independent 8-bit counters.

TCFH and TCFL can be read and written by the CPU, but when they are used in 16-bit mode, data transfer to and from the CPU is performed via a temporary register (TEMP). For details of TEMP, see section 9.3.4, CPU Interface. TCFH and TCFL are initialized to H'00 upon reset.

- 16-bit mode (TCF)

  When CKSH2 is cleared to 0 in TCRF, TCF operates as a 16-bit counter. The TCF input clock is selected by bits CKSL2 to CKSL0 in TCRF.

  TCF can be cleared in the event of a compare match by means of CCLRH in TCSRF.

  When TCF overflows from H'FFFF to H'0000, OVFH is set to 1 in TCSRF. If OVIEH in TCSRF is 1 at this time, IRRTFH is set to 1 in IRR2, and if IENTFH in IENR2 is 1, an interrupt request is sent to the CPU.

- 8-bit mode (TCFL/TCFH)

  When CKSH2 is set to 1 in TCRF, TCFH and TCFL operate as two independent 8-bit counters. The TCFH (TCFL) input clock is selected by bits CKSH2 to CKSH0 (CKSL2 to CKSL0) in TCRF.

Table 13.4 Frame Frequency Selection

Bit 3: CKS3	Bit 2: CKS2	Bit 1: CKS1	Bit 0: CKS0	Operating Clock	Frame Frequency*1	
					ϕ = 2 MHz	ϕ = 250 kHz*3
0	X	0	0	ϕ_W	128 Hz*2	128 Hz*2
			1	$\phi_W/2$	64 Hz*2	64 Hz*2
		1	X	$\phi_W/4$	32 Hz*2	32 Hz*2
1	0	0	0	$\phi/2$	—	244 Hz
			1	$\phi/4$	977 Hz	122 Hz
		1	0	$\phi/8$	488 Hz	61 Hz
			1	$\phi/16$	244 Hz	30.5 Hz
	1	0	0	$\phi/32$	122 Hz	—
			1	$\phi/64$	61 Hz	—
		1	0	$\phi/128$	30.5 Hz	—
			1	$\phi/256$	—	—

Legend:

X: Don't care

Notes: 1. When 1/3 duty is selected, the frame frequency is 4/3 times the value shown.

2. This is the frame frequency when ϕ_W = 32.768 kHz.

3. This is the frame frequency in active (medium-speed, $\phi_{OSC}/16$) mode when ϕ = 2 MHz.

Bit	Bit Name	Initial Value	R/W	Description
3	LVDSEL	0*	R/W	LVDR Detection Level Select 0: Reset detection voltage 2.3 V (typ.) 1: Reset detection voltage 3.3 V (typ.) Select 2.3 V (typical) reset if voltage rise and drop detection interrupts are to be used. For reset detection only, Select 3.3 V (typical) reset.
2	LVDRE	0*	R/W	LVDR Enable 0: LVDR resets disabled 1: LVDR resets enabled
1	LVDDE	0	R/W	Voltage Drop Interrupt Enable 0: Voltage drop interrupt requests disabled 1: Voltage drop interrupt requests enabled
0	LVDUE	0	R/W	Voltage Rise Interrupt Enable 0: Voltage rise interrupt requests disabled 1: Voltage rise interrupt requests enabled

Note: * These bits are not initialized by resets trigged by LVDR. They are initialized by power-on resets and watchdog timer resets.

Table 14.1 LVDCR Settings and Select Functions

LVDCR Settings					Select Functions			
LVDE	LVDSEL	LVDRE	LVDDE	LVDUE	Power-On Reset	LVDR	Low-Voltage-Detection Falling Interrupt	Low-Voltage-Detection Rising Interrupt
0	*	*	*	*	O	—	—	—
1	1	1	0	0	O	O	—	—
1	0	0	1	0	O	—	O	—
1	0	0	1	1	O	—	O	O
1	0	1	1	1	O	O	O	O

Legend: * means invalid.

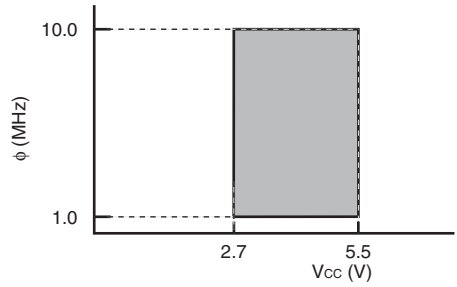
Table 17.2 DC Characteristics (5)

V_{CC} = 1.8 V to 5.5 V, AV_{CC} = 1.8 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified (including subactive mode), T_a = –20°C to +75°C (product with regular specifications), T_a = –40°C to +85°C (product with wide-range temperature specifications), T_a = +75°C (bare die product)

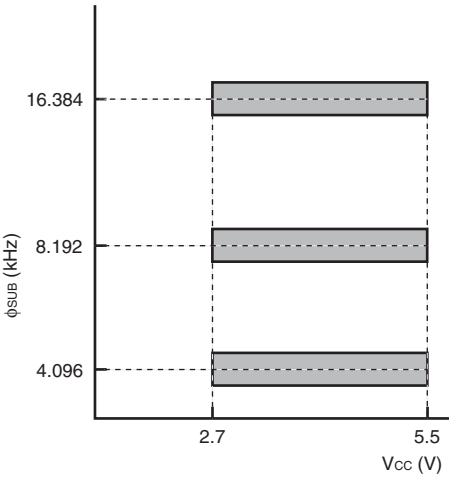
				Values				
Item	**Symbol**	**Applicable Pins**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**	**Notes**
Subactive mode current consumption	I_{SUB}	V_{CC}	V_{CC} = 2.7 V, LCD on, 32-kHz crystal resonator used ($\phi_{SUB} = \phi_W/2$)	—	15.0	30.0	µA	*3 *4
			V_{CC} = 2.7 V, LCD on, 32-kHz crystal resonator used ($\phi_{SUB} = \phi_W/8$)	—	8.0	—		*3 *4 Reference value
Subsleep mode current consumption	I_{SUBSP}	V_{CC}	V_{CC} = 2.7 V, LCD on, 32-kHz crystal resonator used ($\phi_{SUB} = \phi_W/2$)	—	7.5	16.0	µA	*3 *4
Watch mode current consumption	I_{WATCH}	V_{CC}	V_{CC} = 2.7 V, LCD not used, 32-kHz crystal resonator used	—	3.8	6.0	µA	*2 *3 *4
					2.8			*1 *3 *4
Standby mode current consumption	I_{STBY}	V_{CC}	32-kHz crystal resonator not used	—	1.0	5.0	µA	*3 *4
RAM data retaining voltage	V_{RAM}	V_{CC}		1.5	—	—	V	

Item	Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit	Notes
Input/ output leakage current	$\lvert I_{IL} \rvert$	$\overline{RES}$, P43, OSC1, X1, P31 to P37, P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80, IRQAEC, PA0 to PA3, P90 to P95	V_{IN} = 0.5 V to V_{CC} – 0.5 V	—	—	1.0	µA	
		PB0 to PB3	V_{IN} = 0.5 V to AV_{CC} – 0.5 V	—	—	1.0		
Pull-up MOS current	$-I_p$	P31 to P37, P50 to P57, P60 to P67	V_{CC} = 3.0 V, V_{IN} = 0.0 V	30	—	180	µA	
Input capacitance	C_{in}	All input pins except power supply pin	f = 1 MHz, V_{IN} = 0.0 V, T_a = 25°C	—	—	15.0	pF	
Active mode current consumption	I_{OPE1}	V_{CC}	Active (high-speed) mode V_{CC} = 1.8 V, f_{OSC} = 2 MHz	—	0.4	—	mA	*1*3*4 Approx. max. value = 1.1 × Typ.
			Active (high-speed) mode V_{CC} = 3 V, f_{OSC} = 2 MHz	—	0.6	—		*1*3*4 Approx. max. value = 1.1 × Typ.
				—	1.0	—		*2*3*4 Approx. max. value = 1.1 × Typ.
			Active (high-speed) mode V_{CC} = 3 V, f_{OSC} = 4 MHz	—	1.2	—		*1*3*4 Approx. max. value = 1.1 × Typ.
				—	1.6	2.8		*2*3*4 Condition B

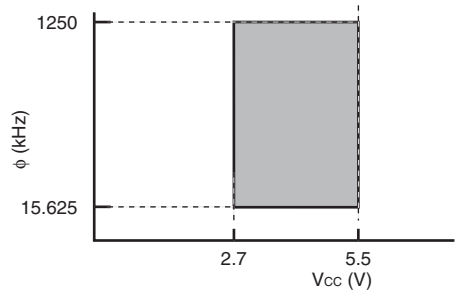
Power Supply Voltage and Operating Frequency Range (System Clock Oscillator Selected)



- Active (high-speed) mode
- Sleep (high-speed) mode (except CPU)



- Subactive mode
- Subsleep mode (except CPU)
- Watch mode (except CPU)



- Active (medium-speed) mode
- Sleep (medium-speed) mode (except A/D converter)

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	LCD Power Supply	Oscillator Pins
Active (high-speed) mode (I_{OPE1})	V_{CC}	Only CPU operates	V_{CC}	Stops	System clock: crystal resonator
Active (medium-speed) mode (I_{OPE2})					Subclock: Pin X1 = GND
Sleep mode	V_{CC}	Only all on-chip timers operate	V_{CC}	Stops	
Subactive mode	V_{CC}	Only CPU operates	V_{CC}	Stops	System clock: crystal resonator
Subsleep mode	V_{CC}	Only all on-chip timers operate CPU stops	V_{CC}	Stops	Subclock: crystal resonator
Watch mode	V_{CC}	Only clock time base operates CPU stops	V_{CC}	Stops	
Standby mode	V_{CC}	CPU and timers both stop	V_{CC}	Stops	System clock: crystal resonator Subclock: Pin X1 = GND

4. Except current which flows to the pull-up MOS or output buffer
5. Used when user mode or boot mode is determined after canceling a reset in the F-ZTAT version
6. Voltage maintained in standby mode

Table 17.23 Power Supply Voltage Detection Circuit Characteristics (2)

Using on-chip reference voltage and ladder resistor (VREFSEL = VINTDSEL = VINTUSEL = 0)

			Rated Values			
Item	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Power supply drop detection voltage	Vint(D)*3	LVDSEL = 0	3.3	3.7	4.2	V
Power supply rise detection voltage	Vint(U)*3	LVDSEL = 0	3.6	4.0	4.5	V
Reset detection voltage 1*1	Vreset1*3	LVDSEL = 0	2.0	2.3	2.7	V
Reset detection voltage 2*2	Vreset2*3	LVDSEL = 1	2.7	3.3	3.9	V

Notes: 1. The above function should be used in conjunction with the voltage drop/rise detection function.
2. Low-voltage detection reset should be selected for low-voltage detection reset 2 only.
3. The values of Vint(D), Vint(U), Vreset1, and Vreset2 change relative to each other.
Example: If Vint(D) is the minimum value, Vint(U), Vreset1, and Vreset2 are also the minimum values.

Table 17.24 Power Supply Voltage Detection Circuit Characteristics (3)

Using on-chip reference voltage and detect voltage external input (VREFSEL = 0, VINTDSEL and VINTUSEL = 1)

			Rated Values			
Item	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
extD/extU interrupt detection level	Vexd		0.80	1.20	1.60	V
extD/extU pin input voltage*2	VextD*1 VextU*1	V_{CC} = 2.7 to 3.3 V	–0.3	—	V_{CC} + 0.3 or AV_{CC} + 0.3, whichever is lower	V
		V_{CC} = 3.3 to 5.5 V	–0.3	—	3.6 or AV_{CC} + 0.3, whichever is lower	V

Notes: 1. The VextD voltage must always be greater than the VextU voltage.
2. The maximum input voltage of the extD and extU pins is 3.6 V.

Mnemonic		Operand Size	Addressing Modes/Instruction Length (bytes)								Operation	Condition Code					Number of Execution States
			#xx:8/16	Rn	@Rn	@(d:16, Rn)	@-Rn/@Rn+	@aa:8/16	@(d:8, PC)	@@aa	—	Branching Condition	I	H	N	Z	V	C	
BIOR	BIOR #xx:3, Rd	B		2								C∨(#xx:3 of Rd8)→C	—	—	—	—	—	↕	2
	BIOR #xx:3, @Rd	B			4							C∨(#xx:3 of @Rd16)→C	—	—	—	—	—	↕	6
	BIOR #xx:3, @aa:8	B						4				C∨(#xx:3 of @aa:8)→C	—	—	—	—	—	↕	6
BXOR	BXOR #xx:3, Rd	B		2								C ⊕ (#xx:3 of Rd8)→C	—	—	—	—	—	↕	2
	BXOR #xx:3, @Rd	B			4							C ⊕ (#xx:3 of @Rd16)→C	—	—	—	—	—	↕	6
	BXOR #xx:3, @aa:8	B						4				C ⊕ (#xx:3 of @aa:8)→C	—	—	—	—	—	↕	6
BIXOR	BIXOR #xx:3, Rd	B		2								C ⊕ (#xx:3 of Rd8)→C	—	—	—	—	—	↕	2
	BIXOR #xx:3, @Rd	B			4							C ⊕ (#xx:3 of @Rd16)→C	—	—	—	—	—	↕	6
	BIXOR #xx:3, @aa:8	B						4				C ⊕ (#xx:3 of @aa:8)→C	—	—	—	—	—	↕	6
Bcc	BRA d:8 (BT d:8)	—							2			PC←PC+d:8	—	—	—	—	—	—	4
	BRN d:8 (BF d:8)	—							2			PC←PC+2	—	—	—	—	—	—	4
	BHI d:8	—							2			If condition	—	—	—	—	—	—	4
	BLS d:8	—							2			is true then	—	—	—	—	—	—	4
	BCC d:8 (BHS d:8)	—							2			PC←PC+d:8	—	—	—	—	—	—	4
	BCS d:8 (BLO d:8)	—							2			else next;	—	—	—	—	—	—	4
	BNE d:8	—							2				—	—	—	—	—	—	4
	BEQ d:8	—							2				—	—	—	—	—	—	4
	BVC d:8	—							2				—	—	—	—	—	—	4
	BVS d:8	—							2				—	—	—	—	—	—	4
	BPL d:8	—							2				—	—	—	—	—	—	4
	BMI d:8	—							2				—	—	—	—	—	—	4
	BGE d:8	—							2				—	—	—	—	—	—	4
	BLT d:8	—							2				—	—	—	—	—	—	4
	BGT d:8	—							2				—	—	—	—	—	—	4
	BLE d:8	—							2				—	—	—	—	—	—	4

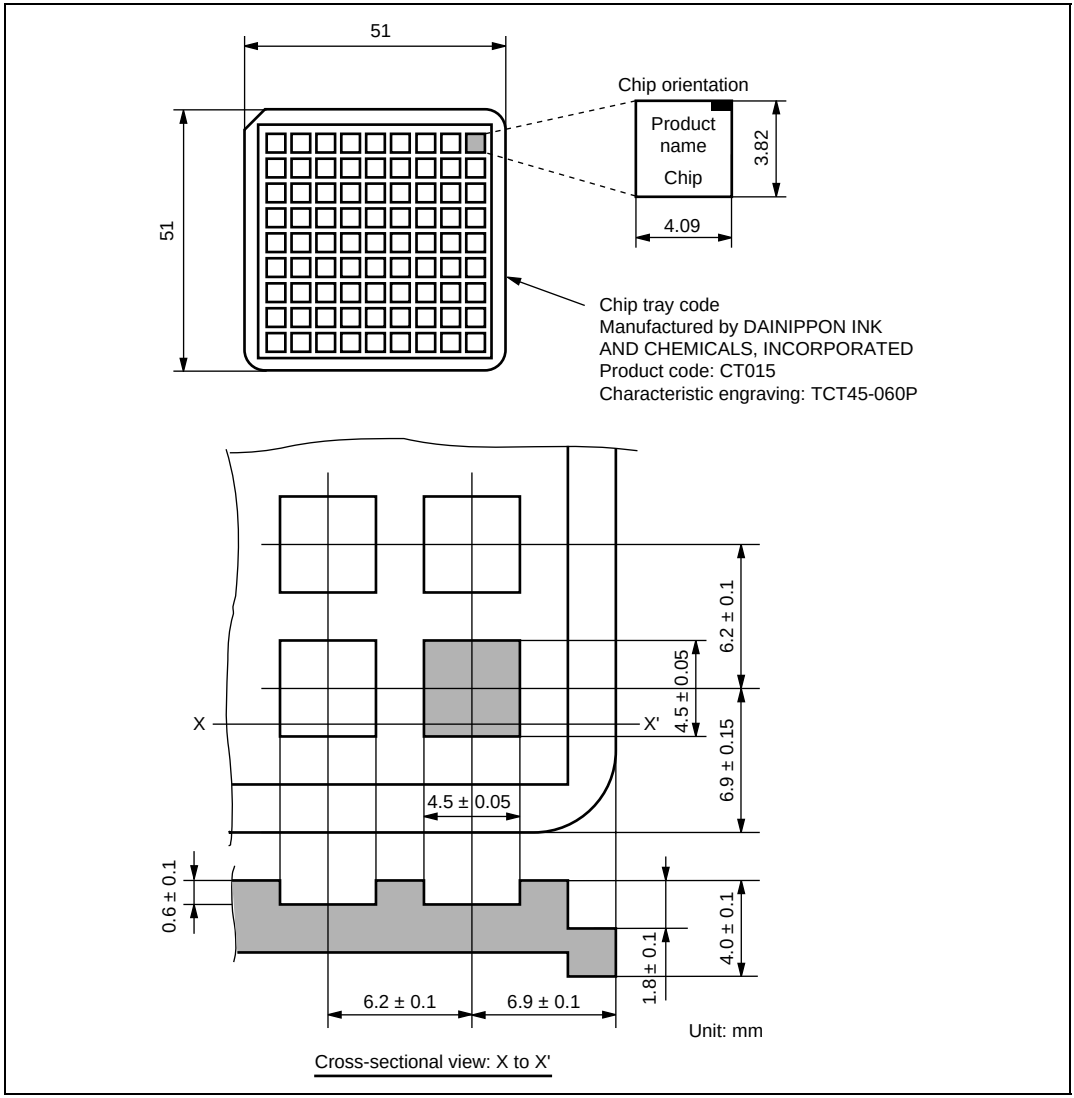


Figure H.3 Chip Tray Specifications (HCD64F38004 and HCD64F38002)