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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	4MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	4KB (2K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90ls4433-4ac

Clock Options

Crystal Oscillator

XTAL1 and XTAL2 are input and output, respectively, of an inverting amplifier, which can be configured for use as an On-chip Oscillator, as shown in Figure 2 and Figure 3. Either a quartz crystal or a ceramic resonator may be used.

External Clock

If the Oscillator is to be used as a clock for an external device, the clock signal from XTAL2 may be routed to one HC buffer while reducing the load capacitor by 5 pF, as shown in Figure 3. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 4.

Figure 2. Oscillator Connections

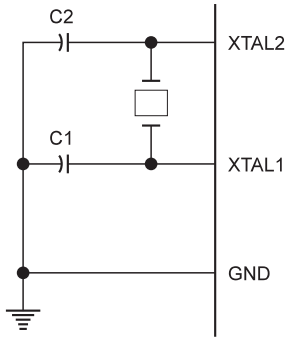


Figure 3. Using MCU Oscillator as a Clock for an External Device

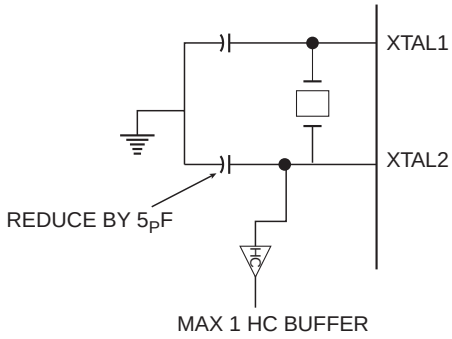
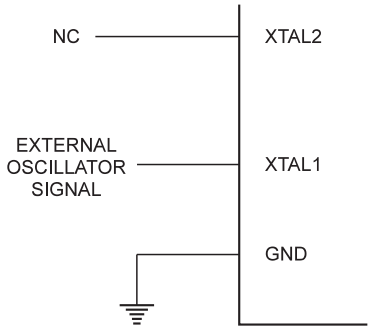


Figure 4. External Clock Drive Configuration



Architectural Overview

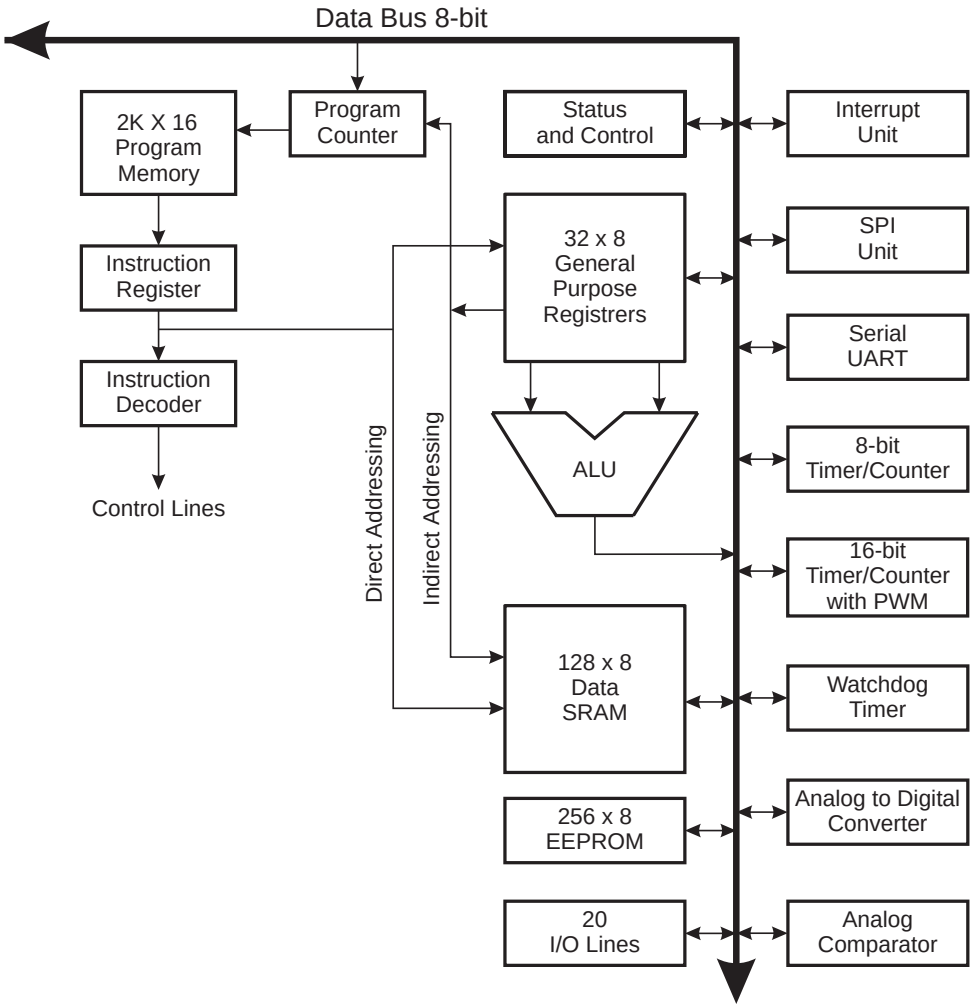
The fast-access Register File concept contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one Arithmetic Logic Unit (ALU) operation is executed. Two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File – in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing, enabling efficient address calculations. One of the three address pointers is also used as the address pointer for the constant table look-up function. These added function registers are the 16-bit X-, Y-, and Z-register.

The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 5 shows the AT90S4433 AVR RISC microcontroller architecture.

In addition to the register operation, the conventional Memory Addressing modes can be used on the Register File as well. This is enabled by the fact that the Register File is assigned the 32 lowermost Data Space addresses ($00 - $1F), allowing them to be accessed as though they were ordinary memory locations.

Figure 5. The AT90S4433 AVR RISC Architecture



The direct addressing reaches the entire data space. The Indirect with Displacement mode features 63 address locations reached from the base address given by the Y- or Z-register.

When using register indirect addressing modes with automatic pre-decrement and post-increment, the address registers X, Y, and Z are decremented and incremented.

The 32 general purpose working registers, 64 I/O Registers and the 128 bytes of internal data SRAM in the AT90S4433 are all accessible through all these addressing modes.

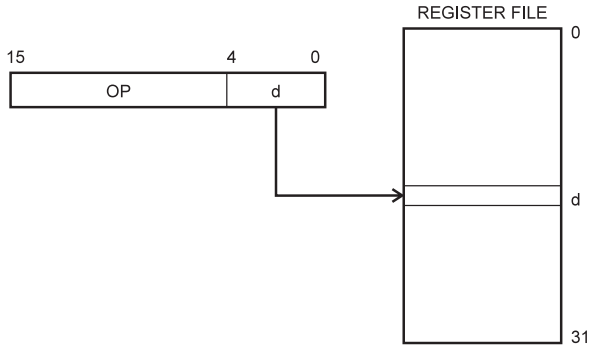
See the next section for a detailed description of the different addressing modes.

Program and Data Addressing Modes

The AT90S4433 AVR RISC microcontroller supports powerful and efficient addressing modes for access to the Flash Program memory, SRAM, Register File, and I/O data memory. This section describes the different addressing modes supported by the AVR architecture. In the figures, OP means the operation code part of the instruction word. To simplify, not all figures show the exact location of the addressing bits.

Register Direct, Single Register Rd

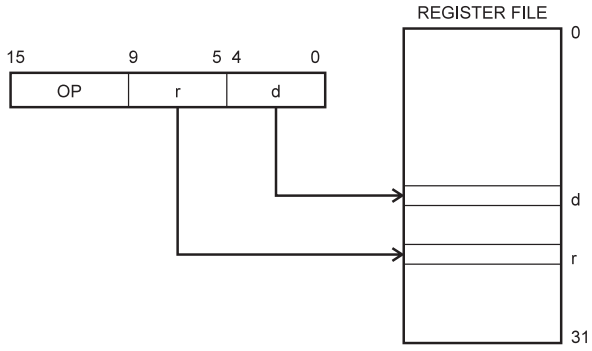
Figure 10. Direct Single Register Addressing



The operand is contained in register d (Rd).

Register Direct, Two Registers Rd and Rr

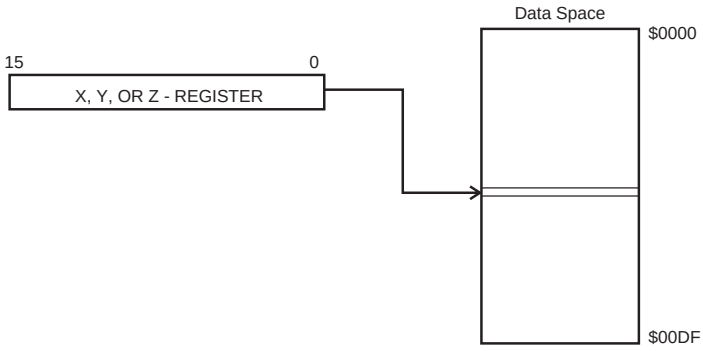
Figure 11. Direct Register Addressing, Two Registers



Operands are contained in registers r (Rr) and d (Rd). The result is stored in register d (Rd).

Data Indirect

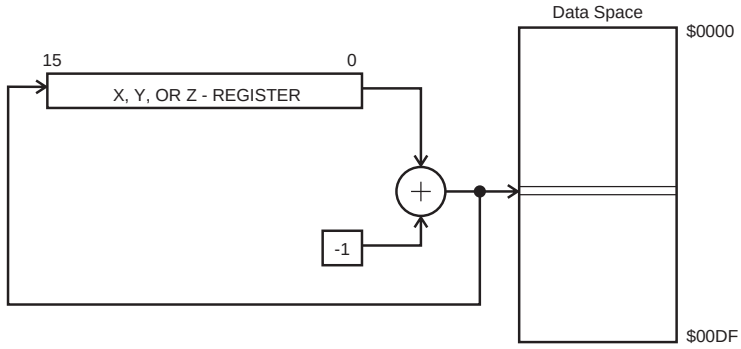
Figure 15. Data Indirect Addressing



Operand address is the contents of the X-, Y-, or the Z-register.

Data Indirect with Pre-decrement

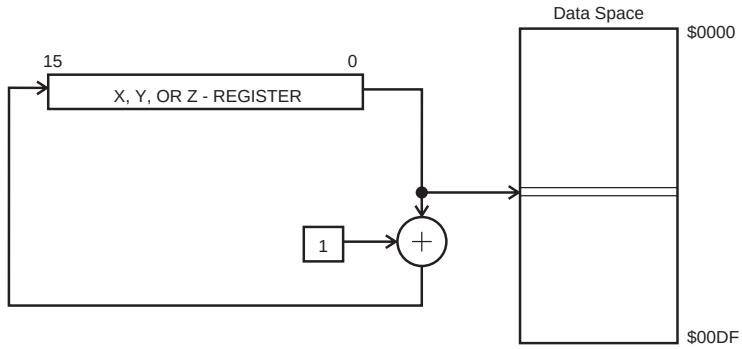
Figure 16. Data Indirect Addressing with Pre-decrement



The X-, Y-, or the Z-register is decremented before the operation. Operand address is the decremented contents of the X-, Y-, or the Z-register.

Data Indirect with Post-increment

Figure 17. Data Indirect Addressing with Post-increment



The X-, Y-, or the Z-register is incremented after the operation. Operand address is the content of the X-, Y-, or the Z-register prior to incrementing.

Stack Pointer – SP

The AT90S4433 Stack Pointer is implemented as an 8-bit register in the I/O space location $3D ($5D). As the AT90S4433 data memory has $0DF locations, eight bits are used.

	7	6	5	4	3	2	1	0	
$3D ($5D)	**SP7**	**SP6**	**SP5**	**SP4**	**SP3**	**SP2**	**SP1**	**SP0**	**SP**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The Stack Pointer points to the data SRAM stack area where the Subroutine and Interrupt stacks are located. This stack space in the data SRAM must be defined by the program before any subroutine calls are executed or interrupts are enabled. The Stack Pointer must be set to point above $60. The Stack Pointer is decremented by one when data is pushed onto the stack with the PUSH instruction, and it is decremented by two when an address is pushed onto the Stack with subroutine calls and interrupts. The Stack Pointer is incremented by one when data is popped from the stack with the POP instruction, and it is incremented by two when an address is popped from the Stack with return from subroutine RET or return from interrupt RETI.

Reset and Interrupt Handling

The AT90S4433 provides 13 different interrupt sources. These interrupts and the separate reset vector each have a separate Program Vector in the Program memory space. All interrupts are assigned individual enable bits, which must be set (one) together with the I-bit in the Status Register in order to enable the interrupt.

The lowest addresses in the Program memory space are automatically defined as the Reset and Interrupt Vectors. The complete list of Vectors is shown in Table 3. The list also determines the priority levels of the different interrupts. The lower the address, the higher the priority level. RESET has the highest priority, and next is INT0 (the External Interrupt Request 0), etc.

Table 3. Reset and Interrupt Vectors

Vector No.	Program Address	Source	Interrupt Definition
1	$000	RESET	External Pin, Power-on Reset, Brown-out Reset and Watchdog Reset
2	$001	INT0	External Interrupt Request 0
3	$002	INT1	External Interrupt Request 1
4	$003	TIMER1 CAPT	Timer/Counter1 Capture Event
5	$004	TIMER1 COMP	Timer/Counter1 Compare Match
6	$005	TIMER1 OVF	Timer/Counter1 Overflow
7	$006	TIMER0 OVF	Timer/Counter0 Overflow
8	$007	SPI, STC	Serial Transfer Complete
9	$008	UART, RX	UART, Rx Complete
10	$009	UART, UDRE	UART Data Register Empty
11	$00A	UART, TX	UART, Tx Complete
12	$00B	ADC	ADC Conversion Complete
13	$00C	EE_RDY	EEPROM Ready
14	$00D	ANA_COMP	Analog Comparator

Figure 25. MCU Start-up, $\overline{\text{RESET}}$ Tied to V_{CC}

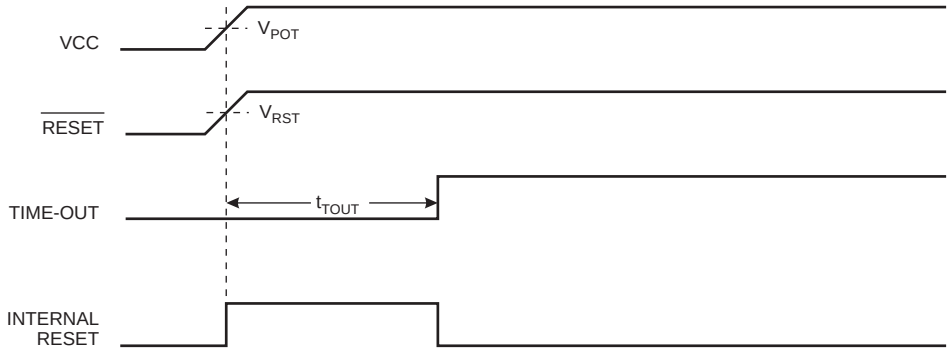
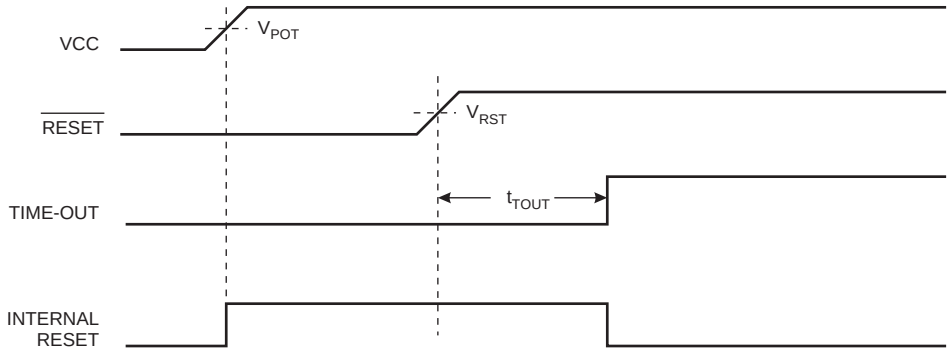


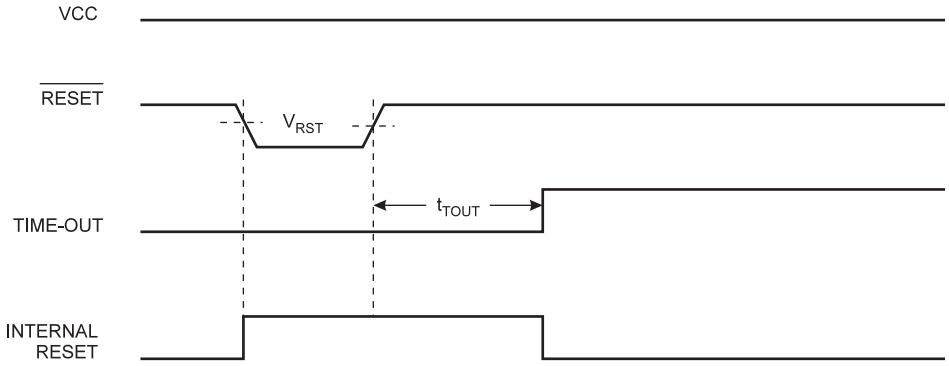
Figure 26. MCU Start-up, $\overline{\text{RESET}}$ Controlled Externally



External Reset

An External Reset is generated by a low level on the $\overline{\text{RESET}}$ pin. Reset pulses longer than 50 ns will generate a Reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a Reset. When the applied signal reaches the Reset Threshold Voltage (V_{RST}) on its positive edge, the delay timer starts the MCU after the Time-out period (t_{TOUT}) has expired.

Figure 27. External Reset during Operation



- **Bit 6 – INTF0: External Interrupt Flag0**

When an edge on the INT0 pin triggers an interrupt request, the corresponding Interrupt Flag, INTF0 becomes set (one). If the I-bit in SREG and the corresponding interrupt enable bit, INT0 in GIMSK is set (one), the MCU will jump to the Interrupt Vector. The flag is always cleared when the interrupt routine is executed. Alternatively, the flag is cleared by writing a logical “1” to it. This flag is always cleared when INT0 is configured as level interrupt.

- **Bits 5..0 – Res: Reserved Bits**

These bits are reserved bits in the AT90S4433 and always read as zero.

Timer/Counter Interrupt Mask Register – TIMSK

Bit	7	6	5	4	3	2	1	0	
$39 ($59)	TOIE1	OCIE1	–	–	TICIE1	–	TOIE0	–	TIMSK
Read/Write	R/W	R/W	R	R	R/W	R	R/W	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – TOIE1: Timer/Counter1 Overflow Interrupt Enable**

When the TOIE1 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 Overflow Interrupt is enabled. The corresponding interrupt (at vector $005) is executed if an overflow in Timer/Counter1 occurs, i.e., when the TOV1 bit is set in the Timer/Counter Interrupt Flag Register (TIFR).

- **Bit 6 – OCIE1: Timer/Counter1 Output Compare Match Interrupt Enable**

When the OCIE1 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 Compare Match Interrupt is enabled. The corresponding interrupt (at vector $004) is executed if a compare match in Timer/Counter1 occurs, i.e., when the OCF1 bit is set in the Timer/Counter Interrupt Flag Register (TIFR).

- **Bits 5, 4 – Res: Reserved Bits**

These bits are reserved bits in the AT90S4433 and always read as zero.

- **Bit 3 – TICIE1: Timer/Counter1 Input Capture Interrupt Enable**

When the TICIE1 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 Input Capture Event Interrupt is enabled. The corresponding interrupt (at vector $003) is executed if a capture-triggering event occurs on pin 14, PB0 (ICP), i.e., when the ICF1 bit is set in the Timer/Counter Interrupt Flag Register (TIFR).

- **Bit 2 – Res: Reserved Bit**

This bit is a reserved bit in the AT90S4433 and always reads as zero.

- **Bit 1 – TOIE0: Timer/Counter0 Overflow Interrupt Enable**

When the TOIE0 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter0 Overflow Interrupt is enabled. The corresponding interrupt (at vector $006) is executed if an overflow in Timer/Counter0 occurs, i.e., when the TOV0 bit is set in the Timer/Counter Interrupt Flag Register (TIFR).

- **Bit 0 – Res: Reserved Bit**

This bit is a reserved bit in the AT90S4433 and always reads as zero.

SPI Status Register – SPSR

Bit	7	6	5	4	3	2	1	0	
$0E ($2E)	**SPIF**	**WCOL**	–	–	–	–	–	–	**SPSR**
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – SPIF: SPI Interrupt Flag**

When a serial transfer is complete, the SPIF bit is set (one) and an interrupt is generated if SPIE in SPCR is set (one) and global interrupts are enabled. If $\overline{SS}$ is an input and is driven low when the SPI is in Master mode, this will also set the SPIF Flag. SPIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, the SPIF bit is cleared by first reading the SPI Status Register with SPIF set (one), then by accessing the SPI Data Register (SPDR).

- **Bit 6 – WCOL: Write Collision Flag**

The WCOL bit is set if the SPI Data Register (SPDR) is written during a data transfer. The WCOL bit (and the SPIF bit) are cleared (zero) by first reading the SPI Status Register with WCOL set (one), and then by accessing the SPI Data Register.

- **Bits 5..0 – Res: Reserved Bits**

These bits are reserved bits in the AT90S4433 and will always read as zero.

The SPI interface on the AT90S4433 is also used for Program memory and EEPROM downloading or uploading. See page 93 for Serial Programming and verification.

SPI Data Register – SPDR

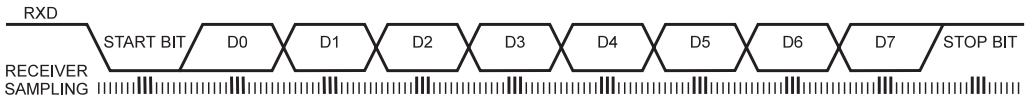
Bit	7	6	5	4	3	2	1	0	
$0F ($2F)	**MSB**							**LSB**	**SPDR**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	X	X	X	X	X	X	X	X	Undefined

The SPI Data Register is a read/write register used for data transfer between the Register File and the SPI Shift Register. Writing to the register initiates data transmission. Reading the register causes the Shift Register Receive buffer to be read.

The Receiver front-end logic samples the signal on the RXD pin at a frequency 16 times the baud rate. While the line is idle, one single sample of logical “0” will be interpreted as the falling edge of a start bit, and the start bit detection sequence is initiated. Let sample 1 denote the first zero-sample. Following the 1-to-0 transition, the Receiver samples the RXD pin at samples 8, 9, and 10. If two or more of these three samples are found to be logical “1”s, the start bit is rejected as a noise spike and the receiver starts looking for the next 1-to-0 transition.

If, however, a valid start bit is detected, sampling of the data bits following the start bit is performed. These bits are also sampled at samples 8, 9, and 10. The logical value found in at least two of the three samples is taken as the bit value. All bits are shifted into the transmitter Shift Register as they are sampled. Sampling of an incoming character is shown in Figure 42.

Figure 42. Sampling Received Data



When the stop bit enters the receiver, the majority of the three samples must be one to accept the stop bit. If two or more samples are logical “0”s, the Framing Error (FE) Flag in the UART Control and Status Register A (UCSRA) is set. Before reading the UDR Register, the user should always check the FE bit to detect Framing Errors.

Whether or not a valid stop bit is detected at the end of a character reception cycle, the data is transferred to UDR and the RXC Flag in UCSRA is set. UDR is, in fact, two physically separate registers: one for Transmitted Data and one for Received Data. When UDR is read, the Receive Data Register is accessed, and when UDR is written, the Transmit Data Register is accessed. If 9-bit data word is selected (the CHR9 bit in the UART Control and Status Register B, UCSRB is set), the RXB8 bit in UCSRB is loaded with bit nine in the Transmit Shift Register when data is transferred to UDR.

If, after having received a character, the UDR Register has not been read since the last receive, the OverRun (OR) Flag in UCSRB is set. This means that the last data byte shifted into the Shift Register could not be transferred to UDR and has been lost. The OR bit is buffered and is updated when the valid data byte in UDR is read. Thus, the user should always check the OR bit after reading the UDR Register in order to detect any overruns if the baud rate is high or CPU load is high.

When the RXEN bit in the UCSRB Register is cleared (zero), the receiver is disabled. This means that the PD0 pin can be used as a general I/O pin. When RXEN is set, the UART receiver will be connected to PD0, which is forced to be an input pin regardless of the setting of the DDD0 bit in DDRD. When PD0 is forced to input by the UART, the PORTD0 bit can still be used to control the pull-up resistor on the pin.

When the CHR9 bit in the UCSRB Register is set, transmitted and received characters are nine bits long, plus start and stop bits. The ninth data bit to be transmitted is the TXB8 bit in UCSRB Register. This bit must be set to the wanted value before a transmission is initiated by writing to the UDR Register. The ninth data bit received is the RXB8 bit in the UCSRB Register.

Table 19. UBR Settings at Various Crystal Frequencies

Baud Rate	1 MHz		%Error	1.8432 MHz		%Error	2 MHz		%Error	2.4576 MHz		%Error
2400	UBR=	**25**	**0.2**	UBR=	**47**	**0.0**	UBR=	**51**	**0.2**	UBR=	**63**	**0.0**
4800	UBR=	**12**	**0.2**	UBR=	**23**	**0.0**	UBR=	**25**	**0.2**	UBR=	**31**	**0.0**
9600	UBR=	6	7.5	UBR=	**11**	**0.0**	UBR=	**12**	**0.2**	UBR=	**15**	**0.0**
14400	UBR=	3	7.8	UBR=	**7**	**0.0**	UBR=	8	3.7	UBR=	10	3.1
19200	UBR=	2	7.8	UBR=	**5**	**0.0**	UBR=	6	7.5	UBR=	**7**	**0.0**
28800	UBR=	1	7.8	UBR=	**3**	**0.0**	UBR=	3	7.8	UBR=	4	6.3
38400	UBR=	1	22.9	UBR=	**2**	**0.0**	UBR=	2	7.8	UBR=	**3**	**0.0**
57600	UBR=	0	7.8	UBR=	**1**	**0.0**	UBR=	1	7.8	UBR=	2	12.5
76800	UBR=	0	22.9	UBR=	1	33.3	UBR=	1	22.9	UBR=	**1**	**0.0**
115200	UBR=	0	84.3	UBR=	**0**	**0.0**	UBR=	0	7.8	UBR=	0	25.0

Baud Rate	3.2768 MHz		%Error	3.6864 MHz		%Error	4 MHz		%Error	4.608 MHz		%Error
2400	UBR=	**84**	**0.4**	UBR=	**95**	**0.0**	UBR=	**103**	**0.2**	UBR=	**119**	**0.0**
4800	UBR=	**42**	**0.8**	UBR=	**47**	**0.0**	UBR=	**51**	**0.2**	UBR=	**59**	**0.0**
9600	UBR=	**20**	**1.6**	UBR=	**23**	**0.0**	UBR=	**25**	**0.2**	UBR=	**29**	**0.0**
14400	UBR=	**13**	**1.6**	UBR=	**15**	**0.0**	UBR=	16	2.1	UBR=	**19**	**0.0**
19200	UBR=	10	3.1	UBR=	**11**	**0.0**	UBR=	**12**	**0.2**	UBR=	**14**	**0.0**
28800	UBR=	**6**	**1.6**	UBR=	**7**	**0.0**	UBR=	8	3.7	UBR=	**9**	**0.0**
38400	UBR=	4	6.3	UBR=	**5**	**0.0**	UBR=	6	7.5	UBR=	7	6.7
57600	UBR=	3	12.5	UBR=	**3**	**0.0**	UBR=	3	7.8	UBR=	**4**	**0.0**
76800	UBR=	2	12.5	UBR=	**2**	**0.0**	UBR=	2	7.8	UBR=	3	6.7
115200	UBR=	1	12.5	UBR=	**1**	**0.0**	UBR=	1	7.8	UBR=	2	20.0

Baud Rate	7.3728 MHz		%Error	8 MHz		%Error	9.216 MHz		%Error	11.059 MHz		%Error
2400	UBR=	**191**	**0.0**	UBR=	**207**	**0.2**	UBR=	**239**	**0.0**	UBR=	287	-
4800	UBR=	**95**	**0.0**	UBR=	**103**	**0.2**	UBR=	**119**	**0.0**	UBR=	**143**	**0.0**
9600	UBR=	**47**	**0.0**	UBR=	**51**	**0.2**	UBR=	**59**	**0.0**	UBR=	**71**	**0.0**
14400	UBR=	**31**	**0.0**	UBR=	**34**	**0.8**	UBR=	**39**	**0.0**	UBR=	**47**	**0.0**
19200	UBR=	**23**	**0.0**	UBR=	**25**	**0.2**	UBR=	**29**	**0.0**	UBR=	**35**	**0.0**
28800	UBR=	**15**	**0.0**	UBR=	16	2.1	UBR=	**19**	**0.0**	UBR=	**23**	**0.0**
38400	UBR=	**11**	**0.0**	UBR=	**12**	**0.2**	UBR=	**14**	**0.0**	UBR=	**17**	**0.0**
57600	UBR=	**7**	**0.0**	UBR=	8	3.7	UBR=	**9**	**0.0**	UBR=	**11**	**0.0**
76800	UBR=	**5**	**0.0**	UBR=	6	7.5	UBR=	7	6.7	UBR=	**8**	**0.0**
115200	UBR=	**3**	**0.0**	UBR=	3	7.8	UBR=	**4**	**0.0**	UBR=	**5**	**0.0**

keeps running for as long as the ADEN bit is set and is continuously reset when ADEN is low.

When initiating a conversion by setting the ADSC bit in ADCSR, the conversion starts at the following rising edge of the ADC clock cycle. The actual sample-and-hold takes place 1.5 ADC clock cycles after the start of the conversion. The result is ready and written to the ADC Result Register after 13 cycles. In Single Conversion mode, the ADC needs one more clock cycle before a new conversion can be started (see Figure 47). If ADSC is set high in this period, the ADC will start the new conversion immediately. In Free Run mode, a new conversion will be started immediately after the result is written to the ADC Result Register. Using Free Run mode and an ADC clock frequency of 200 kHz gives the lowest conversion time, 65 µs, equivalent to 15.4 kSPS. For a summary of conversion times, see Table 21.

Figure 46. ADC Timing Diagram, First Conversion (Single Conversion Mode)

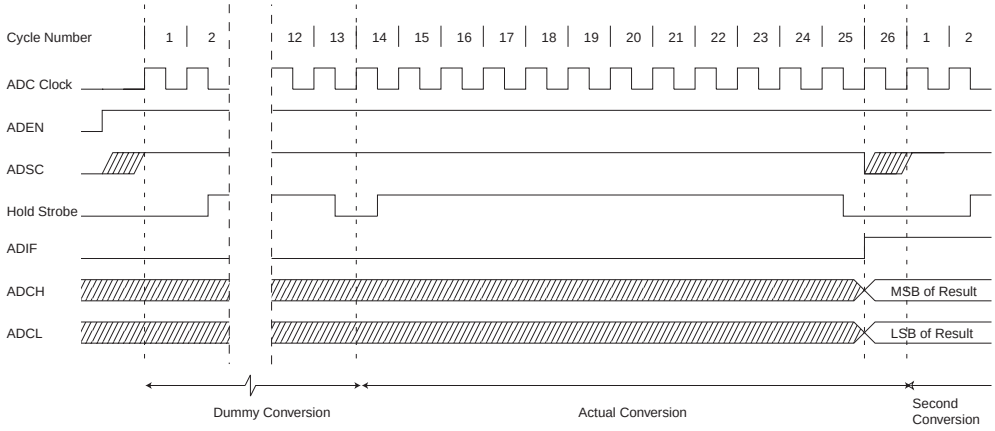


Table 21. ADC Conversion Time

Condition	Sample Cycle Number	Result Ready(Cycle Number)	Total Conversion Time (Cycles)	Total Conversion Time (µs)
1st Conversion, Free Run	13.5	25	25	125 - 500
1st Conversion, Single	13.5	25	26	130 - 520
Free Run Conversion	1.5	13	13	65 - 260
Single Conversion	1.5	13	14	70 - 280

I/O Ports

All AVR ports have true Read-Modify-Write functionality when used as general digital I/O ports. This means that the direction of one port pin can be changed without unintentionally changing the direction of any other pin with the SBI and CBI instructions. The same applies for changing drive value (if configured as output) or enabling/disabling of pull-up resistors (if configured as input).

Port B

Port B is a 6-bit bi-directional I/O port.

Three I/O memory address locations are allocated for the Port B, one each for the Data Register – PORTB, $18($38), Data Direction Register – DDRB, $17($37), and the Port B Input Pins – PINB, $16($36). The Port B Input Pins address is read only, while the Data Register and the Data Direction Register are read/write.

All port pins have individually selectable pull-up resistors. The Port B output buffers can sink 20 mA and thus drive LED displays directly. When pins PB0 to PB7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

The Port B pins with alternate functions are shown in Table 23.

Table 23. Port B Pin Alternate Functions

Port Pin	Alternate Functions
PB0	ICP (Timer/Counter1 Input Capture Pin)
PB1	OC1 (Timer/Counter1 Output Compare Match Output)
PB2	$\overline{SS}$ (SPI Slave Select Input)
PB3	MOSI (SPI Bus Master Output/Slave Input)
PB4	MISO (SPI Bus Master Input/Slave Output)
PB5	SCK (SPI Bus Serial Clock)

When the pins are used for the alternate function, the DDRB and PORTB Registers have to be set according to the alternate function description.

Port B Data Register – PORTB

Bit	7	6	5	4	3	2	1	0	
$18 ($38)	–	–	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	PORTB
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port B Data Direction Register – DDRB

Bit	7	6	5	4	3	2	1	0	
$17 ($37)	–	–	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port B Input Pins Address – PINB

Bit	7	6	5	4	3	2	1	0	
$16 ($36)	–	–	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	PINB
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	0	0	N/A	N/A	N/A	N/A	N/A	N/A	

Port C Data Register – PORTC

Bit	7	6	5	4	3	2	1	0	
$15 ($35)	–	–	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	PORTC
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port C Data Direction Register – DDRC

Bit	7	6	5	4	3	2	1	0	
$14 ($34)	–	–	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port C Input Pins Address – PINC

Bit	7	6	5	4	3	2	1	0	
$13 ($33)	–	–	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	PINC
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	0	0	N/A	N/A	N/A	N/A	N/A	N/A	

The Port C Input Pins address (PINC) is not a register; this address enables access to the physical value on each Port C pin. When reading PORTC, the Port C Data Latch is read, and when reading PINC, the logical values present on the pins are read.

Port C as General Digital I/O

All six pins in Port C have equal functionality when used as digital I/O pins.

PCn, general I/O pin: The DDCn bit in the DDRC Register selects the direction of this pin. If DDCn is set (one), PCn is configured as an output pin. If DDCn is cleared (zero), PCn is configured as an input pin. If PORTCn is set (one) when the pin is configured as an input pin, the MOS pull-up resistor is activated. To switch the pull-up resistor off, PORTCn has to be cleared (zero) or the pin has to be configured as an output pin.The port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Table 25. DDCn Effects on Port C Pins[1]

DDCn	PORTCn	I/O	Pull-up	Comment
0	0	Input	No	Tri-state (high-Z)
0	1	Input	Yes	PCn will source current if ext. pulled low.
1	0	Output	No	Push-pull Zero Output
1	1	Output	No	Push-pull One Output

Note: 1. n: 5..0, pin number

Port D as General Digital I/O

PDn, General I/O pin: The DDDn bit in the DDRD Register selects the direction of this pin. If DDDn is set (one), PDn is configured as an output pin. If DDDn is cleared (zero), PDn is configured as an input pin. If PDn is set (one) when configured as an input pin, the MOS pull-up resistor is activated. To switch the pull-up resistor off, the PDn has to be cleared (zero) or the pin has to be configured as an output pin.The port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Table 27. DDDn Bits on Port D Pins(1)

DDDn	PORTDn	I/O	Pull-up	Comment
0	0	Input	No	Tri-state (high-Z)
0	1	Input	Yes	PDn will source current if ext. pulled low.
1	0	Output	No	Push-pull Zero Output
1	1	Output	No	Push-pull One Output

Note: 1. n: 7,6..0, pin number.

Alternate Functions of Port D

- **AIN1 – Port D, Bit 7**

AIN1, Analog Comparator Negative Input. When configured as an input (DDD7 is cleared [zero]), and with the internal MOS pull-up resistor switched off (PD7 is cleared [zero]), this pin also serves as the negative input of the On-chip Analog Comparator. During Power-down mode, the Schmitt trigger of the digital input is disconnected. This allows analog signals, which are close to $V_{CC}/2$, to be present during Power-down without causing excessive power consumption.

- **AIN0 – Port D, Bit 6**

AIN0, Analog Comparator Positive Input. When configured as an input (DDD6 is cleared [zero]), and with the internal MOS pull-up resistor switched off (PD6 is cleared [zero]), this pin also serves as the positive input of the On-chip Analog Comparator. During Power-down mode, the Schmitt trigger of the digital input is disconnected. This allows analog signals, which are close to $V_{CC}/2$, to be present during Power-down without causing excessive power consumption.

- **T1 – Port D, Bit 5**

T1, Timer/Counter1 Counter Source. See the Timer description for further details

- **T0 – Port D, Bit 4**

T0: Timer/Counter0 Counter Source. See the Timer description for further details.

- **INT1 – Port D, Bit 3**

INT1, External Interrupt Source 1: The PD3 pin can serve as an external interrupt source to the MCU. See the interrupt description for further details and how to enable the source.

- **INT0 – Port D, Bit 2**

INT0, External Interrupt Source 0: The PD2 pin can serve as an external interrupt source to the MCU. See the interrupt description for further details and how to enable the source.

Chip Erase

The Chip Erase command will erase the Flash and EEPROM memories and the Lock bits. The Lock bits are not reset until the Flash and EEPROM have been completely erased. The Fuse bits are not changed. Chip Erase must be performed before the Flash or EEPROM is reprogrammed.

A: Load Command “Chip Erase”

1. Set XA1, XA0 to “10”. This enables command loading.
2. Set BS to “0”.
3. Set DATA to “1000 0000”. This is the command for Chip Erase.
4. Give XTAL1 a positive pulse. This loads the command.
5. Give $\overline{WR}$ a t_{WLWH_CE} wide negative pulse to execute Chip Erase. See Table 33 for t_{WLWH_CE} value. Chip Erase does not generate any activity on the RDY/$\overline{BSY}$ pin.

Programming the Flash

A: Load Command “Write Flash”

1. Set XA1, XA0 to “10”. This enables command loading.
2. Set BS to “0”.
3. Set DATA to “0001 0000”. This is the command for Write Flash.
4. Give XTAL1 a positive pulse. This loads the command.

B: Load Address High Byte

1. Set XA1, XA0 to “00”. This enables address loading.
2. Set BS to “1”. This selects High Byte.
3. Set DATA = Address High Byte ($00 - $07).
4. Give XTAL1 a positive pulse. This loads the address High Byte.

C: Load Address Low Byte

1. Set XA1, XA0 to “00”. This enables address loading.
2. Set BS to “0”. This selects Low Byte.
3. Set DATA = Address Low Byte ($00 - $FF).
4. Give XTAL1 a positive pulse. This loads the address Low Byte.

D: Load Data Low Byte

1. Set XA1, XA0 to “01”. This enables data loading.
2. Set DATA = Data Low Byte ($00 - $FF).
3. Give XTAL1 a positive pulse. This loads the data Low Byte.

E: Write Data Low Byte

1. Set BS to “0”. This selects low data.
2. Give $\overline{WR}$ a negative pulse. This starts programming of the data byte. RDY/$\overline{BSY}$ goes low.
3. Wait until RDY/$\overline{BSY}$ goes high to program the next byte.

(See Figure 63 for signal waveforms.)

F: Load Data High Byte

1. Set XA1, XA0 to “01”. This enables data loading.
2. Set DATA = Data High Byte ($00 - $FF).
3. Give XTAL1 a positive pulse. This loads the data High Byte.

Typical Characteristics

The following charts show typical behavior. These figures are not tested during manufacturing. All current consumption measurements are performed with all I/O pins configured as inputs and with internal pull-ups enabled. A sine wave generator with rail-to-rail output is used as clock source.

The power consumption in Power-down mode is independent of clock selection.

The current consumption is a function of several factors, such as: operating voltage, operating frequency, loading of I/O pins, switching rate of I/O pins, code executed and ambient temperature. The dominating factors are operating voltage and frequency.

The current drawn from capacitive loaded pins may be estimated (for one pin) as $C_L \bullet V_{CC} \bullet f$, where C_L = load capacitance, V_{CC} = operating voltage and f = average switching frequency of I/O pin.

The parts are characterized at frequencies higher than test limits. Parts are not guaranteed to function properly at frequencies higher than the ordering code indicates.

The difference between current consumption in Power-down mode with Watchdog Timer enabled and Power-down mode with Watchdog Timer disabled represents the differential current drawn by the Watchdog Timer.

The difference between Power-down mode with Brown-out Detector enabled and Power-down mode with Watchdog Timer disabled represents the differential current drawn by the Brown-out Detector.

Figure 70. Active Supply Current vs. Frequency

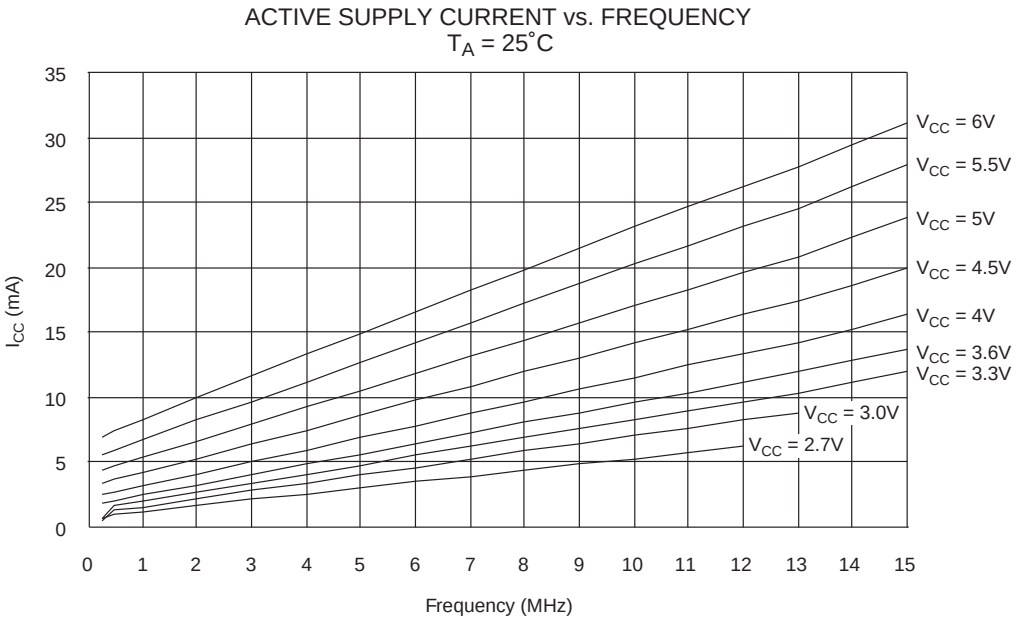


Figure 85. I/O Pin Source Current vs. Output Voltage

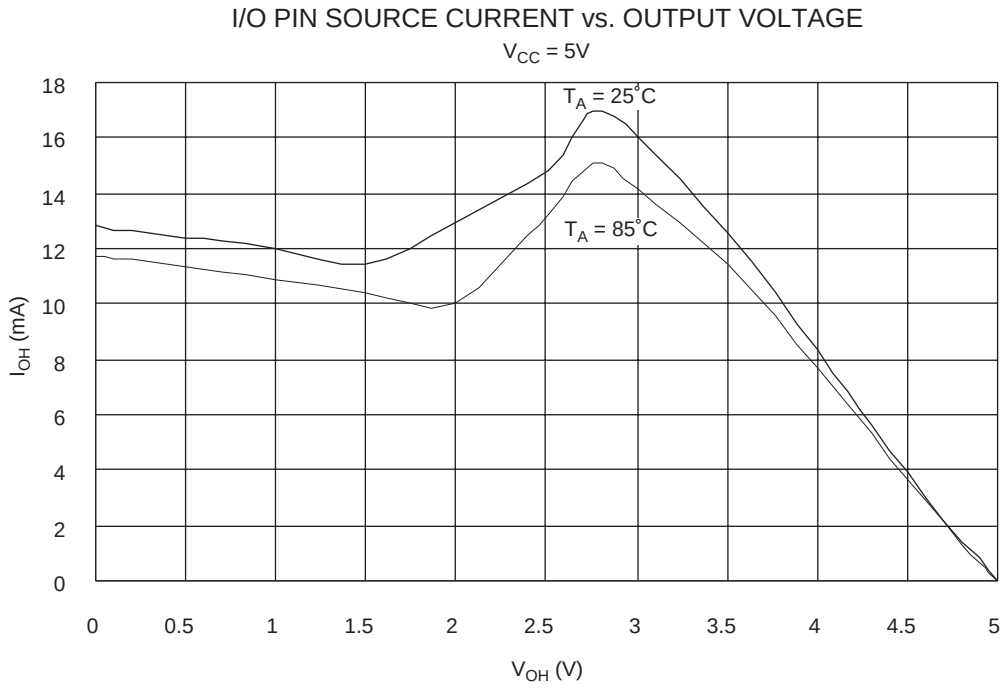
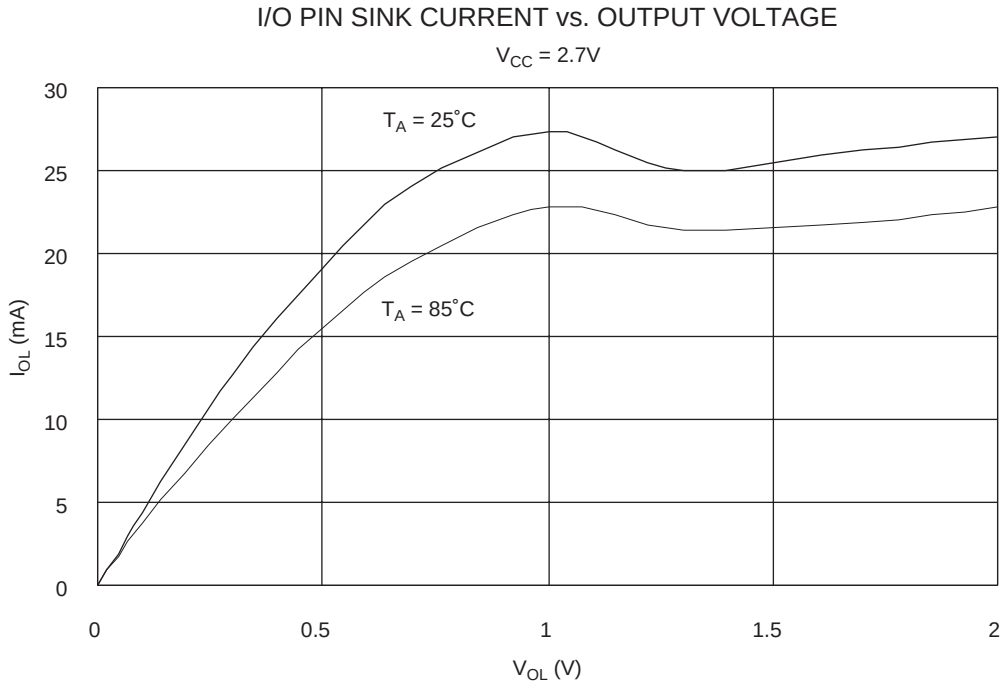


Figure 86. I/O Pin Sink Current vs. Output Voltage



Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
$3F ($5F)	SREG	I	T	H	S	V	N	Z	C	page 19
$3E ($5E)	Reserved	–	–	–	–	–	–	–	–	page 20
$3D ($5D)	SP	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	page 20
$3C ($5C)	Reserved									
$3B ($5B)	GIMSK	INT1	INT0	–	–	–	–	–	–	page 27
$3A ($5A)	GIFR	INTF1	INTF0							page 27
$39 ($59)	TIMSK	TOIE1	OCIE1	–	–	TICIE1	–	TOIE0	–	page 28
$38 ($58)	TIFR	TOV1	OCF1	–	–	ICF1	–	TOV0	–	page 29
$37 ($57)	Reserved									
$36 ($56)	Reserved									
$35 ($55)	MCUCR	–		SE	SM	ISC11	ISC10	ISC01	ISC00	page 30
$34 ($54)	MCUSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	page 26
$33 ($53)	TCCR0	–	–	–	–	–	CS02	CS01	CS00	page 34
$32 ($52)	TCNT0	Timer/Counter0 (8 Bits)								page 35
$31 ($51)	Reserved									
$30 ($50)	Reserved									
$2F ($4F)	TCCR1A	COM11	COM10	–	–	–	–	PWM11	PWM10	page 37
$2E ($4E)	TCCR1B	ICNC1	ICES1	–	–	CTC1	CS12	CS11	CS10	page 38
$2D ($4D)	TCNT1H	Timer/Counter1 – Counter Register High Byte								page 39
$2C ($4C)	TCNT1L	Timer/Counter1 – Counter Register Low Byte								page 39
$2B ($4B)	OCR1H	Timer/Counter1 – Output Compare Register High Byte								page 40
$2A ($4A)	OCR1L	Timer/Counter1 – Output Compare Register Low Byte								page 40
$29 ($49)	Reserved									
$28 ($48)	Reserved									
$27 ($47)	ICR1H	Timer/Counter1 – Input Capture Register High Byte								page 41
$26 ($46)	ICR1L	Timer/Counter1 – Input Capture Register Low Byte								page 41
$25 ($45)	Reserved									
$24 ($44)	Reserved									
$23 ($43)	Reserved									
$22 ($42)	Reserved									
$21 ($41)	WDTCR	–	–	–	WDTOE	WDE	WDP2	WDP1	WDP0	page 43
$20 ($40)	Reserved									
$1F ($3F)	Reserved									
$1E ($3E)	EEAR	EEPROM Address Register								page 45
$1D ($3D)	EEDR	EEPROM Data Register								page 45
$1C ($3C)	EECR	–	–	–	–	EERIE	EEMWE	EEWE	EERE	page 45
$1B ($3B)	Reserved									
$1A ($3A)	Reserved									
$19 ($39)	Reserved									
$18 ($38)	PORTB	–	–	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	page 72
$17 ($37)	DDRB	–	–	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	page 72
$16 ($36)	PINB	–	–	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	page 72
$15 ($35)	PORTC	–	–	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	page 78
$14 ($34)	DDRC	–	–	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	page 78
$13 ($33)	PINC	–	–	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	page 78
$12 ($32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	page 80
$11 ($31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	page 80
$10 ($30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	page 80
$0F ($2F)	SPDR	SPI Data Register								page 52
$0E ($2E)	SPSR	SPIF	WCOL	–	–	–	–	–	–	page 52
$0D ($2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	page 51
$0C ($2C)	UDR	UART I/O Data Register								page 57
$0B ($2B)	UCSRA	RXC	TXC	UDRE	FE	OR	–	–	–	page 57
$0A ($2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	CHR9	RXB8	TXB8	page 58
$09 ($29)	UBRR	UART Baud Rate Register								page 61
$08 ($28)	ACSR	ACD	AINBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	page 62
$07 ($27)	ADMUX	–	ADCBG	–	–	–	MUX2	MUX1	MUX0	page 68
$06 ($26)	ADCSR	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	page 68
$05 ($25)	ADCH	–	–	–	–	–	–	ADC9	ADC8	page 69
$04 ($24)	ADCL	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	page 69
$03 ($23)	UBRRHI					UART Baud Rate Register High				page 61
$02 ($22)	Reserved									
$01 ($21)	Reserved									
$00 ($20)	Reserved									

Ordering Information

Power Supply	Speed (MHz)	Ordering Code	Package	Operation Range
2.7 - 6.0V	4	AT90LS4433-4AC AT90LS4433-4PC	32A 28P3	Commercial (0°C to 70°C)
		AT90LS4433-4AI AT90LS4433-4PI	32A 28P3	Industrial (-40°C to 85°C)
4.0 - 6.0V	8	AT90S4433-8AC AT90S4433-8PC	32A 28P3	Commercial (0°C to 70°C)
		AT90S4433-8AI AT90S4433-8PI	32A 28P3	Industrial (-40°C to 85°C)

Package Type	
32A	32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
28P3	28-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)