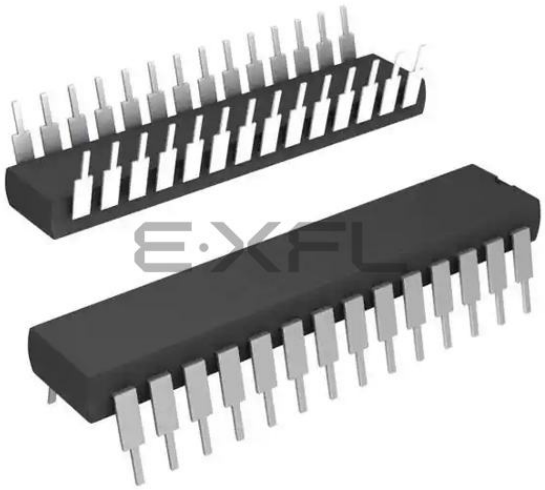

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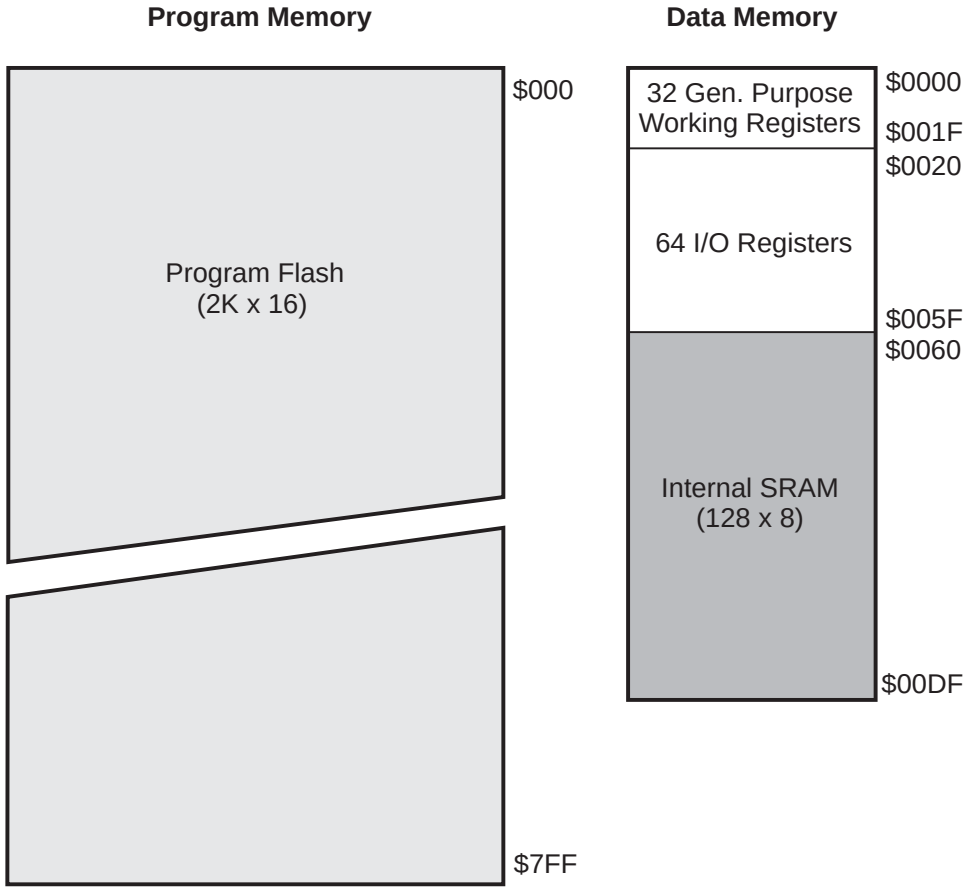
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	4MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	4KB (2K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90ls4433-4pc

Figure 6. AT90S4433 Memory Maps

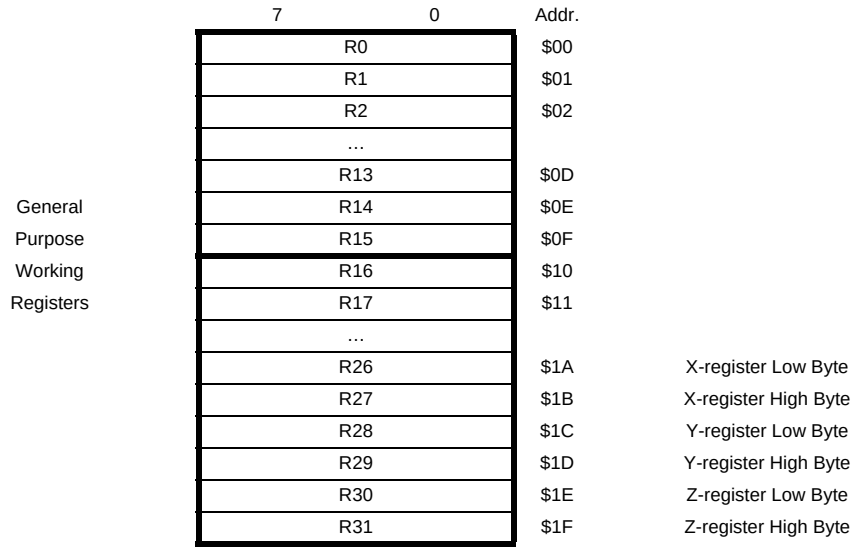


A flexible interrupt module has its control registers in the I/O space with an additional Global Interrupt Enable bit in the Status Register. All the different interrupts have a separate Interrupt Vector in the Interrupt Vector table at the beginning of the Program memory. The different interrupts have priority in accordance with their Interrupt Vector position. The lower the Interrupt Vector address, the higher the priority.

General Purpose Register File

Figure 7 shows the structure of the 32 general purpose working registers in the CPU.

Figure 7. AVR CPU General Purpose Working Registers



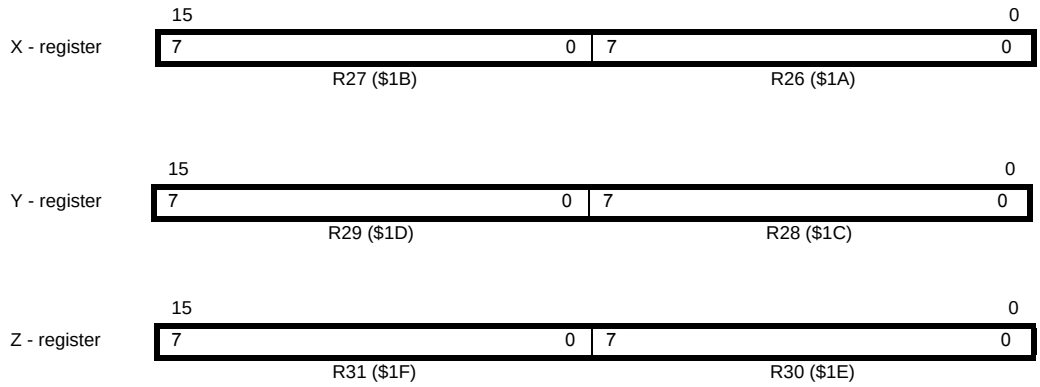
All the register operating instructions in the instruction set have direct and single cycle access to all registers. The only exceptions are the five constant arithmetic and logic instructions SBCI, SUBI, CPI, ANDI, and ORI between a constant and a register, and the LDI instruction for load immediate constant data. These instructions apply to the second half of the registers in the Register File (R16..R31). The general SBC, SUB, CP, AND, and OR, and all other operations between two registers or on a single register apply to the entire Register File.

As shown in Figure 7, each register is also assigned a data memory address, mapping them directly into the first 32 locations of the user Data Space. Although not being physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X-, Y- ,and Z-registers can be set to index any register in the file.

X-register, Y-register and Z-register

The registers R26..R31 have some added functions to their general purpose usage. These registers are address pointers for indirect addressing of the Data Space. The three indirect address registers X, Y, and Z are defined as:

Figure 8. X-, Y-, and Z-registers



In the different addressing modes, these address registers have functions as fixed displacement, automatic increment and decrement (see the descriptions for the different instructions).

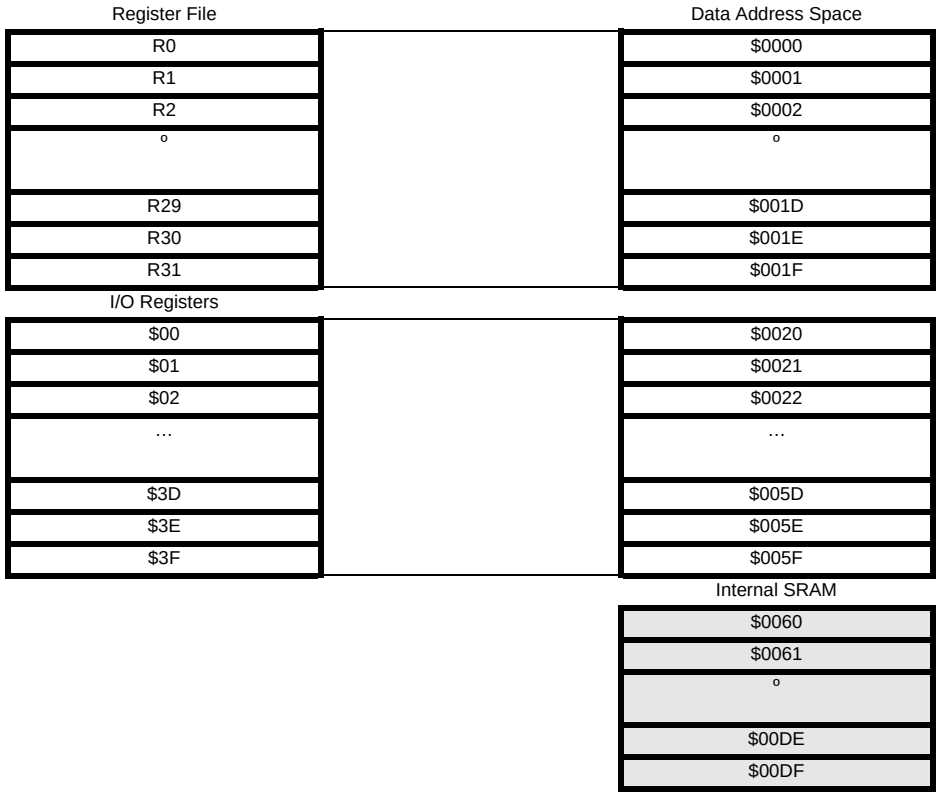
ALU – Arithmetic Logic Unit

The high-performance AVR ALU operates in direct connection with all the 32 general purpose working registers. Within a single clock cycle, ALU operations between registers in the Register File are executed. The ALU operations are divided into three main categories: arithmetic, logical, and bit functions.

In-System Programmable Flash Program Memory

The AT90S4433 contains 4K bytes of On-chip, In-System Programmable Flash memory for program storage. Since all instructions are 16- or 32-bit words, the Flash is organized as 2K x 16. The Flash memory has an endurance of at least 1,000 write/erase cycles. The AT90S4433 Program Counter (PC) is 11 bits wide, thus addressing the 2,048 program memory addresses. See page 93 for a detailed description of Flash data downloading. See page 12 for the different program memory addressing modes.

Figure 9. SRAM Organization



SRAM Data Memory

Figure 9 shows how the AT90S4433 SRAM memory is organized.

The lower 224 data memory locations address the Register File, the I/O memory and the internal data SRAM. The first 96 locations address the Register File and I/O memory, and the next 128 locations address the internal data SRAM.

The five different addressing modes for the data memory cover: Direct, Indirect with Displacement, Indirect, Indirect with Pre-decrement, and Indirect with Post-increment. In the Register File, registers R26 to R31 feature the indirect addressing pointer registers.

Stack Pointer – SP

The AT90S4433 Stack Pointer is implemented as an 8-bit register in the I/O space location $3D ($5D). As the AT90S4433 data memory has $0DF locations, eight bits are used.

	7	6	5	4	3	2	1	0	
$3D ($5D)	**SP7**	**SP6**	**SP5**	**SP4**	**SP3**	**SP2**	**SP1**	**SP0**	**SP**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The Stack Pointer points to the data SRAM stack area where the Subroutine and Interrupt stacks are located. This stack space in the data SRAM must be defined by the program before any subroutine calls are executed or interrupts are enabled. The Stack Pointer must be set to point above $60. The Stack Pointer is decremented by one when data is pushed onto the stack with the PUSH instruction, and it is decremented by two when an address is pushed onto the Stack with subroutine calls and interrupts. The Stack Pointer is incremented by one when data is popped from the stack with the POP instruction, and it is incremented by two when an address is popped from the Stack with return from subroutine RET or return from interrupt RETI.

Reset and Interrupt Handling

The AT90S4433 provides 13 different interrupt sources. These interrupts and the separate reset vector each have a separate Program Vector in the Program memory space. All interrupts are assigned individual enable bits, which must be set (one) together with the I-bit in the Status Register in order to enable the interrupt.

The lowest addresses in the Program memory space are automatically defined as the Reset and Interrupt Vectors. The complete list of Vectors is shown in Table 3. The list also determines the priority levels of the different interrupts. The lower the address, the higher the priority level. RESET has the highest priority, and next is INT0 (the External Interrupt Request 0), etc.

Table 3. Reset and Interrupt Vectors

Vector No.	Program Address	Source	Interrupt Definition
1	$000	RESET	External Pin, Power-on Reset, Brown-out Reset and Watchdog Reset
2	$001	INT0	External Interrupt Request 0
3	$002	INT1	External Interrupt Request 1
4	$003	TIMER1 CAPT	Timer/Counter1 Capture Event
5	$004	TIMER1 COMP	Timer/Counter1 Compare Match
6	$005	TIMER1 OVF	Timer/Counter1 Overflow
7	$006	TIMER0 OVF	Timer/Counter0 Overflow
8	$007	SPI, STC	Serial Transfer Complete
9	$008	UART, RX	UART, Rx Complete
10	$009	UART, UDRE	UART Data Register Empty
11	$00A	UART, TX	UART, Tx Complete
12	$00B	ADC	ADC Conversion Complete
13	$00C	EE_RDY	EEPROM Ready
14	$00D	ANA_COMP	Analog Comparator

Figure 24. Reset Logic

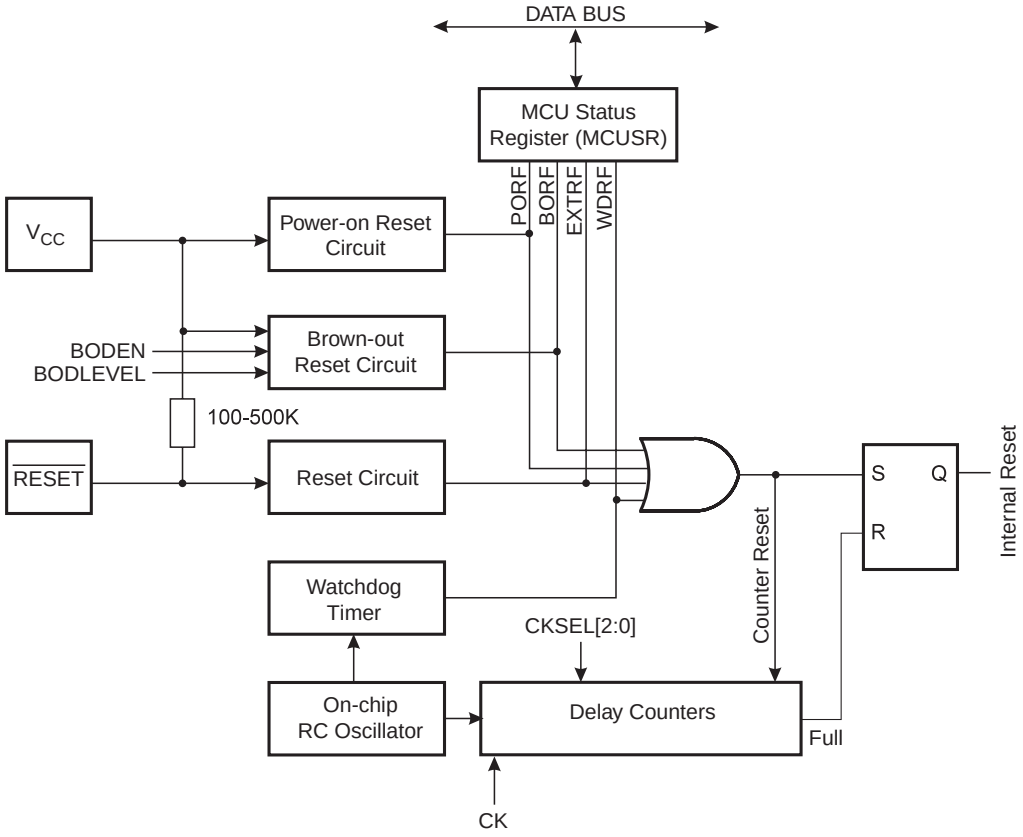


Table 4. Reset Characteristics (V_{CC} = 5.0V)

Symbol	Parameter	Min	Typ	Max	Units
V_{POT}[1]	Power-on Reset Threshold Voltage, rising	1.0	1.4	1.8	V
	Power-on Reset Threshold Voltage, falling	0.4	0.6	0.8	V
V_{RST}	$\overline{\text{RESET}}$ Pin Threshold Voltage		0.6 V_{CC}		V
V_{BOT}	Brown-out Reset Threshold Voltage	2.2 (BODLEVEL=1)	2.7 (BODLEVEL=1)	3.0 (BODLEVEL=1)	V
		3.5 (BODLEVEL=0)	4.0 (BODLEVEL=0)	4.5 (BODLEVEL=0)	

Note: 1. The Power-on Reset will not work unless the supply voltage has been below V_{POT} (falling).

SPI Status Register – SPSR

Bit	7	6	5	4	3	2	1	0	
$0E ($2E)	**SPIF**	**WCOL**	–	–	–	–	–	–	**SPSR**
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – SPIF: SPI Interrupt Flag**

When a serial transfer is complete, the SPIF bit is set (one) and an interrupt is generated if SPIE in SPCR is set (one) and global interrupts are enabled. If $\overline{SS}$ is an input and is driven low when the SPI is in Master mode, this will also set the SPIF Flag. SPIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, the SPIF bit is cleared by first reading the SPI Status Register with SPIF set (one), then by accessing the SPI Data Register (SPDR).

- **Bit 6 – WCOL: Write Collision Flag**

The WCOL bit is set if the SPI Data Register (SPDR) is written during a data transfer. The WCOL bit (and the SPIF bit) are cleared (zero) by first reading the SPI Status Register with WCOL set (one), and then by accessing the SPI Data Register.

- **Bits 5..0 – Res: Reserved Bits**

These bits are reserved bits in the AT90S4433 and will always read as zero.

The SPI interface on the AT90S4433 is also used for Program memory and EEPROM downloading or uploading. See page 93 for Serial Programming and verification.

SPI Data Register – SPDR

Bit	7	6	5	4	3	2	1	0	
$0F ($2F)	**MSB**							**LSB**	**SPDR**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	X	X	X	X	X	X	X	X	Undefined

The SPI Data Register is a read/write register used for data transfer between the Register File and the SPI Shift Register. Writing to the register initiates data transmission. Reading the register causes the Shift Register Receive buffer to be read.

- **Bit 4 – FE: Framing Error**

This bit is set if a Framing Error condition is detected, i.e., when the stop bit of an incoming character is zero.

The FE bit is cleared when the stop bit of received data is one.

- **Bit 3 – OR: OverRun**

This bit is set if an OverRun condition is detected, i.e., when a character already present in the UDR Register is not read before the next character has been shifted into the Receiver Shift Register. The OR bit is buffered, which means that it will be set once the valid data still in UDRE is read.

The OR bit is cleared (zero) when data is received and transferred to UDR.

- **Bits 2..1 – Res: Reserved Bits**

These bits are reserved bits in the AT90S4433 and will always read as zero.

- **Bit 0 – MPCM: Multi-processor Communication Mode**

This bit is used to enter Multi-processor Communication mode. The bit is set when the slave MCU waits for an address byte to be received. When the MCU has been addressed, the MCU switches off the MPCM bit and starts data reception.

For a detailed description, see “Multi-processor Communication Mode”.

UART Control and Status Register B – UCSRB

Bit	7	6	5	4	3	2	1	0	
$0A ($2A)	**RXCIE**	**TXCIE**	**UDRIE**	**RXEN**	**TXEN**	**CHR9**	**RXB8**	**TXB8**	**UCSRB**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	W	
Initial Value	0	0	0	0	0	0	1	0	

- **Bit 7 – RXCIE: RX Complete Interrupt Enable**

When this bit is set (one), a setting of the RXC bit in UCSRA will cause the Receive Complete Interrupt routine to be executed, provided that global interrupts are enabled.

- **Bit 6 – TXCIE: TX Complete Interrupt Enable**

When this bit is set (one), a setting of the TXC bit in UCSRA will cause the Transmit Complete Interrupt routine to be executed, provided that global interrupts are enabled.

- **Bit 5 – UDRIE: UART Data Register Empty Interrupt Enable**

When this bit is set (one), a setting of the UDRE bit in UCSRA will cause the UART Data Register Empty Interrupt routine to be executed, provided that global interrupts are enabled.

- **Bit 4 – RXEN: Receiver Enable**

This bit enables the UART Receiver when set (one). When the Receiver is disabled, the RXC, OR, and FE status flags cannot become set. If these flags are set, turning off RXEN does not cause them to be cleared.

Table 19. UBR Settings at Various Crystal Frequencies

Baud Rate	1 MHz		%Error	1.8432 MHz		%Error	2 MHz		%Error	2.4576 MHz		%Error
2400	UBR=	**25**	**0.2**	UBR=	**47**	**0.0**	UBR=	**51**	**0.2**	UBR=	**63**	**0.0**
4800	UBR=	**12**	**0.2**	UBR=	**23**	**0.0**	UBR=	**25**	**0.2**	UBR=	**31**	**0.0**
9600	UBR=	6	7.5	UBR=	**11**	**0.0**	UBR=	**12**	**0.2**	UBR=	**15**	**0.0**
14400	UBR=	3	7.8	UBR=	**7**	**0.0**	UBR=	8	3.7	UBR=	10	3.1
19200	UBR=	2	7.8	UBR=	**5**	**0.0**	UBR=	6	7.5	UBR=	**7**	**0.0**
28800	UBR=	1	7.8	UBR=	**3**	**0.0**	UBR=	3	7.8	UBR=	4	6.3
38400	UBR=	1	22.9	UBR=	**2**	**0.0**	UBR=	2	7.8	UBR=	**3**	**0.0**
57600	UBR=	0	7.8	UBR=	**1**	**0.0**	UBR=	1	7.8	UBR=	2	12.5
76800	UBR=	0	22.9	UBR=	1	33.3	UBR=	1	22.9	UBR=	**1**	**0.0**
115200	UBR=	0	84.3	UBR=	**0**	**0.0**	UBR=	0	7.8	UBR=	0	25.0

Baud Rate	3.2768 MHz		%Error	3.6864 MHz		%Error	4 MHz		%Error	4.608 MHz		%Error
2400	UBR=	**84**	**0.4**	UBR=	**95**	**0.0**	UBR=	**103**	**0.2**	UBR=	**119**	**0.0**
4800	UBR=	**42**	**0.8**	UBR=	**47**	**0.0**	UBR=	**51**	**0.2**	UBR=	**59**	**0.0**
9600	UBR=	**20**	**1.6**	UBR=	**23**	**0.0**	UBR=	**25**	**0.2**	UBR=	**29**	**0.0**
14400	UBR=	**13**	**1.6**	UBR=	**15**	**0.0**	UBR=	16	2.1	UBR=	**19**	**0.0**
19200	UBR=	10	3.1	UBR=	**11**	**0.0**	UBR=	**12**	**0.2**	UBR=	**14**	**0.0**
28800	UBR=	**6**	**1.6**	UBR=	**7**	**0.0**	UBR=	8	3.7	UBR=	**9**	**0.0**
38400	UBR=	4	6.3	UBR=	**5**	**0.0**	UBR=	6	7.5	UBR=	7	6.7
57600	UBR=	3	12.5	UBR=	**3**	**0.0**	UBR=	3	7.8	UBR=	**4**	**0.0**
76800	UBR=	2	12.5	UBR=	**2**	**0.0**	UBR=	2	7.8	UBR=	3	6.7
115200	UBR=	1	12.5	UBR=	**1**	**0.0**	UBR=	1	7.8	UBR=	2	20.0

Baud Rate	7.3728 MHz		%Error	8 MHz		%Error	9.216 MHz		%Error	11.059 MHz		%Error
2400	UBR=	**191**	**0.0**	UBR=	**207**	**0.2**	UBR=	**239**	**0.0**	UBR=	287	-
4800	UBR=	**95**	**0.0**	UBR=	**103**	**0.2**	UBR=	**119**	**0.0**	UBR=	**143**	**0.0**
9600	UBR=	**47**	**0.0**	UBR=	**51**	**0.2**	UBR=	**59**	**0.0**	UBR=	**71**	**0.0**
14400	UBR=	**31**	**0.0**	UBR=	**34**	**0.8**	UBR=	**39**	**0.0**	UBR=	**47**	**0.0**
19200	UBR=	**23**	**0.0**	UBR=	**25**	**0.2**	UBR=	**29**	**0.0**	UBR=	**35**	**0.0**
28800	UBR=	**15**	**0.0**	UBR=	16	2.1	UBR=	**19**	**0.0**	UBR=	**23**	**0.0**
38400	UBR=	**11**	**0.0**	UBR=	**12**	**0.2**	UBR=	**14**	**0.0**	UBR=	**17**	**0.0**
57600	UBR=	**7**	**0.0**	UBR=	8	3.7	UBR=	**9**	**0.0**	UBR=	**11**	**0.0**
76800	UBR=	**5**	**0.0**	UBR=	6	7.5	UBR=	7	6.7	UBR=	**8**	**0.0**
115200	UBR=	**3**	**0.0**	UBR=	3	7.8	UBR=	**4**	**0.0**	UBR=	**5**	**0.0**

keeps running for as long as the ADEN bit is set and is continuously reset when ADEN is low.

When initiating a conversion by setting the ADSC bit in ADCSR, the conversion starts at the following rising edge of the ADC clock cycle. The actual sample-and-hold takes place 1.5 ADC clock cycles after the start of the conversion. The result is ready and written to the ADC Result Register after 13 cycles. In Single Conversion mode, the ADC needs one more clock cycle before a new conversion can be started (see Figure 47). If ADSC is set high in this period, the ADC will start the new conversion immediately. In Free Run mode, a new conversion will be started immediately after the result is written to the ADC Result Register. Using Free Run mode and an ADC clock frequency of 200 kHz gives the lowest conversion time, 65 µs, equivalent to 15.4 kSPS. For a summary of conversion times, see Table 21.

Figure 46. ADC Timing Diagram, First Conversion (Single Conversion Mode)

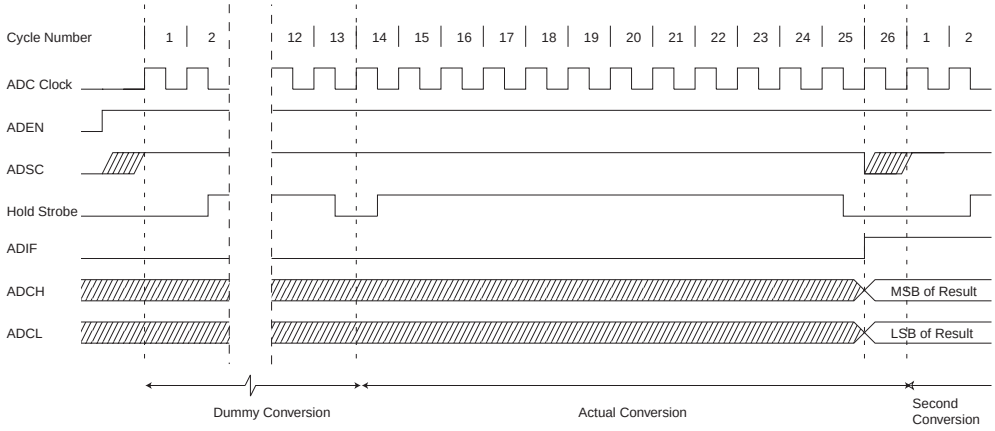


Table 21. ADC Conversion Time

Condition	Sample Cycle Number	Result Ready(Cycle Number)	Total Conversion Time (Cycles)	Total Conversion Time (µs)
1st Conversion, Free Run	13.5	25	25	125 - 500
1st Conversion, Single	13.5	25	26	130 - 520
Free Run Conversion	1.5	13	13	65 - 260
Single Conversion	1.5	13	14	70 - 280

Figure 47. ADC Timing Diagram, Single Conversion

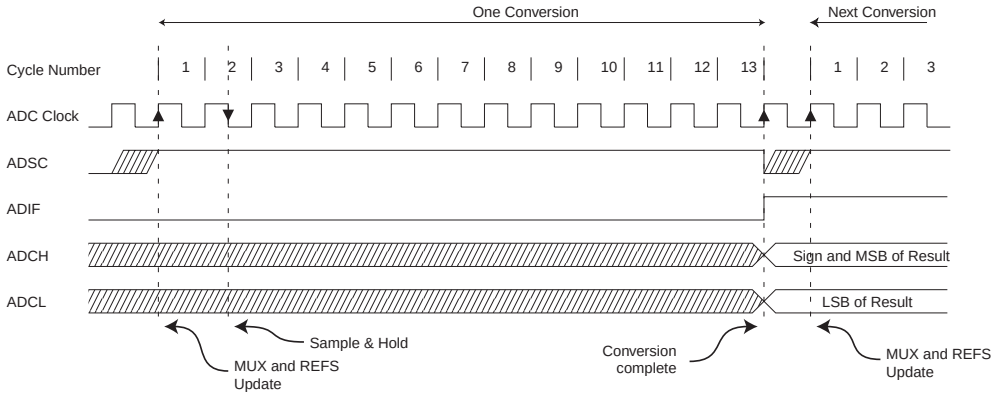
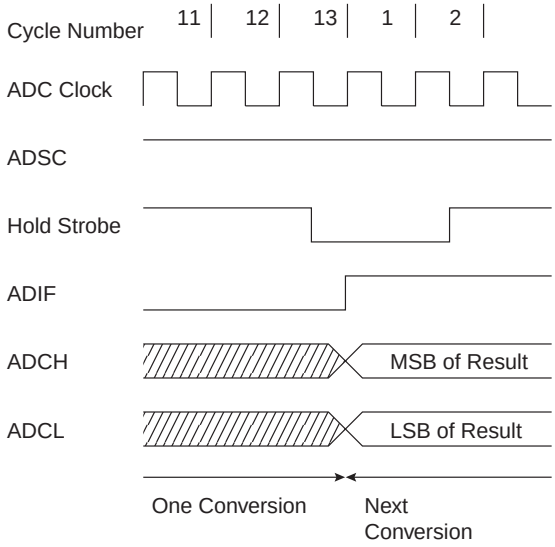


Figure 48. ADC Timing Diagram, Free Run Conversion



ADC Noise Canceler Function

The ADC features a Noise Canceler that enables conversion during Idle mode to reduce noise induced from the CPU core. To make use of this feature, the following procedure should be used:

1. Make sure that the ADC is enabled and is not busy converting. Single Conversion mode must be selected and the ADC conversion complete interrupt must be enabled. Thus:
   ADEN = 1
   ADSC = 0
   ADFR = 0
   ADIE = 1
2. Enter Idle mode. The ADC will start a conversion once the CPU has been halted.
3. If no other interrupts occur before the ADC conversion completes, the ADC interrupt will wake up the MCU and execute the ADC conversion complete interrupt routine.

- **Bit 5 – ADFR: ADC Free Run Select**

When this bit is set (one), the ADC operates in Free Run mode. In this mode, the ADC samples and updates the Data Registers continuously. Clearing this bit (zero) will terminate Free Run mode.

- **Bit 4 – ADIF: ADC Interrupt Flag**

This bit is set (one) when an ADC conversion completes and the Data Registers are updated. The ADC Conversion Complete interrupt is executed if the ADIE bit and the I-bit in SREG are set (one). ADIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ADIF is cleared by writing a logical “1” to the flag. Beware that if doing a Read-Modify-Write on ADCSR, a pending interrupt can be disabled. This also applies if the SBI and CBI instructions are used.

- **Bit 3 – ADIE: ADC Interrupt Enable**

When this bit is set (one) and the I-bit in SREG is set (one), the ADC Conversion Complete interrupt is activated.

- **Bits 2..0 – ADPS2..ADPS0: ADC Prescaler Select Bits**

These bits determine the division factor between the XTAL frequency and the input clock to the ADC.

Table 22. ADC Prescaler Selections

ADPS2	ADPS1	ADPS0	Division Factor
0	0	0	2
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

ADC Data Register – ADCL AND ADCH

Bit	15	14	13	12	11	10	9	8	
$05 ($25)	–	–	–	–	–	–	ADC9	ADC8	ADCH
$04 ($26)	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	ADCL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

When an ADC conversion is complete, the result is found in these two registers. In Free Run mode, it is essential that both registers are read and that ADCL is read before ADCH.

ADC Characteristics T_A = -40°C to 85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Resolution			10		Bits
	Absolute Accuracy	V_{REF} = 4V ADC clock = 200 kHz		1	2	LSB
	Absolute Accuracy	V_{REF} = 4V ADC clock = 1 MHz		4		LSB
	Absolute Accuracy	V_{REF} = 4V ADC clock = 2 MHz		16		LSB
	Integral Non-linearity	V_{REF} > 2V		0.5		LSB
	Differential Non-linearity	V_{REF} > 2V		0.5		LSB
	Zero Error (Offset)			1		LSB
	Conversion Time		65		260	µs
	Clock Frequency		50		200	kHz
AVCC	Analog Supply Voltage		V_{CC} - 0.3(1)		V_{CC} + 0.3(2)	V
V_{REF}	Reference Voltage		2		AVCC	V
R_{REF}	Reference Input Resistance		6	10	13	kΩ
R_{AIN}	Analog Input Resistance			100		MΩ

Notes: 1. Minimum for AVCC is 2.7V.
2. Maximum for AVCC is 6.0V.

I/O Ports

All AVR ports have true Read-Modify-Write functionality when used as general digital I/O ports. This means that the direction of one port pin can be changed without unintentionally changing the direction of any other pin with the SBI and CBI instructions. The same applies for changing drive value (if configured as output) or enabling/disabling of pull-up resistors (if configured as input).

Port B

Port B is a 6-bit bi-directional I/O port.

Three I/O memory address locations are allocated for the Port B, one each for the Data Register – PORTB, $18($38), Data Direction Register – DDRB, $17($37), and the Port B Input Pins – PINB, $16($36). The Port B Input Pins address is read only, while the Data Register and the Data Direction Register are read/write.

All port pins have individually selectable pull-up resistors. The Port B output buffers can sink 20 mA and thus drive LED displays directly. When pins PB0 to PB7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

The Port B pins with alternate functions are shown in Table 23.

Table 23. Port B Pin Alternate Functions

Port Pin	Alternate Functions
PB0	ICP (Timer/Counter1 Input Capture Pin)
PB1	OC1 (Timer/Counter1 Output Compare Match Output)
PB2	$\overline{SS}$ (SPI Slave Select Input)
PB3	MOSI (SPI Bus Master Output/Slave Input)
PB4	MISO (SPI Bus Master Input/Slave Output)
PB5	SCK (SPI Bus Serial Clock)

When the pins are used for the alternate function, the DDRB and PORTB Registers have to be set according to the alternate function description.

Port B Data Register – PORTB

Bit	7	6	5	4	3	2	1	0	
$18 ($38)	–	–	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	PORTB
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

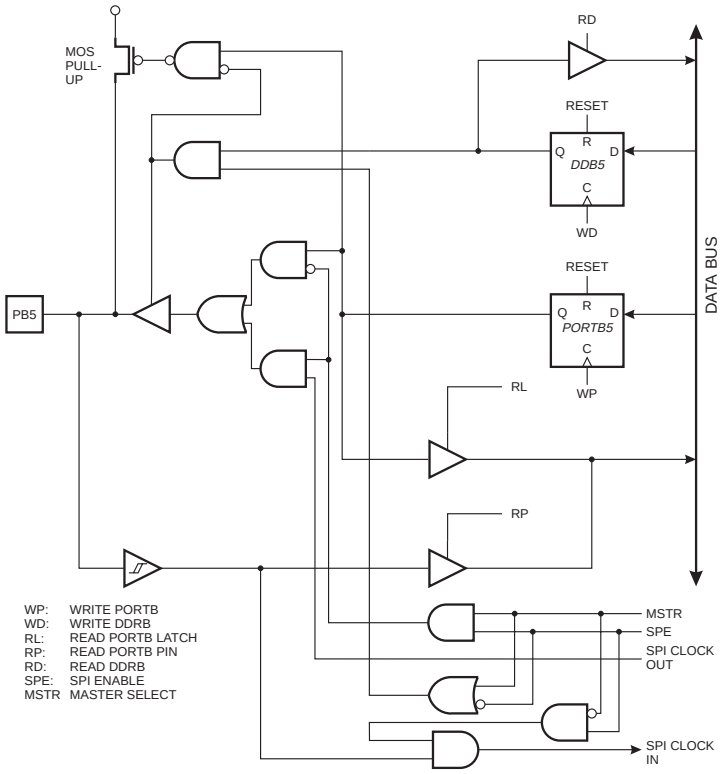
Port B Data Direction Register – DDRB

Bit	7	6	5	4	3	2	1	0	
$17 ($37)	–	–	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port B Input Pins Address – PINB

Bit	7	6	5	4	3	2	1	0	
$16 ($36)	–	–	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	PINB
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	0	0	N/A	N/A	N/A	N/A	N/A	N/A	

Figure 55. Port B Schematic Diagram (Pin PB5)



Port C

Port C is a 6-bit bi-directional I/O port.

Three I/O memory address locations are allocated for the Port C, one each for the Data Register – PORTC, $15($35), Data Direction Register – DDRC, $14($34), and the Port C Input Pins – PINC, $13($33). The Port C Input Pins address is read only, while the Data Register and the Data Direction Register are read/write.

All port pins have individually selectable pull-up resistors. The Port C output buffers can sink 20 mA and thus drive LED displays directly. When pins PC0 to PC5 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

Port C has an alternate function as analog inputs for the ADC. If some Port C pins are configured as outputs, it is essential that these do not switch when a conversion is in progress. This might corrupt the result of the conversion.

During Power-down mode, the Schmitt triggers of the digital inputs are disconnected. This allows an analog voltage close to $V_{CC}/2$ to be present during Power-down without causing excessive power consumption.

Programming the Fuse Bits

The algorithm for programming the Fuse bits is as follows (refer to “Programming the Flash” for details on command and data loading):

A: Load Command “0100 0000”.

B: Load Data Low Byte. Bit n = “0” programs and bit n = “1” erases the Fuse bit.

Bit 5 = SPIEN Fuse bit
Bit 4 = BODLEVEL Fuse bit
Bit 3 = BODEN Fuse bit
Bit 2 = CKSEL2 Fuse bit
Bit 1 = CKSEL1 Fuse bit
Bit 0 = CKSEL0 Fuse bit
Bits 7 - 6 = “1”. These bits are reserved and should be left unprogrammed (“1”).

1. Give $\overline{WR}$ a t_{WLWH_PFB} wide negative pulse to execute the programming, t_{WLWH_PFB} is found in Table 33. Programming the Fuse bits does not generate any activity on the RDY/$\overline{BSY}$ pin.

Programming the Lock Bits

The algorithm for programming the Lock bits is as follows (refer to “Programming the Flash” for details on command and data loading):

A: Load Command “0010 0000”.

B: Load Data Low Byte. Bit n = “0” programs the Lock bit.

Bit 2 = Lock bit 2
Bit 1 = Lock bit 1
Bits 7 - 3, 0 = “1”. These bits are reserved and should be left unprogrammed (“1”).

C: Write Data Low Byte.

The Lock bits can only be cleared by executing Chip Erase.

Reading the Fuse and Lock Bits

The algorithm for reading the Fuse and Lock bits is as follows (refer to “Programming the Flash” for details on command loading):

A: Load Command “0000 0100”.

1. Set $\overline{OE}$ to “0”, and BS to “0”. The status of the Fuse bits can now be read at DATA (“0” means programmed).
   Bit 5 = SPIEN Fuse bit
   Bit 4 = BODLEVEL Fuse bit
   Bit 3 = BODEN Fuse bit
   Bit 2 = CKSEL2 Fuse bit
   Bit 1 = CKSEL1 Fuse bit
   Bit 0 = CKSEL0 Fuse bit
2. Set BS to “1”. The status of the Lock bits can now be read at DATA (“0” means programmed).
   Bit 2 = Lock Bit 2
   Bit 1= Lock Bit 1
3. Set $\overline{OE}$ to “1”.

External Clock Drive Waveforms

Figure 69. External Clock

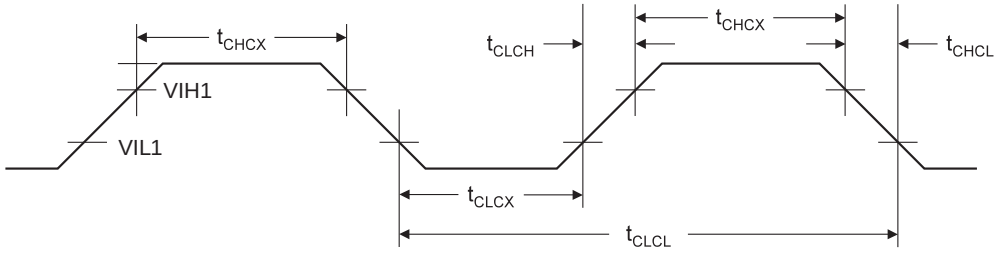
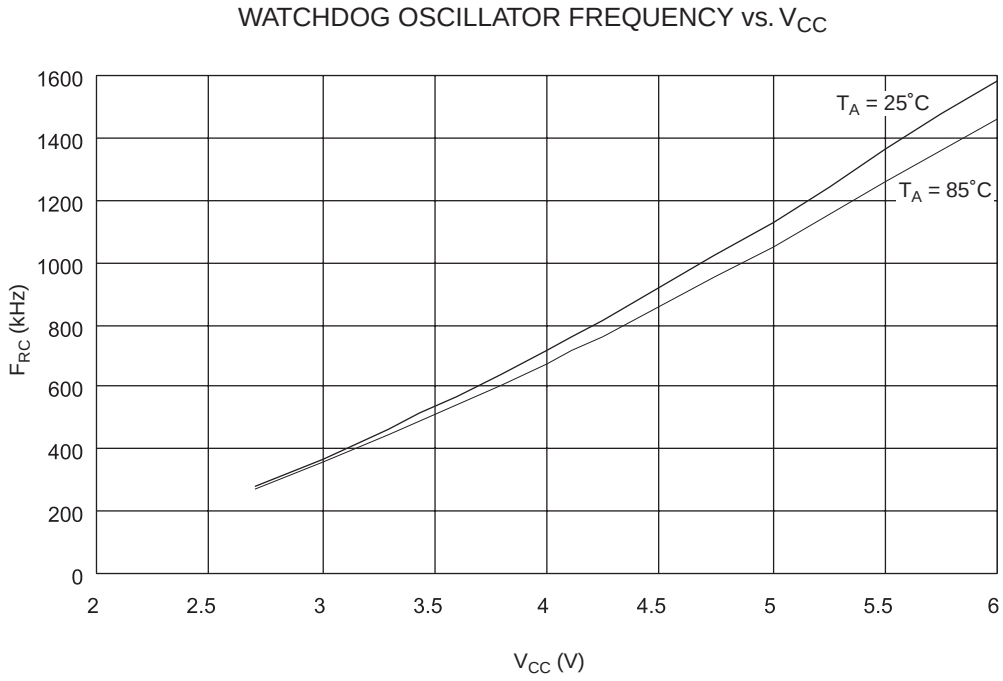


Table 39. External Clock Drive

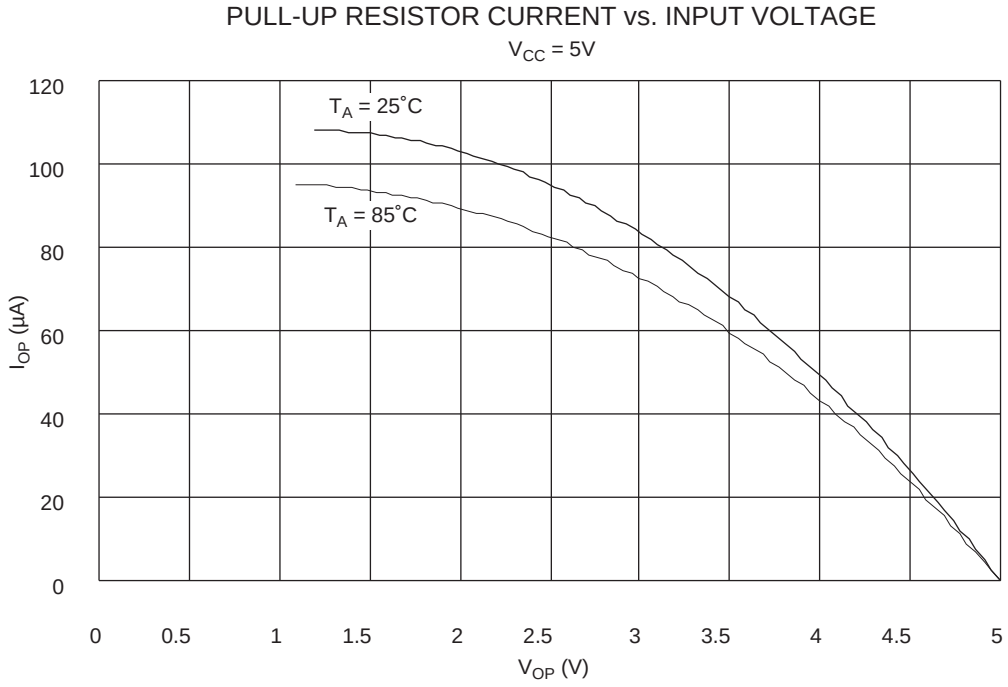
Symbol	Parameter	V_{CC} = 2.7V to 6.0V		V_{CC} = 4.0V to 6.0V		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0.0	4.0	0.0	8.0	MHz
t_{CLCL}	Clock Period	250.0		125.0		ns
t_{CHCX}	High Time	100.0		50.0		ns
t_{CLCX}	Low Time	100.0		50.0		ns
t_{CLCH}	Rise Time		1.6		0.5	µs
t_{CHCL}	Fall Time		1.6		0.5	µs

Figure 81. Watchdog Oscillator Frequency vs. V_{CC}



Sink and source capabilities of I/O ports are measured on one pin at a time.

Figure 82. Pull-up Resistor Current vs. Input Voltage



Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
$3F ($5F)	SREG	I	T	H	S	V	N	Z	C	page 19
$3E ($5E)	Reserved	–	–	–	–	–	–	–	–	page 20
$3D ($5D)	SP	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	page 20
$3C ($5C)	Reserved									
$3B ($5B)	GIMSK	INT1	INT0	–	–	–	–	–	–	page 27
$3A ($5A)	GIFR	INTF1	INTF0							page 27
$39 ($59)	TIMSK	TOIE1	OCIE1	–	–	TICIE1	–	TOIE0	–	page 28
$38 ($58)	TIFR	TOV1	OCF1	–	–	ICF1	–	TOV0	–	page 29
$37 ($57)	Reserved									
$36 ($56)	Reserved									
$35 ($55)	MCUCR	–		SE	SM	ISC11	ISC10	ISC01	ISC00	page 30
$34 ($54)	MCUSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	page 26
$33 ($53)	TCCR0	–	–	–	–	–	CS02	CS01	CS00	page 34
$32 ($52)	TCNT0	Timer/Counter0 (8 Bits)								page 35
$31 ($51)	Reserved									
$30 ($50)	Reserved									
$2F ($4F)	TCCR1A	COM11	COM10	–	–	–	–	PWM11	PWM10	page 37
$2E ($4E)	TCCR1B	ICNC1	ICES1	–	–	CTC1	CS12	CS11	CS10	page 38
$2D ($4D)	TCNT1H	Timer/Counter1 – Counter Register High Byte								page 39
$2C ($4C)	TCNT1L	Timer/Counter1 – Counter Register Low Byte								page 39
$2B ($4B)	OCR1H	Timer/Counter1 – Output Compare Register High Byte								page 40
$2A ($4A)	OCR1L	Timer/Counter1 – Output Compare Register Low Byte								page 40
$29 ($49)	Reserved									
$28 ($48)	Reserved									
$27 ($47)	ICR1H	Timer/Counter1 – Input Capture Register High Byte								page 41
$26 ($46)	ICR1L	Timer/Counter1 – Input Capture Register Low Byte								page 41
$25 ($45)	Reserved									
$24 ($44)	Reserved									
$23 ($43)	Reserved									
$22 ($42)	Reserved									
$21 ($41)	WDTCR	–	–	–	WDTOE	WDE	WDP2	WDP1	WDP0	page 43
$20 ($40)	Reserved									
$1F ($3F)	Reserved									
$1E ($3E)	EEAR	EEPROM Address Register								page 45
$1D ($3D)	EEDR	EEPROM Data Register								page 45
$1C ($3C)	EECR	–	–	–	–	EERIE	EEMWE	EEWE	EERE	page 45
$1B ($3B)	Reserved									
$1A ($3A)	Reserved									
$19 ($39)	Reserved									
$18 ($38)	PORTB	–	–	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	page 72
$17 ($37)	DDRB	–	–	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	page 72
$16 ($36)	PINB	–	–	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	page 72
$15 ($35)	PORTC	–	–	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	page 78
$14 ($34)	DDRC	–	–	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	page 78
$13 ($33)	PINC	–	–	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	page 78
$12 ($32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	page 80
$11 ($31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	page 80
$10 ($30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	page 80
$0F ($2F)	SPDR	SPI Data Register								page 52
$0E ($2E)	SPSR	SPIF	WCOL	–	–	–	–	–	–	page 52
$0D ($2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	page 51
$0C ($2C)	UDR	UART I/O Data Register								page 57
$0B ($2B)	UCSRA	RXC	TXC	UDRE	FE	OR	–	–	–	page 57
$0A ($2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	CHR9	RXB8	TXB8	page 58
$09 ($29)	UBRR	UART Baud Rate Register								page 61
$08 ($28)	ACSR	ACD	AINBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	page 62
$07 ($27)	ADMUX	–	ADCBG	–	–	–	MUX2	MUX1	MUX0	page 68
$06 ($26)	ADCSR	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	page 68
$05 ($25)	ADCH	–	–	–	–	–	–	ADC9	ADC8	page 69
$04 ($24)	ADCL	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	page 69
$03 ($23)	UBRRHI					UART Baud Rate Register High				page 61
$02 ($22)	Reserved									
$01 ($21)	Reserved									
$00 ($20)	Reserved									

Data Sheet Change Log for AT90S/LS4433

This section containes a log on the changes made to the data sheet for AT90S/LS4433. All refereces to pages in Change Log, are referred to this document.

Changes from Rev. 1042E-09/01 to Ref. 1042F-03/02

1 **Updated minimum AREF Voltage on page 5 and page 64.**

2 **Corrected VBOT Max for BODLEVEL = 1 in Table 4 on page 22.**

3 **Updated Corporate Template.**

Changes from Rev. 1042F-03/02 to Ref. 1042G-09/02

1 **Added wathermark “Not recommended for new designs. Use ATmega8”.**

2 **Added Errata Sheet to the Data Sheet.**

Changes from Rev. 1042G-09/02 to Ref. 1042H-04/03

1 **Updated the “Errata for AT90S/LS4433 Rev. Rev. C/D/E/F” on page 119.**

2 **Updated “Packaging Information” on page 117.**