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Details

Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	4KB (2K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90s4433-8ac

Description

The AT90S4433 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the AT90S4433 achieves throughputs approaching 1 MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The AT90S4433 provides the following features: 4K bytes of In-System Programmable Flash, 256 bytes of EEPROM, 128 bytes of SRAM, 20 general purpose I/O lines, 32 general purpose working registers, two flexible Timer/Counters with compare modes, internal and external interrupts, a programmable serial UART, 6-channel, 10-bit ADC, programmable Watchdog Timer with internal Oscillator, an SPI serial port and two software-selectable Power-saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset.

The device is manufactured using Atmel's high-density non-volatile memory technology. The On-chip Flash Program memory can be re-programmed In-System through an SPI serial interface or by a conventional non-volatile memory programmer. By combining a RISC 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT90S4433 is a powerful microcontroller that provides a highly flexible and cost-effective solution to many embedded control applications.

The AT90S4433 AVR is supported with a full suite of program and system development tools including: C Compilers, macro assemblers, program debugger/simulators, In-Circuit Emulators and evaluation kits.

Table 1. Comparison Table

Device	Flash	EEPROM	SRAM	Voltage Range	Frequency
AT90S4433	4K	256B	128B	4.0V - 6.0V	0 - 8 MHz
AT90LS4433	4K	256B	128B	2.7V - 6.0V	0 - 4 MHz

Pin Descriptions

VCC	Supply voltage.
GND	Ground.
Port B (PB5..PB0)	<p>Port B is a 6-bit bi-directional I/O port with internal pull-up resistors. The Port B output buffers can sink 20 mA. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated.</p> <p>Port B also serves the functions of various special features of the AT90S4433 as listed on page 73.</p> <p>The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.</p>
Port C (PC5..PC0)	<p>Port C is a 6-bit bi-directional I/O port with internal pull-up resistors. The Port C output buffers can sink 20 mA. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. Port C also serves as the analog inputs to the A/D Converter.</p> <p>The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.</p>
Port D (PD7..PD0)	<p>Port D is an 8-bit bi-directional I/O port with internal pull-up resistors. The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated.</p> <p>Port D also serves the functions of various special features of the AT90S4433 as listed on page 81.</p> <p>The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.</p>
$\overline{\text{RESET}}$	Reset input. An External Reset is generated by a low level on the $\overline{\text{RESET}}$ pin. Reset pulses longer than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.
XTAL1	Input to the inverting oscillator amplifier and input to the internal clock operating circuit
XTAL2	Output from the inverting oscillator amplifier
AVCC	AVCC is the supply voltage for Port A and the A/D Converter. If the ADC is not used, this pin must be connected to V_{CC} . If the ADC is used, this pin should be connected to V_{CC} via a low-pass filter. See page 64 for details on operation of the ADC.
AREF	AREF is the analog reference input for the A/D Converter. For ADC operations, a voltage in the range 2.0V to AVCC must be applied to this pin.
AGND	If the board has a separate analog ground plane, this pin should be connected to this ground plane. Otherwise, connect to GND.

General Purpose Register File

Figure 7 shows the structure of the 32 general purpose working registers in the CPU.

Figure 7. AVR CPU General Purpose Working Registers

	7	0	Addr.	
	R0		\$00	
	R1		\$01	
	R2		\$02	
	...			
	R13		\$0D	
	R14		\$0E	
	R15		\$0F	
General	R16		\$10	
Purpose	R17		\$11	
Working	...			
Registers	R26		\$1A	X-register Low Byte
	R27		\$1B	X-register High Byte
	R28		\$1C	Y-register Low Byte
	R29		\$1D	Y-register High Byte
	R30		\$1E	Z-register Low Byte
	R31		\$1F	Z-register High Byte

All the register operating instructions in the instruction set have direct and single cycle access to all registers. The only exceptions are the five constant arithmetic and logic instructions SBCI, SUBI, CPI, ANDI, and ORI between a constant and a register, and the LDI instruction for load immediate constant data. These instructions apply to the second half of the registers in the Register File (R16..R31). The general SBC, SUB, CP, AND, and OR, and all other operations between two registers or on a single register apply to the entire Register File.

As shown in Figure 7, each register is also assigned a data memory address, mapping them directly into the first 32 locations of the user Data Space. Although not being physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X-, Y-, and Z-registers can be set to index any register in the file.

X-register, Y-register and Z-register

The registers R26..R31 have some added functions to their general purpose usage. These registers are address pointers for indirect addressing of the Data Space. The three indirect address registers X, Y, and Z are defined as:

Figure 8. X-, Y-, and Z-registers

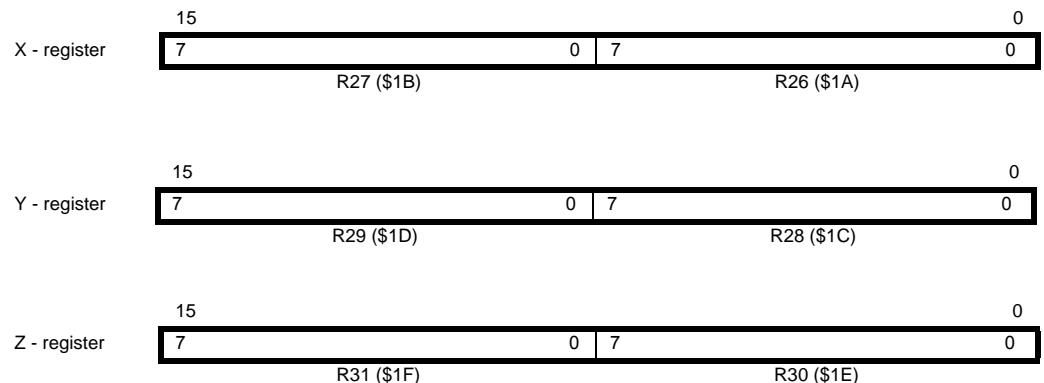


Table 2. AT90S4433 I/O Space⁽¹⁾ (Continued)

I/O Address (SRAM Address)	Name	Function
\$17 (\$37)	DDRB	Data Direction Register, Port B
\$16 (\$36)	PINB	Input Pins, Port B
\$15 (\$35)	PORTC	Data Register, Port C
\$14 (\$34)	DDRC	Data Direction Register, Port C
\$13 (\$33)	PINC	Input Pins, Port C
\$12 (\$32)	PORTD	Data Register, Port D
\$11 (\$31)	DDRD	Data Direction Register, Port D
\$10 (\$30)	PIND	Input Pins, Port D
\$0F (\$2F)	SPDR	SPI I/O Data Register
\$0E (\$2E)	SPSR	SPI Status Register
\$0D (\$2D)	SPCR	SPI Control Register
\$0C (\$2C)	UDR	UART I/O Data Register
\$0B (\$2B)	UCSRA	UART Control and Status Register A
\$0A (\$2A)	UCSRB	UART Control and Status Register B
\$09 (\$29)	UBRR	UART Baud Rate Register
\$08 (\$28)	ACSR	Analog Comparator Control and Status Register
\$07 (\$27)	ADMUX	ADC Multiplexer Select Register
\$06 (\$26)	ADCSR	ADC Control and Status Register
\$05 (\$25)	ADCH	ADC Data Register High
\$04 (\$24)	ADCL	ADC Data Register Low
\$03 (\$23)	UBRRHI	UART Baud Rate Register High

Note: 1. Reserved and unused locations are not shown in the table.

All AT90S4433 I/Os and peripherals are placed in the I/O space. The I/O locations are accessed by the IN and OUT instructions transferring data between the 32 general purpose working registers and the I/O space. I/O Registers within the address range \$00 - \$1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions. Refer to the instruction set section for more details. When using the I/O specific commands IN and OUT, the I/O addresses \$00 - \$3F must be used. When addressing I/O Registers as SRAM, \$20 must be added to this address. All I/O Register addresses throughout this document are shown with the SRAM address in parentheses.

For compatibility with future devices, reserved bits should be written to zero when accessed. Reserved I/O memory addresses should never be written.

Some of the Status Flags are cleared by writing a logical “1” to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers \$00 to \$1F only.

The I/O and Peripherals Control Registers are explained in the following sections.

Stack Pointer – SP

The AT90S4433 Stack Pointer is implemented as an 8-bit register in the I/O space location \$3D (\$5D). As the AT90S4433 data memory has \$0DF locations, eight bits are used.

	7	6	5	4	3	2	1	0	
\$3D (\$5D)	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SP
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The Stack Pointer points to the data SRAM stack area where the Subroutine and Interrupt stacks are located. This stack space in the data SRAM must be defined by the program before any subroutine calls are executed or interrupts are enabled. The Stack Pointer must be set to point above \$60. The Stack Pointer is decremented by one when data is pushed onto the stack with the PUSH instruction, and it is decremented by two when an address is pushed onto the Stack with subroutine calls and interrupts. The Stack Pointer is incremented by one when data is popped from the stack with the POP instruction, and it is incremented by two when an address is popped from the Stack with return from subroutine RET or return from interrupt RETI.

Reset and Interrupt Handling

The AT90S4433 provides 13 different interrupt sources. These interrupts and the separate reset vector each have a separate Program Vector in the Program memory space. All interrupts are assigned individual enable bits, which must be set (one) together with the I-bit in the Status Register in order to enable the interrupt.

The lowest addresses in the Program memory space are automatically defined as the Reset and Interrupt Vectors. The complete list of Vectors is shown in Table 3. The list also determines the priority levels of the different interrupts. The lower the address, the higher the priority level. RESET has the highest priority, and next is INT0 (the External Interrupt Request 0), etc.

Table 3. Reset and Interrupt Vectors

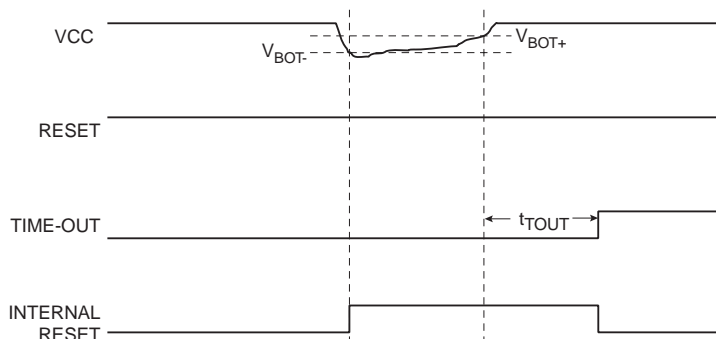
Vector No.	Program Address	Source	Interrupt Definition
1	\$000	RESET	External Pin, Power-on Reset, Brown-out Reset and Watchdog Reset
2	\$001	INT0	External Interrupt Request 0
3	\$002	INT1	External Interrupt Request 1
4	\$003	TIMER1 CAPT	Timer/Counter1 Capture Event
5	\$004	TIMER1 COMP	Timer/Counter1 Compare Match
6	\$005	TIMER1 OVF	Timer/Counter1 Overflow
7	\$006	TIMER0 OVF	Timer/Counter0 Overflow
8	\$007	SPI, STC	Serial Transfer Complete
9	\$008	UART, RX	UART, Rx Complete
10	\$009	UART, UDRE	UART Data Register Empty
11	\$00A	UART, TX	UART, Tx Complete
12	\$00B	ADC	ADC Conversion Complete
13	\$00C	EE_RDY	EEPROM Ready
14	\$00D	ANA_COMP	Analog Comparator

Brown-out Detection

AT90S4433 has an On-chip Brown-out Detection (BOD) circuit for monitoring the V_{CC} level during the operation. The power supply must be decoupled with a 47 nF to 100 nF capacitor if the BOD function is used. The BOD circuit can be enabled/disabled by the fuse BODEN. When BODEN is enabled (BODEN programmed), and V_{CC} decreases to a value below the trigger level, the Brown-out Reset is immediately activated. When V_{CC} increases above the trigger level, the Brown-out Reset is deactivated after a delay. The delay is defined by the user in the same way as the delay of POR signal (see Table 5). The trigger level for the BOD can be selected by the fuse BODLEVEL to be 2.7V (BODLEVEL unprogrammed), or 4.0V (BODLEVEL programmed). The trigger level has a hysteresis of 50 mV to ensure spike-free Brown-out Detection.

The BOD circuit will only detect a drop in V_{CC} if the voltage stays below the trigger level for longer than 3 μ s for trigger level 4.0V, 7 μ s for trigger level 2.7V (typical values).

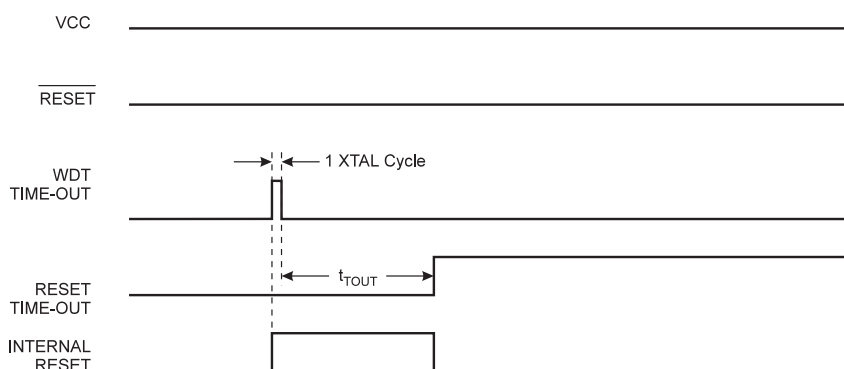
Figure 28. Brown-out Reset during Operation



Watchdog Reset

When the Watchdog times out, it will generate a short reset pulse of one XTAL cycle duration. On the falling edge of this pulse, the delay timer starts counting the Time-out period (t_{TOUT}). See page 43 for details on operation of the Watchdog.

Figure 29. Watchdog Reset during Operation



MCU Status Register – MCUSR

The MCU Status Register provides information on which reset source caused an MCU Reset.

Bit	7	6	5	4	3	2	1	0	
\$34 (\$54)	–	–	–	–	WDRF	BORF	EXTRF	PORF	MCUSR
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0					See Bit Description

- **Bits 7..4 – Res: Reserved Bits**

These bits are reserved bits in the AT90S4433 and always read as zero.

- **Bit 3 – WDRF: Watchdog Reset Flag**

This bit is set if a Watchdog Reset occurs. The bit is cleared by a Power-On Reset, or by writing a logical “0” to the flag.

- **Bit 2 – BORF: Brown-out Reset Flag**

This bit is set if a Brown-out Reset occurs. The bit is cleared by a Power-on Reset, or by writing a logical “0” to the flag.

- **Bit 1 – EXTRF: External Reset Flag**

This bit is set if an External Reset occurs. The bit is cleared by a Power-on Reset, or by writing a logical “0” to the flag.

- **Bit 0 – PORF: Power-on Reset Flag**

This bit is set if a Power-on Reset occurs. The bit is cleared only by writing a logical “0” to the flag.

To make use of the Reset Flags to identify a reset condition, the user should read and then clear the MCUSR as early as possible in the program. If the register is cleared before another reset occurs, the source of the reset can be found by examining the Reset Flags.

Interrupt Handling

The AT90S4433 has two 8-bit Interrupt Mask Control Registers; GIMSK (General Interrupt Mask) Register and TIMSK (Timer/Counter Interrupt Mask) Register.

When an interrupt occurs, the Global Interrupt Enable I-bit is cleared (zero) and all interrupts are disabled. The user software can set (one) the I-bit to enable nested interrupts. The I-bit is set (one) when a Return from Interrupt instruction (RETI) is executed.

When the Program Counter is vectored to the actual Interrupt Vector in order to execute the interrupt handling routine, hardware clears the corresponding flag that generated the interrupt. Some of the interrupt flags can also be cleared by writing a logical “1” to the flag bit position(s) to be cleared.

If an interrupt condition occurs when the corresponding interrupt enable bit is cleared (zero), the Interrupt Flag will be set and remembered until the interrupt is enabled or the flag is cleared by software.

If one or more interrupt conditions occur when the Global Interrupt Enable bit is cleared (zero), the corresponding Interrupt Flag(s) will be set and remembered until the Global Interrupt Enable bit is set (one), and will be executed by order of priority.

Note that external level interrupt does not have a flag and will only be remembered for as long as the interrupt condition is active.

Timer/Counter1 Control Register A – TCCR1A

Bit	7	6	5	4	3	2	1	0	
\$2F (\$4F)	COM11	COM10	–	–	–	–	PWM11	PWM10	TCCR1A
Read/Write	R/W	R/W	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

• Bits 7, 6 – COM11, COM10: Compare Output Mode1, Bits 1, and 0

The COM11 and COM10 control bits determine any output pin action following a Compare Match in Timer/Counter1. Any output pin actions affect pin OC1 (Output Compare pin 1). This is an alternative function to an I/O port, and the corresponding direction control bit must be set (one) to control an output pin. The control configuration is shown in Table 10.

Table 10. Compare 1 Mode Select

COM11	COM10	Description
0	0	Timer/Counter1 disconnected from output pin OC1
0	1	Toggle the OC1 output line.
1	0	Clear the OC1 output line (to zero).
1	1	Set the OC1 output line (to one).

In PWM mode, these bits have a different function. Refer to Table 11 for a detailed description.

• Bits 5..2 – Res: Reserved Bits

These bits are reserved bits in the AT90S4433 and always read as zero.

• Bits 1, 0 – PWM11, PWM10: Pulse Width Modulator Select Bits

These bits select PWM operation of Timer/Counter1 as specified in Table 11. This mode is described on page 41.

Table 11. PWM Mode Select

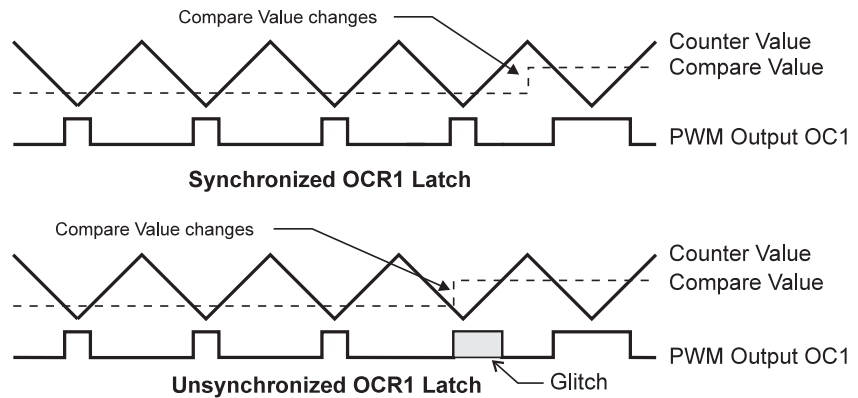
PWM11	PWM10	Description
0	0	PWM operation of Timer/Counter1 is disabled
0	1	Timer/Counter1 is an 8-bit PWM
1	0	Timer/Counter1 is a 9-bit PWM
1	1	Timer/Counter1 is a 10-bit PWM

Table 14. Compare1 Mode Select in PWM Mode

COM11	COM10	Effect on OC1
0	0	Not connected
0	1	Not connected
1	0	Cleared on compare match, up-counting. Set on compare match, down-counting (non-inverted PWM).
1	1	Cleared on compare match, down-counting. Set on compare match, up-counting (inverted PWM).

Note that in the PWM mode, the ten least significant OCR1 bits, when written, are transferred to a temporary location. They are latched when Timer/Counter1 reaches TOP. This prevents the occurrence of odd-length PWM pulses (glitches) in the event of an unsynchronized OCR1 write. See Figure 34 for an example.

Figure 34. Effects on Unsynchronized OCR1 Latching



During the time between the write and the latch operation, a read from OCR1 will read the contents of the temporary location. This means that the most recently written value always will read out of OCR1.

When OCR1 contains \$0000 or TOP, the output OC1 is updated to low or high on the next compare match according to the settings of COM11 and COM10. This is shown in Table 15.

Table 15. PWM Outputs OCR = \$0000 or TOP

COM11	COM10	OCR1	Output OC1
1	0	\$0000	L
1	0	TOP	H
1	1	\$0000	H
1	1	TOP	L

In PWM mode, the Timer Overflow Flag1 (TOV1) is set when the counter changes direction at \$0000. Timer Overflow Interrupt1 operates exactly as in normal Timer/Counter mode, i.e., it is executed when TOV1 is set, provided that Timer Overflow Interrupt1 and global interrupts are enabled. This also applies to the Timer Output Compare1 Flag and interrupt.

- **Bits 2..0 – WDP2, WDP1, WDP0: Watchdog Timer Prescaler 2, 1, and 0**

The WDP2, WDP1, and WDP0 bits determine the Watchdog Timer prescaling when the Watchdog Timer is enabled. The different prescaling values and their corresponding time-out periods are shown in Table 16.

Table 16. Watchdog Timer Prescale Select⁽¹⁾

WDP2	WDP1	WDP0	Number of WDT Oscillator Cycles	Typical Time-out at V _{CC} = 3.0V	Typical Time-out at V _{CC} = 5.0V
0	0	0	16K cycles	47 ms	15 ms
0	0	1	32K cycles	94 ms	30 ms
0	1	0	64K cycles	0.19 s	60 ms
0	1	1	128K cycles	0.38 s	0.12 s
1	0	0	256K cycles	0.75 s	0.24 s
1	0	1	512K cycles	1.5 s	0.49 s
1	1	0	1,024K cycles	3.0 s	0.97 s
1	1	1	2,048K cycles	6.0 s	1.9 s

Note: 1. The frequency of the Watchdog Oscillator is voltage dependent, as shown in the Electrical Characteristics section.

The WDR (Watchdog Reset) instruction should always be executed before the Watchdog Timer is enabled. This ensures that the reset period will be in accordance with the Watchdog Timer prescale settings. If the Watchdog Timer is enabled without reset, the Watchdog Timer may not start counting from zero.

To avoid unintentional MCU reset, the Watchdog Timer should be disabled or Reset before changing the Watchdog Timer Prescale Select.

- **Bit 4 – FE: Framing Error**

This bit is set if a Framing Error condition is detected, i.e., when the stop bit of an incoming character is zero.

The FE bit is cleared when the stop bit of received data is one.

- **Bit 3 – OR: OverRun**

This bit is set if an OverRun condition is detected, i.e., when a character already present in the UDR Register is not read before the next character has been shifted into the Receiver Shift Register. The OR bit is buffered, which means that it will be set once the valid data still in UDRE is read.

The OR bit is cleared (zero) when data is received and transferred to UDR.

- **Bits 2..1 – Res: Reserved Bits**

These bits are reserved bits in the AT90S4433 and will always read as zero.

- **Bit 0 – MPCM: Multi-processor Communication Mode**

This bit is used to enter Multi-processor Communication mode. The bit is set when the slave MCU waits for an address byte to be received. When the MCU has been addressed, the MCU switches off the MPCM bit and starts data reception.

For a detailed description, see “Multi-processor Communication Mode”.

UART Control and Status Register B – UCSRB

Bit	7	6	5	4	3	2	1	0	
\$0A (\$2A)	RXCIE	TXCIE	UDRIE	RXEN	TXEN	CHR9	RXB8	TXB8	UCSRB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	W	
Initial Value	0	0	0	0	0	0	1	0	

- **Bit 7 – RXCIE: RX Complete Interrupt Enable**

When this bit is set (one), a setting of the RXC bit in UCSRA will cause the Receive Complete Interrupt routine to be executed, provided that global interrupts are enabled.

- **Bit 6 – TXCIE: TX Complete Interrupt Enable**

When this bit is set (one), a setting of the TXC bit in UCSRA will cause the Transmit Complete Interrupt routine to be executed, provided that global interrupts are enabled.

- **Bit 5 – UDRIE: UART Data Register Empty Interrupt Enable**

When this bit is set (one), a setting of the UDRE bit in UCSRA will cause the UART Data Register Empty Interrupt routine to be executed, provided that global interrupts are enabled.

- **Bit 4 – RXEN: Receiver Enable**

This bit enables the UART Receiver when set (one). When the Receiver is disabled, the RXC, OR, and FE status flags cannot become set. If these flags are set, turning off RXEN does not cause them to be cleared.

UART Baud Rate Register – UBRR

Bit	15	14	13	12	11	10	9	8	
\$03 (\$23)	–	–	–	–	MSB			LSB	UBRRHI
\$09 (\$29)	MSB							LSB	UBRR
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

This is a 12-bit register that contains the UART Baud Rate according to the equation on the previous page. The UBRRHI contains the four most significant bits, and the UBRR contains the eight least significant bits of the UART Baud Rate.

Figure 47. ADC Timing Diagram, Single Conversion

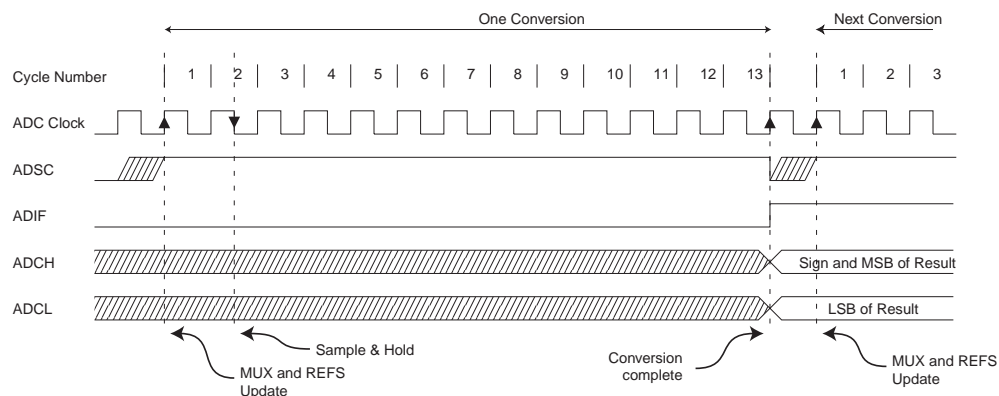
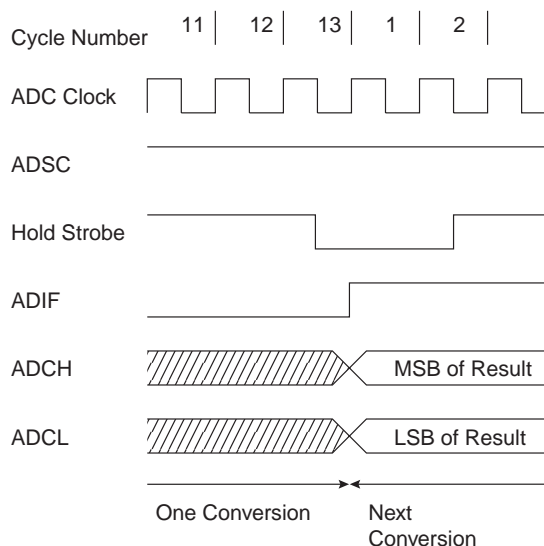


Figure 48. ADC Timing Diagram, Free Run Conversion



ADC Noise Canceler Function

The ADC features a Noise Canceler that enables conversion during Idle mode to reduce noise induced from the CPU core. To make use of this feature, the following procedure should be used:

1. Make sure that the ADC is enabled and is not busy converting. Single Conversion mode must be selected and the ADC conversion complete interrupt must be enabled. Thus:
 $ADEN = 1$
 $ADSC = 0$
 $ADFR = 0$
 $ADIE = 1$
2. Enter Idle mode. The ADC will start a conversion once the CPU has been halted.
3. If no other interrupts occur before the ADC conversion completes, the ADC interrupt will wake up the MCU and execute the ADC conversion complete interrupt routine.

ADC Characteristics $T_A = -40^{\circ}\text{C}$ to 85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Resolution			10		Bits
	Absolute Accuracy	$V_{REF} = 4\text{V}$ ADC clock = 200 kHz		1	2	LSB
	Absolute Accuracy	$V_{REF} = 4\text{V}$ ADC clock = 1 MHz		4		LSB
	Absolute Accuracy	$V_{REF} = 4\text{V}$ ADC clock = 2 MHz		16		LSB
	Integral Non-linearity	$V_{REF} > 2\text{V}$		0.5		LSB
	Differential Non-linearity	$V_{REF} > 2\text{V}$		0.5		LSB
	Zero Error (Offset)			1		LSB
	Conversion Time		65		260	μs
	Clock Frequency		50		200	kHz
AVCC	Analog Supply Voltage		$V_{CC} - 0.3^{(1)}$		$V_{CC} + 0.3^{(2)}$	V
V_{REF}	Reference Voltage		2		AVCC	V
R_{REF}	Reference Input Resistance		6	10	13	k Ω
R_{AIN}	Analog Input Resistance			100		M Ω

Notes: 1. Minimum for AVCC is 2.7V.
2. Maximum for AVCC is 6.0V.

Figure 58. Port D Schematic Diagram (Pin PD1)

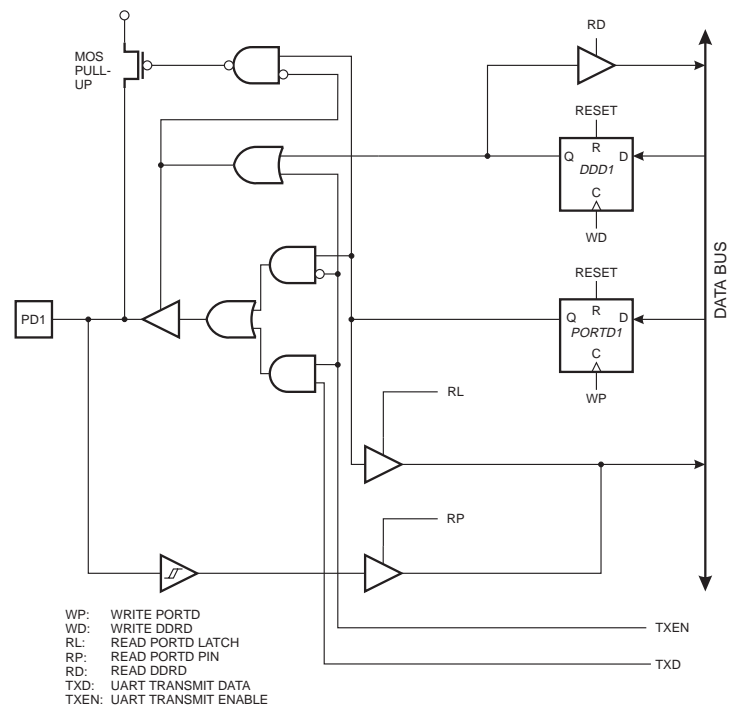


Figure 59. Port D Schematic Diagram (Pins PD2 and PD3)

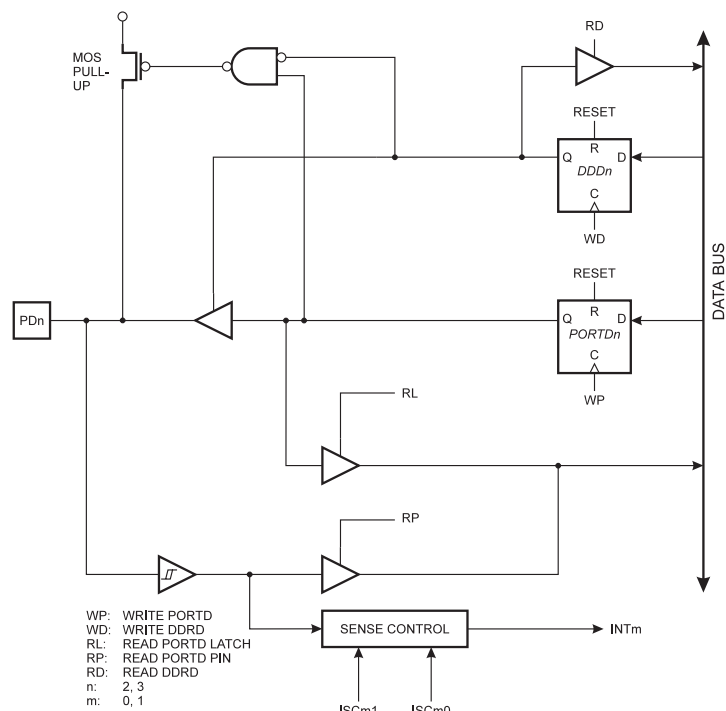


Table 30. Pin Name Mapping

Signal Name in Programming Mode	Pin Name	I/O	Function
RDY/BSY	PD1	O	0: Device is busy programming, 1: Device is ready for new command
\overline{OE}	PD2	I	Output Enable (active low)
\overline{WR}	PD3	I	Write Pulse (active low)
BS	PD4	I	Byte Select ("0" selects Low Byte, "1" selects High Byte)
XA0	PD5	I	XTAL Action Bit 0
XA1	PD6	I	XTAL Action Bit 1
DATA	PC1 - 0, PB5 - 0	I/O	Bi-directional Data Bus (output when \overline{OE} is low)

Table 31. XA1 and XA0 Coding

XA1	XA0	Action when XTAL1 is Pulsed
0	0	Load Flash or EEPROM Address (high or low address byte determined by BS)
0	1	Load Data (high or low data byte for Flash determined by BS)
1	0	Load Command
1	1	No Action, Idle

Table 32. Command Byte Bit Coding

Command Byte	Command Executed
1000 0000	Chip Erase
0100 0000	Write Fuse Bits
0010 0000	Write Lock Bits
0001 0000	Write Flash
0001 0001	Write EEPROM
0000 1000	Read Signature Bytes
0000 0100	Read Fuse and Lock Bits
0000 0010	Read Flash
0000 0011	Read EEPROM

Enter Programming Mode

The following algorithm puts the device in Parallel Programming mode:

1. Apply supply voltage according to Table 29, between V_{CC} and GND.
2. Set the \overline{RESET} and BS pin to "0" and wait at least 100 ns.
3. Apply 11.5 - 12.5V to \overline{RESET} . Any activity on BS within 100 ns after +12V has been applied to \overline{RESET} will cause the device to fail entering Programming mode.

Chip Erase

The Chip Erase command will erase the Flash and EEPROM memories and the Lock bits. The Lock bits are not reset until the Flash and EEPROM have been completely erased. The Fuse bits are not changed. Chip Erase must be performed before the Flash or EEPROM is reprogrammed.

A: Load Command "Chip Erase"

1. Set XA1, XA0 to "10". This enables command loading.
2. Set BS to "0".
3. Set DATA to "1000 0000". This is the command for Chip Erase.
4. Give XTAL1 a positive pulse. This loads the command.
5. Give \overline{WR} a t_{WLWH_CE} wide negative pulse to execute Chip Erase. See Table 33 for t_{WLWH_CE} value. Chip Erase does not generate any activity on the RDY/ \overline{BSY} pin.

Programming the Flash

A: Load Command "Write Flash"

1. Set XA1, XA0 to "10". This enables command loading.
2. Set BS to "0".
3. Set DATA to "0001 0000". This is the command for Write Flash.
4. Give XTAL1 a positive pulse. This loads the command.

B: Load Address High Byte

1. Set XA1, XA0 to "00". This enables address loading.
2. Set BS to "1". This selects High Byte.
3. Set DATA = Address High Byte (\$00 - \$07).
4. Give XTAL1 a positive pulse. This loads the address High Byte.

C: Load Address Low Byte

1. Set XA1, XA0 to "00". This enables address loading.
2. Set BS to "0". This selects Low Byte.
3. Set DATA = Address Low Byte (\$00 - \$FF).
4. Give XTAL1 a positive pulse. This loads the address Low Byte.

D: Load Data Low Byte

1. Set XA1, XA0 to "01". This enables data loading.
2. Set DATA = Data Low Byte (\$00 - \$FF).
3. Give XTAL1 a positive pulse. This loads the data Low Byte.

E: Write Data Low Byte

1. Set BS to "0". This selects low data.
2. Give \overline{WR} a negative pulse. This starts programming of the data byte. RDY/ \overline{BSY} goes low.
3. Wait until RDY/ \overline{BSY} goes high to program the next byte.

(See Figure 63 for signal waveforms.)

F: Load Data High Byte

1. Set XA1, XA0 to "01". This enables data loading.
2. Set DATA = Data High Byte (\$00 - \$FF).
3. Give XTAL1 a positive pulse. This loads the data High Byte.

Figure 71. Active Supply Current vs. V_{CC}

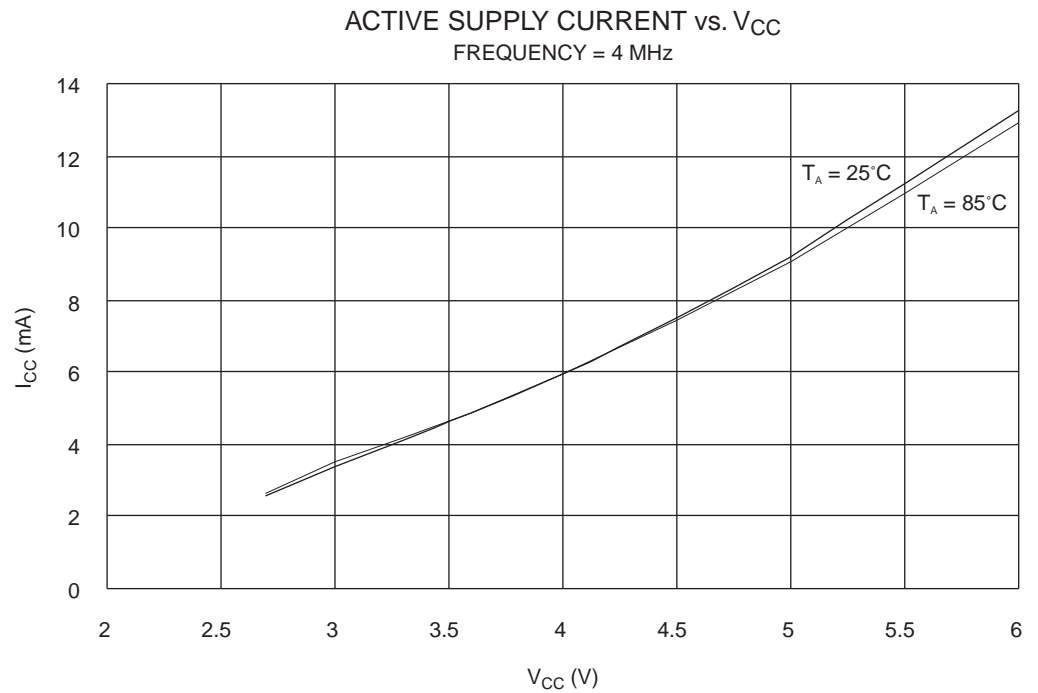


Figure 72. Idle Supply Current vs. Frequency

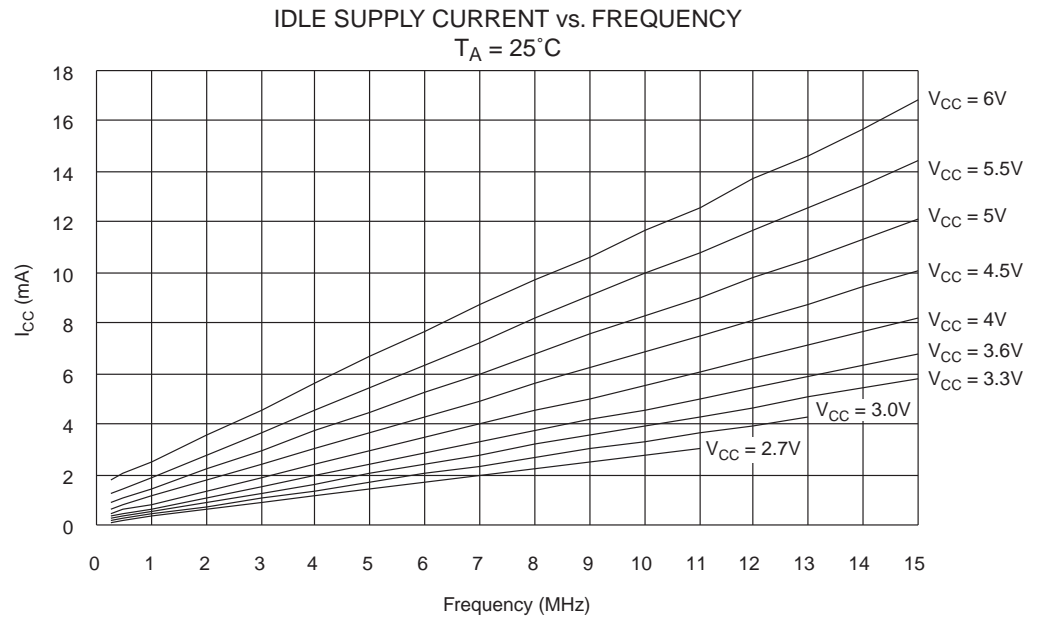


Figure 73. Idle Supply Current vs. V_{CC}

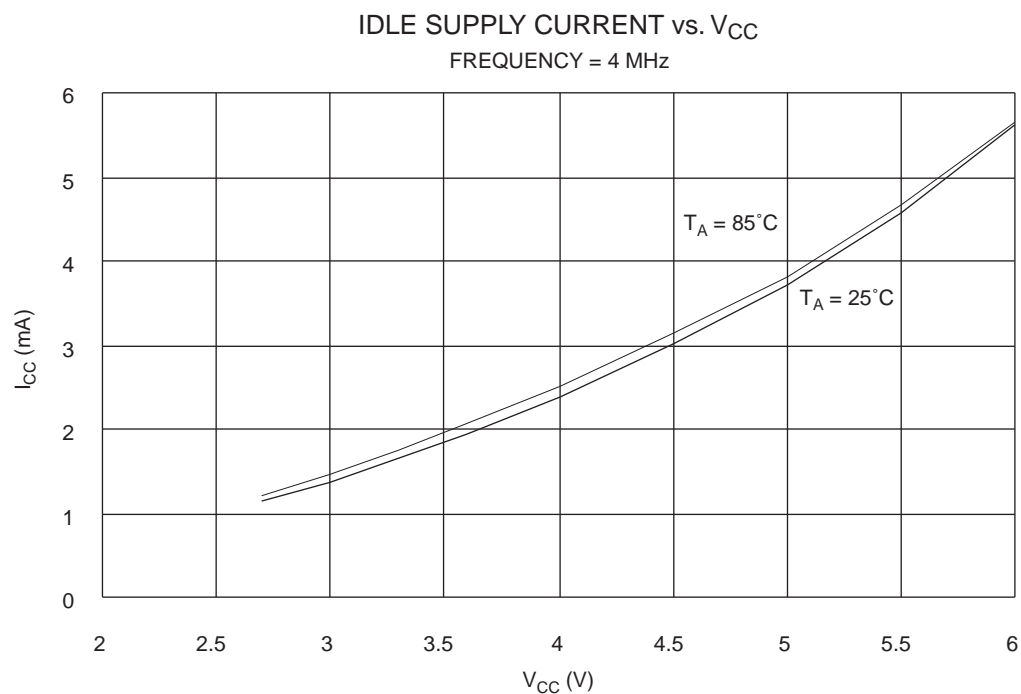


Figure 74. Power-down Supply Current vs. V_{CC}

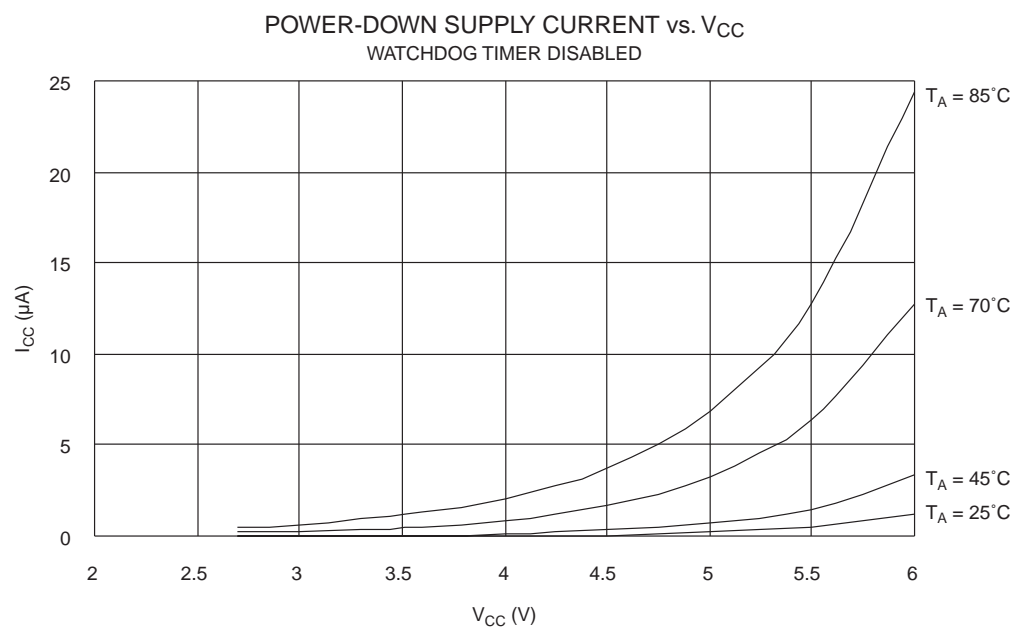


Figure 83. Pull-up Resistor Current vs. Input Voltage

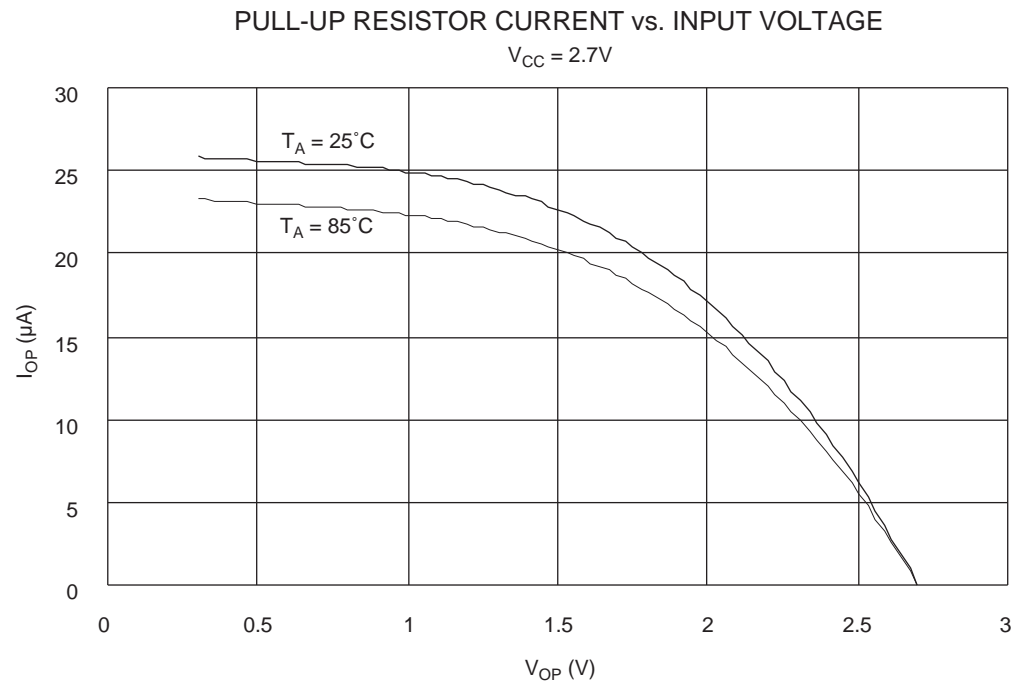


Figure 84. I/O Pin Sink Current vs. Output Voltage

