Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	LED, POR, PWM, WDT
Number of I/O	18
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c5131a-tisil

Typical Application

Recommended External components

All the external components described in the figure below must be implemented as close as possible from the microcontroller package.

The following figure represents the typical wiring schematic.

Figure 4. Typical Application

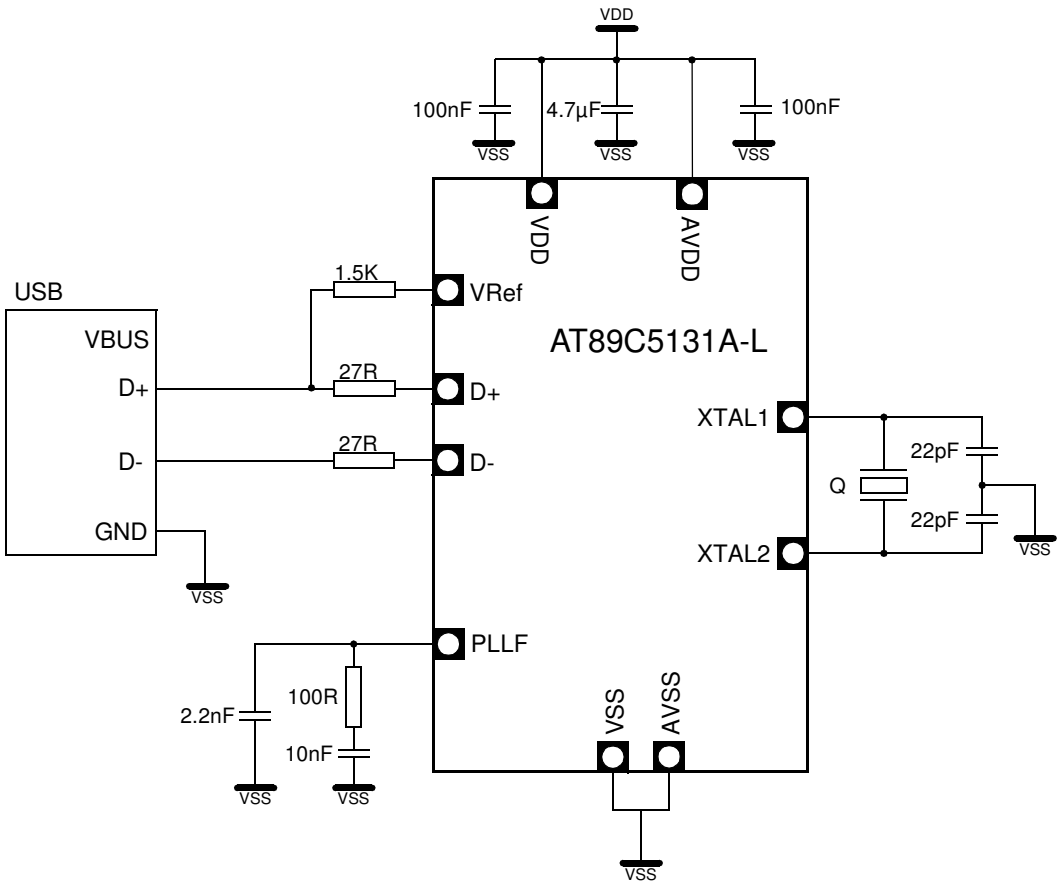


Table 21. Timer SFR's

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
TH0	8Ch	Timer/Counter 0 High byte								
TL0	8Ah	Timer/Counter 0 Low byte								
TH1	8Dh	Timer/Counter 1 High byte								
TL1	8Bh	Timer/Counter 1 Low byte								
TH2	CDh	Timer/Counter 2 High byte								
TL2	CCh	Timer/Counter 2 Low byte								
TCON	88h	Timer/Counter 0 and 1 control	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	Timer/Counter 0 and 1 Modes	GATE1	C/T1#	M11	M01	GATE0	C/T0#	M10	M00
T2CON	C8h	Timer/Counter 2 control	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#
T2MOD	C9h	Timer/Counter 2 Mode							T2OE	DCEN
RCAP2H	CBh	Timer/Counter 2 Reload/Capture High byte								
RCAP2L	CAh	Timer/Counter 2 Reload/Capture Low byte								
WDTRST	A6h	WatchDog Timer Reset								
WDTPRG	A7h	WatchDog Timer Program						S2	S1	S0

Table 22. Serial I/O Port SFR's

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCON	98h	Serial Control	FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	99h	Serial Data Buffer								
SADEN	B9h	Slave Address Mask								
SADDR	A9h	Slave Address								

Table 23. Baud Rate Generator SFR's

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
BRL	9Ah	Baud Rate Reload								
BDRCON	9Bh	Baud Rate Control				BRR	TBCK	RBCK	SPD	SRC

Table 24. PCA SFR's

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CCON	D8h	PCA Timer/Counter Control	CF	CR		CCF4	CCF3	CCF2	CCF1	CCF0
CMOD	D9h	PCA Timer/Counter Mode	CIDL	WDTE				CPS1	CPS0	ECF
CL	E9h	PCA Timer/Counter Low byte								
CH	F9h	PCA Timer/Counter High byte								
CCAPM0 CCAPM1 CCAPM2 CCAPM3 CCAPM4	DAh DBh DCh DDh DEh	PCA Timer/Counter Mode 0 PCA Timer/Counter Mode 1 PCA Timer/Counter Mode 2 PCA Timer/Counter Mode 3 PCA Timer/Counter Mode 4		ECOM0 ECOM1 ECOM2 ECOM3 ECOM4	CAPP0 CAPP1 CAPP2 CAPP3 CAPP4	CAPN0 CAPN1 CAPN2 CAPN3 CAPN4	MAT0 MAT1 MAT2 MAT3 MAT4	TOG0 TOG1 TOG2 TOG3 TOG4	PWM0 PWM1 PWM2 PWM3 PWM4	ECCF0 ECCF1 ECCF2 ECCF3 ECCF4
CCAP0H CCAP1H CCAP2H CCAP3H CCAP4H	FAh FBh FCh FDh FEh	PCA Compare Capture Module 0 H PCA Compare Capture Module 1 H PCA Compare Capture Module 2 H PCA Compare Capture Module 3 H PCA Compare Capture Module 4 H	CCAP0H7 CCAP1H7 CCAP2H7 CCAP3H7 CCAP4H7	CCAP0H6 CCAP1H6 CCAP2H6 CCAP3H6 CCAP4H6	CCAP0H5 CCAP1H5 CCAP2H5 CCAP3H5 CCAP4H5	CCAP0H4 CCAP1H4 CCAP2H4 CCAP3H4 CCAP4H4	CCAP0H3 CCAP1H3 CCAP2H3 CCAP3H3 CCAP4H3	CCAP0H2 CCAP1H2 CCAP2H2 CCAP3H2 CCAP4H2	CCAP0H1 CCAP1H1 CCAP2H1 CCAP3H1 CCAP4H1	CCAP0H0 CCAP1H0 CCAP2H0 CCAP3H0 CCAP4H0
CCAP0L CCAP1L CCAP2L CCAP3L CCAP4L	EAh EBh ECh EDh EEh	PCA Compare Capture Module 0 L PCA Compare Capture Module 1 L PCA Compare Capture Module 2 L PCA Compare Capture Module 3 L PCA Compare Capture Module 4 L	CCAP0L7 CCAP1L7 CCAP2L7 CCAP3L7 CCAP4L7	CCAP0L6 CCAP1L6 CCAP2L6 CCAP3L6 CCAP4L6	CCAP0L5 CCAP1L5 CCAP2L5 CCAP3L5 CCAP4L5	CCAP0L4 CCAP1L4 CCAP2L4 CCAP3L4 CCAP4L4	CCAP0L3 CCAP1L3 CCAP2L3 CCAP3L3 CCAP4L3	CCAP0L2 CCAP1L2 CCAP2L2 CCAP3L2 CCAP4L2	CCAP0L1 CCAP1L1 CCAP2L1 CCAP3L1 CCAP4L1	CCAP0L0 CCAP1L0 CCAP2L0 CCAP3L0 CCAP4L0

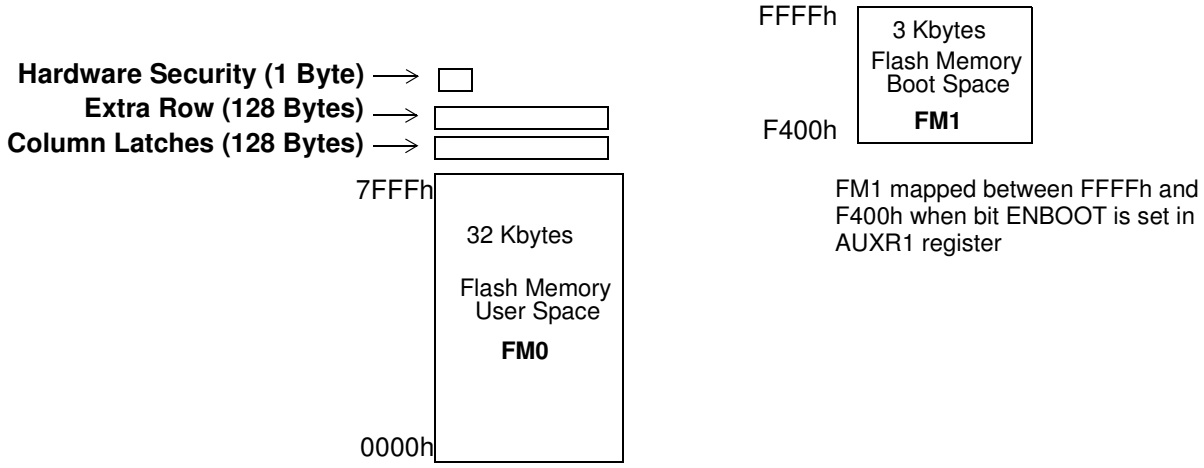
Table 25. Interrupt SFR's

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
IEN0	A8h	Interrupt Enable Control 0	EA	EC	ET2	ES	ET1	EX1	ET0	EX0
IEN1	B1h	Interrupt Enable Control 1		EUSB				ESPI	ETWI	EKB
IPL0	B8h	Interrupt Priority Control Low 0		PPCL	PT2L	PSL	PT1L	PX1L	PT0L	PX0L
IPH0	B7h	Interrupt Priority Control High 0		PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
IPL1	B2h	Interrupt Priority Control Low 1		PUSBL				PSPIL	PTWIL	PKBL
IPH1	B3h	Interrupt Priority Control High 1		PUSBH				PSPIH	PTWIH	PKBH

Table 26. PLL SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
PLLCON	A3h	PLL Control						EXT48	PLLEN	PLOCK
PLLDIV	A4h	PLL Divider	R3	R2	R1	R0	N3	N2	N1	N0

Figure 16. Flash Memory Architecture



FM0 Memory Architecture

The Flash memory is made up of 4 blocks (see Figure 16):

1. The memory array (user space) 32 Kbytes
2. The Extra Row
3. The Hardware security bits
4. The column latch registers

User Space

This space is composed of a 32 Kbytes Flash memory organized in 256 pages of 128 bytes. It contains the user's application code.

Extra Row (XRow)

This row is a part of FM0 and has a size of 128 bytes. The extra row contains information for bootloader usage. (see Table 39.Software Registers, page 39)

Hardware Security Space

The hardware security space is a part of FM0 and has a size of 1 byte.
The 4 MSB can be read/written by software. The 4 LSB can only be read by software and written by hardware in parallel mode.

Column Latches

The column latches, also part of FM0, have a size of full page (128 bytes).
The column latches are the entrance buffers of the three previous memory locations (user array, XRow and Hardware security byte).

Overview of FM0 Operations

The CPU interfaces to the Flash memory through the FCON register and AUXR1 register.

These registers are used to:

- Map the memory spaces in the adressable space
- Launch the programming of the memory spaces
- Get the status of the Flash memory (busy/not busy)
- Select the Flash memory FM0/FM1.

Mapping of the Memory Space

By default, the user space is accessed by MOVC instruction for read only. The column latches space is made accessible by setting the FPS bit in FCON register. Writing is possible from 0000h to 7FFFh, address bits 6 to 0 are used to select an address within a page while bits 14 to 7 are used to select the programming address of the page.

Setting this bit takes precedence on the EXTRAM bit in AUXR register.

Loading the Column Latches

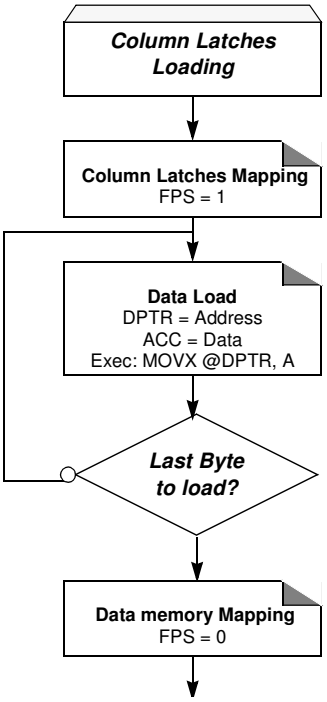
Any number of data from 1 byte to 128 bytes can be loaded in the column latches. This provides the capability to program the whole memory by byte, by page or by any number of bytes in a page.

When programming is launched, an automatic erase of the locations loaded in the column latches is first performed, then programming is effectively done. Thus, no page or block erase is needed and only the loaded data are programmed in the corresponding page.

The following procedure is used to load the column latches and is summarized in Figure 17:

- Map the column latch space by setting FPS bit.
- Load the DPTR with the address to load.
- Load Accumulator register with the data to load.
- Execute the MOVX @DPTR, A instruction.
- If needed loop the three last instructions until the page is completely loaded.

Figure 17. Column Latches Loading Procedure



Programming the Flash Spaces

User

The following procedure is used to program the User space and is summarized in Figure 18:

- Load data in the column latches from address 0000h to 7FFFh(1).
- Disable the interrupts.
- Launch the programming by writing the data sequence 50h followed by A0h in FCON register.
  The end of the programming indicated by the FBUSY flag cleared.
- Enable the interrupts.

Note: 1. The last page address used when loading the column latch is the one used to select the page programming address.

Registers

Table 36. FCON (S:D1h)
Flash Control Register

7	6	5	4	3	2	1	0
FPL3	**FPL2**	**FPL1**	**FPL0**	**FPS**	**FMOD1**	**FMOD0**	**FBUSY**

Bit Number	Bit Mnemonic	Description
7-4	FPL3:0	**Programming Launch Command Bits** Write 5Xh followed by AXh to launch the programming according to FMOD1:0. (see Table 35.)
3	FPS	**Flash Map Program Space** Set to map the column latch space in the data memory space. Clear to re-map the data memory space.
2-1	FMOD1:0	**Flash Mode** See Table 34 or Table 35.
0	FBUSY	**Flash Busy** Set by hardware when programming is in progress. Clear by hardware when programming is done. Can not be cleared by software.

Reset Value = 0000 0000b

Flash Registers and Memory Map

The AT89C5131A-L Flash memory uses several registers:

- Hardware register can be accessed with a parallel programmer.Some bits of the hardware register can be changed, also, by API (i.e. X2 and BLJB bits of Hardware security Byte) or ISP.
- Software registers are in a special page of the Flash memory which can be accessed through the API or with the parallel programming modes. This page, called “Extra Flash Memory”, is not in the internal Flash program memory addressing space.

Hardware Registers

The only hardware register of the AT89C5131A-L is called Hardware Security Byte (HSB).

Table 37. Hardware Security Byte (HSB)

7	6	5	4	3	2	1	0
X2	**BLJB**	**OSCON1**	**OSCON0**	**-**	**LB2**	**LB1**	**LB0**

Bit Number	Bit Mnemonic	Description
7	X2	**X2 Mode** Cleared to force X2 mode (6 clocks per instruction) Set to force X1 mode, Standard Mode (Default).
6	BLJB	**Bootloader Jump Bit** Set this bit to start the user’s application on next reset at address 0000h. Cleared this bit to start the bootloader at address F400h (default).
5-4	OSCON1-0	**Oscillator Control Bits** These two bits are used to control the oscillator in order to reduce consumption. **OSCON1 OSCON0 Description** 1 1 The oscillator is configured to run from 0 to 32 MHz 1 0 The oscillator is configured to run from 0 to 16 MHz 0 1 The oscillator is configured to run from 0 to 8 MHz 0 0 This configuration shouldn’t be set
3	-	**Reserved**
2-0	LB2-0	**User Memory Lock Bits** See Table 38

Bootloader Jump Bit (BLJB)

One bit of the HSB, the BLJB bit, is used to force the boot address:

- When this bit is set the boot address is 0000h.
- When this bit is reset the boot address is F400h. By default, this bit is cleared and the ISP is enabled.

Flash Memory Lock Bits

The three lock bits provide different levels of protection for the on-chip code and data, when programmed as shown in Table 38.

In-System Programming (ISP)

With the implementation of the User Space (FM0) and the Boot Space (FM1) in Flash technology the AT89C5131 allows the system engineer the development of applications with a very high level of flexibility. This flexibility is based on the possibility to alter the customer program at any stages of a product's life:

- Before mounting the chip on the PCB, FM0 flash can be programmed with the application code. FM1 is always preprogrammed by Atmel with a USB bootloader.(1)
- Once the chip is mounted on the PCB, it can be programmed by serial mode via the USB bus.

Note: 1. The user can also program his own bootloader in FM1.

This ISP allows code modification over the total lifetime of the product.

Besides the default Bootloaders Atmel provide customers all the needed Application-Programming-Interfaces (API) which are needed for the ISP. The API are located in the Boot memory.

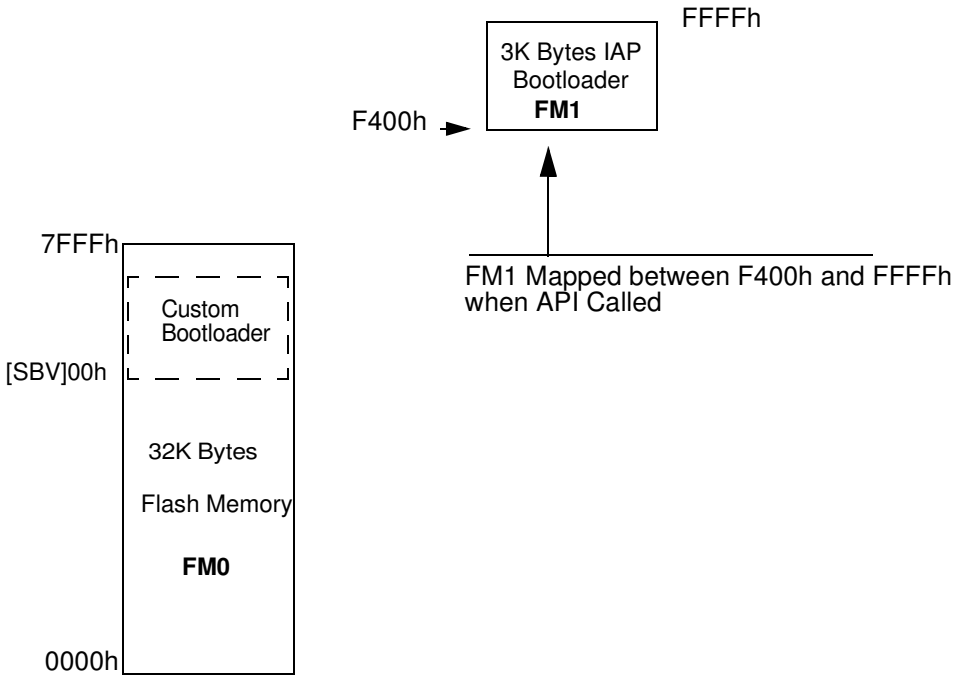
This allow the customer to have a full use of the 32-Kbyte user memory.

Flash Programming and Erasure

There are three methods for programming the Flash memory:

- The Atmel bootloader located in FM1 is activated by the application. Low level API routines (located in FM1)will be used to program FM0. The interface used for serial downloading to FM0 is the USB. API can be called also by user's bootloader located in FM0 at [SBV]00h.
- A further method exist in activating the Atmel boot loader by hardware activation. See the Section "Hardware Registers".
- The FM0 can be programmed also by the parallel mode using a programmer.

Figure 22. Flash Memory Mapping



On-chip Expanded RAM (ERAM)

The AT89C5131A-L provides additional Bytes of random access memory (RAM) space for increased data parameters handling and high level language usage.

AT89C5131A-L devices have an expanded RAM in the external data space; maximum size and location are described in Table 44.

Table 44. Description of Expanded RAM

Part Number	ERAM Size	Address	
		Start	End
AT89C5131A-L	1024	00h	3FFh

The AT89C5131A-L has on-chip data memory which is mapped into the following four separate segments.

1. The Lower 128 bytes of RAM (addresses 00h to 7Fh) are directly and indirectly addressable.
2. The Upper 128 bytes of RAM (addresses 80h to FFh) are indirectly addressable only.
3. The Special Function Registers, SFRs, (addresses 80h to FFh) are directly addressable only.
4. The expanded RAM bytes are indirectly accessed by MOVX instructions, and with the EXTRAM bit cleared in the AUXR register (see Table 44)

The lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

Figure 25. Internal and External Data Memory Address

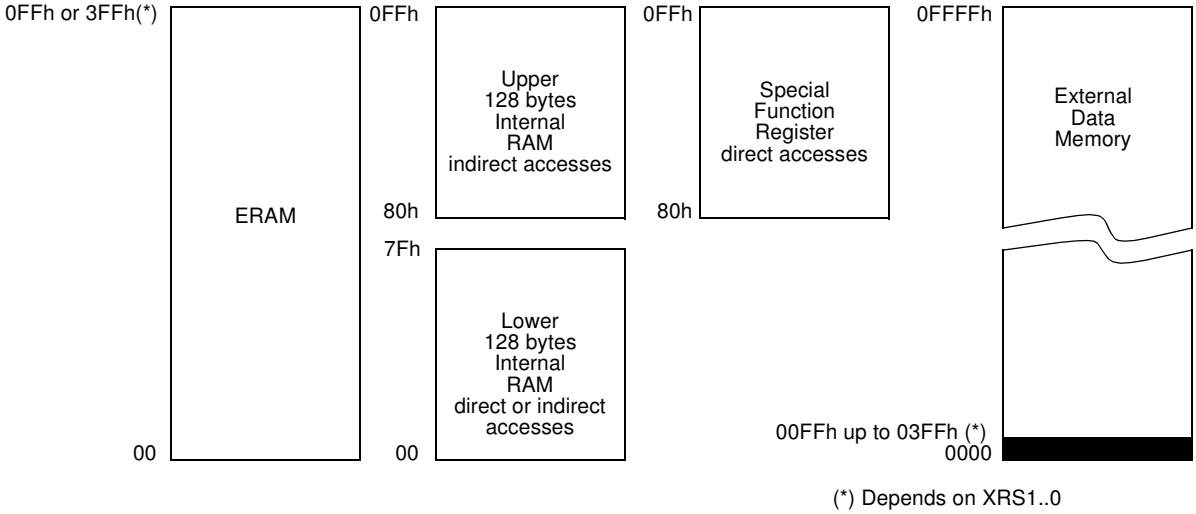


Table 45. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
DPU	**-**	**M0**	**-**	**XRS1**	**XRS0**	**EXTRAM**	**AO**

Bit Number	Bit Mnemonic	Description
7	DPU	**Disable Weak Pull Up** Cleared to enabled weak pull up on standard Ports. Set to disable weak pull up on standard Ports.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit
5	M0	**Pulse length** Cleared to stretch MOVX control: the $\overline{RD}$ and the $\overline{WR}$ pulse length is 6 clock periods (default). Set to stretch MOVX control: the $\overline{RD}$ and the $\overline{WR}$ pulse length is 30 clock periods.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit
3	XRS1	**ERAM Size** **XRS1 XRS0 — ERAM size** 0 0 — 256 bytes 0 1 — 512 bytes 1 0 — 768 bytes 1 1 — 1024 bytes (default)
2	XRS0	
1	EXTRAM	**EXTRAM bit** Cleared to access internal ERAM using MOVX at $\overline{Ri}$ at DPTR. Set to access external memory.
0	AO	**ALE Output bit** Cleared, ALE is emitted at a constant rate of 1/6 the oscillator frequency (or 1/3 if X2 mode is used) (default). Set, ALE is active only when a MOVX or MOVC instruction is used.

Reset Value = 0X0X 1100b

Not bit addressable

the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition.

- The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function.

Table 51 shows the CCAPMn settings for the various PCA functions.

Table 50. CCAPMn Registers (n = 0-4)

CCAPM0 - PCA Module 0 Compare/Capture Control Register (0DAh)
CCAPM1 - PCA Module 1 Compare/Capture Control Register (0DBh)
CCAPM2 - PCA Module 2 Compare/Capture Control Register (0DCh)
CCAPM3 - PCA Module 3 Compare/Capture Control Register (0DDh)
CCAPM4 - PCA Module 4 Compare/Capture Control Register (0DEh)

7	6	5	4	3	2	1	0
-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	ECOMn	**Enable Comparator** Cleared to disable the comparator function. Set to enable the comparator function.
5	CAPPn	**Capture Positive** Cleared to disable positive edge capture. Set to enable positive edge capture.
4	CAPNn	**Capture Negative** Cleared to disable negative edge capture. Set to enable negative edge capture.
3	MATn	**Match** When MATn = 1, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
2	TOGn	**Toggle** When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
1	PWMn	**Pulse Width Modulation Mode** Cleared to disable the CEXn pin to be used as a pulse width modulated output. Set to enable the CEXn pin to be used as a pulse width modulated output.
0	ECCFn	**Enable CCF Interrupt** Cleared to disable compare/capture flag CCFn in the CCON register to generate an interrupt. Set to enable compare/capture flag CCFn in the CCON register to generate an interrupt.

Reset Value = X000 0000b
Not bit addressable

BRL - Baud Rate Reload Register for the internal baud rate generator, UART (9Ah)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

Reset Value = 0000 0000b

Table 57. T2CON Register

T2CON - Timer 2 Control Register (C8h)

7	6	5	4	3	2	1	0
TF2	**EXF2**	**RCLK**	**TCLK**	**EXEN2**	**TR2**	**C/T2#**	**CP/RL2#**

Bit Number	Bit Mnemonic	Description
7	TF2	**Timer 2 overflow Flag** Must be cleared by software. Set by hardware on Timer 2 overflow, if RCLK = 0 and TCLK = 0.
6	EXF2	**Timer 2 External Flag** Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2 = 1. When set, causes the CPU to vector to Timer 2 interrupt routine when Timer 2 interrupt is enabled. Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1)
5	RCLK	**Receive Clock bit for UART** Cleared to use Timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use Timer 2 overflow as receive clock for serial port in mode 1 or 3.
4	TCLK	**Transmit Clock bit for UART** Cleared to use Timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use Timer 2 overflow as transmit clock for serial port in mode 1 or 3.
3	EXEN2	**Timer 2 External Enable bit** Cleared to ignore events on T2EX pin for Timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if Timer 2 is not used to clock the serial port.
2	TR2	**Timer 2 Run control bit** Cleared to turn off Timer 2. Set to turn on Timer 2.
1	C/T2#	**Timer/Counter 2 select bit** Cleared for timer operation (input from internal clock system: $F_{CLK\ PERIPH}$). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.
0	CP/RL2#	**Timer 2 Capture/Reload bit** If RCLK = 1 or TCLK = 1, CP/RL2# is ignored and timer is forced to Auto-reload on Timer 2 overflow. Cleared to Auto-reload on Timer 2 overflows or negative transitions on T2EX pin if EXEN2 = 1. Set to capture on negative transitions on T2EX pin if EXEN2 = 1.

Reset Value = 0000 0000b
Bit addressable

Interrupt Sources and Vector Addresses

Table 67. Vector Table

Number	Polling Priority	Interrupt Source	Interrupt Request	Vector Address
0	0	Reset		0000h
1	1	INT0	IE0	0003h
2	2	Timer 0	TF0	000Bh
3	3	INT1	IE1	0013h
4	4	Timer 1	IF1	001Bh
5	6	UART	RI+TI	0023h
6	7	Timer 2	TF2+EXF2	002Bh
7	5	PCA	CF + CCFn (n = 0-4)	0033h
8	8	Keyboard	KBDIT	003Bh
9	9	TWI	TWIIT	0043h
10	10	SPI	SPIIT	004Bh
11	11			0053h
12	12			005Bh
13	13			0063h
14	14	USB	UEPINT + USBINT	006Bh
15	15			0073h

Registers

Table 86. SSCON Register

SSCON - Synchronous Serial Control Register (93h)

7	6	5	4	3	2	1	0
CR2	SSIE	STA	STO	SI	AA	CR1	CR0

Bit Number	Bit Mnemonic	Description
7	CR2	**Control Rate bit 2** See .
6	SSIE	**Synchronous Serial Interface Enable bit** Clear to disable SSLC. Set to enable SSLC.
5	STA	**Start flag** Set to send a START condition on the bus.
4	ST0	**Stop flag** Set to send a STOP condition on the bus.
3	SI	**Synchronous Serial Interrupt flag** Set by hardware when a serial interrupt is requested. Must be cleared by software to acknowledge interrupt.
2	AA	**Assert Acknowledge flag** Clear in master and slave receiver modes, to force a not acknowledge (high level on SDA). Clear to disable SLA or GCA recognition. Set to recognise SLA or GCA (if GC set) for entering slave receiver or transmitter modes. Set in master and slave receiver modes, to force an acknowledge (low level on SDA). This bit has no effect when in master transmitter mode.
1	CR1	**Control Rate bit 1** See Table 80
0	CR0	**Control Rate bit 0** See Table 80

Table 87. SSDAT (095h) - Synchronous Serial Data Register (read/write)

SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
7	6	5	4	3	2	1	0

Bit Number	Bit Mnemonic	Description
7	SD7	Address bit 7 or Data bit 7.
6	SD6	Address bit 6 or Data bit 6.
5	SD5	Address bit 5 or Data bit 5.
4	SD4	Address bit 4 or Data bit 4.
3	SD3	Address bit 3 or Data bit 3.
2	SD2	Address bit 2 or Data bit 2.

- Endpoint enable

  Before using an endpoint, this one will be enabled by setting the EPEN bit in the UEPCONX register.

  An endpoint which is not enabled won't answer to any USB request. The Default Control Endpoint (Endpoint 0) will always be enabled in order to answer to USB standard requests.

- Endpoint type configuration

  All Standard Endpoints can be configured in Control, Bulk, Interrupt or Isochronous mode. The Ping-pong Endpoints can be configured in Bulk, Interrupt or Isochronous mode. The configuration of an endpoint is performed by setting the field EPTYPE with the following values:

  – Control:EPTYPE = 00b
  – Isochronous:EPTYPE = 01b
  – Bulk:EPTYPE = 10b
  – Interrupt:EPTYPE = 11b

  The Endpoint 0 is the Default Control Endpoint and will always be configured in Control type.

- Endpoint direction configuration

  For Bulk, Interrupt and Isochronous endpoints, the direction is defined with the EPDIR bit of the UEPCONX register with the following values:

  – IN:EPDIR = 1b
  – OUT:EPDIR = 0b

  For Control endpoints, the EPDIR bit has no effect.

- Summary of Endpoint Configuration:

  Do not forget to select the correct endpoint number in the UEPNUM register before accessing to endpoint specific registers.

Table 90. Summary of Endpoint Configuration

Endpoint Configuration	EPEN	EPDIR	EPTYPE	UEPCONX
Disabled	0b	Xb	XXb	0XXX XXXb
Control	1b	Xb	00b	80h
Bulk-in	1b	1b	10b	86h
Bulk-out	1b	0b	10b	82h
Interrupt-In	1b	1b	11b	87h
Interrupt-Out	1b	0b	11b	83h
Isochronous-In	1b	1b	01b	85h
Isochronous-Out	1b	0b	01b	81h

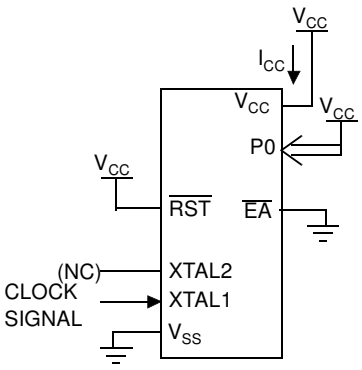
Table 98. UEPSTAX (S:CEh) USB Endpoint X Status Register

7	6	5	4	3	2	1	0
DIR	RXOUTB1	STALLRQ	TXRDY	STL/CRC	RXSETUP	RXOUTB0	TXCMP

Bit Number	Bit Mnemonic	Description
7	DIR	**Control Endpoint Direction** This bit is used only if the endpoint is configured in the control type (seeSection “UEPCONX Register UEPCONX (S:D4h) USB Endpoint X Control Register”). This bit determines the Control data and status direction. The device firmware will set this bit ONLY for the IN data stage, before any other USB operation. Otherwise, the device firmware will clear this bit.
6	RXOUTB1	**Received OUT Data Bank 1 for Endpoints 4, 5 and 6 (Ping-pong mode)** This bit is set by hardware after a new packet has been stored in the endpoint FIFO data bank 1 (only in Ping-pong mode). Then, the endpoint interrupt is triggered if enabled (see“UEPINT Register UEPINT (S:F8h read-only) USB Endpoint Interrupt Register” on page 145) and all the following OUT packets to the endpoint bank 1 are rejected (NAK’ed) until this bit has been cleared, excepted for Isochronous Endpoints. This bit will be cleared by the device firmware after reading the OUT data from the endpoint FIFO.
5	STALLRQ	**Stall Handshake Request** Set this bit to request a STALL answer to the host for the next handshake.Clear this bit otherwise. For CONTROL endpoints: cleared by hardware when a valid SETUP PID is received.
4	TXRDY	**TX Packet Ready** Set this bit after a packet has been written into the endpoint FIFO for IN data transfers. Data will be written into the endpoint FIFO only after this bit has been cleared. Set this bit without writing data to the endpoint FIFO to send a Zero Length Packet. This bit is cleared by hardware, as soon as the packet has been sent for Isochronous endpoints, or after the host has acknowledged the packet for Control, Bulk and Interrupt endpoints. When this bit is cleared, the endpoint interrupt is triggered if enabled (see“UEPINT Register UEPINT (S:F8h read-only) USB Endpoint Interrupt Register” on page 145).
3	STLCRC	**Stall Sent/CRC error flag** - For Control, Bulk and Interrupt Endpoints: This bit is set by hardware after a STALL handshake has been sent as requested by STALLRQ. Then, the endpoint interrupt is triggered if enabled (see“UEPINT Register UEPINT (S:F8h read-only) USB Endpoint Interrupt Register” on page 145) It will be cleared by the device firmware. - For Isochronous Endpoints **(Read-Only)**: This bit is set by hardware if the last received data is corrupted (CRC error on data). This bit is updated by hardware when a new data is received.
2	RXSETUP	**Received SETUP** This bit is set by hardware when a valid SETUP packet has been received from the host. Then, all the other bits of the register are cleared by hardware and the endpoint interrupt is triggered if enabled (see“UEPINT Register UEPINT (S:F8h read-only) USB Endpoint Interrupt Register” on page 145). It will be cleared by the device firmware after reading the SETUP data from the endpoint FIFO.
1	RXOUTB0	**Received OUT Data Bank 0** (see also RXOUTB1 bit for Ping-pong Endpoints) This bit is set by hardware after a new packet has been stored in the endpoint FIFO data bank 0. Then, the endpoint interrupt is triggered if enabled (see“UEPINT Register UEPINT (S:F8h read-only) USB Endpoint Interrupt Register” on page 145) and all the following OUT packets to the endpoint bank 0 are rejected (NAK’ed) until this bit has been cleared, excepted for Isochronous Endpoints. However, for control endpoints, an early SETUP transaction may overwrite the content of the endpoint FIFO, even if its Data packet is received while this bit is set. This bit will be cleared by the device firmware after reading the OUT data from the endpoint FIFO.
0	TXCMPL	**Transmitted IN Data Complete** This bit is set by hardware after an IN packet has been transmitted for Isochronous endpoints and after it has been accepted (ACK’ed) by the host for Control, Bulk and Interrupt endpoints. Then, the endpoint interrupt is triggered if enabled (see“UEPINT Register UEPINT (S:F8h read-only) USB Endpoint Interrupt Register” on page 145). This bit will be cleared by the device firmware before setting TXRDY.

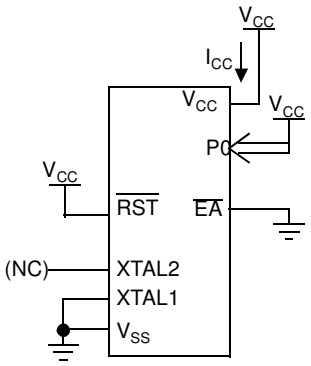
Reset Value = 00h

Figure 79. I_{CC} Test Condition, Idle Mode



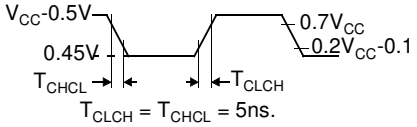
All other pins are disconnected.

Figure 80. I_{CC} Test Condition, Power-down Mode



All other pins are disconnected.

Figure 81. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes



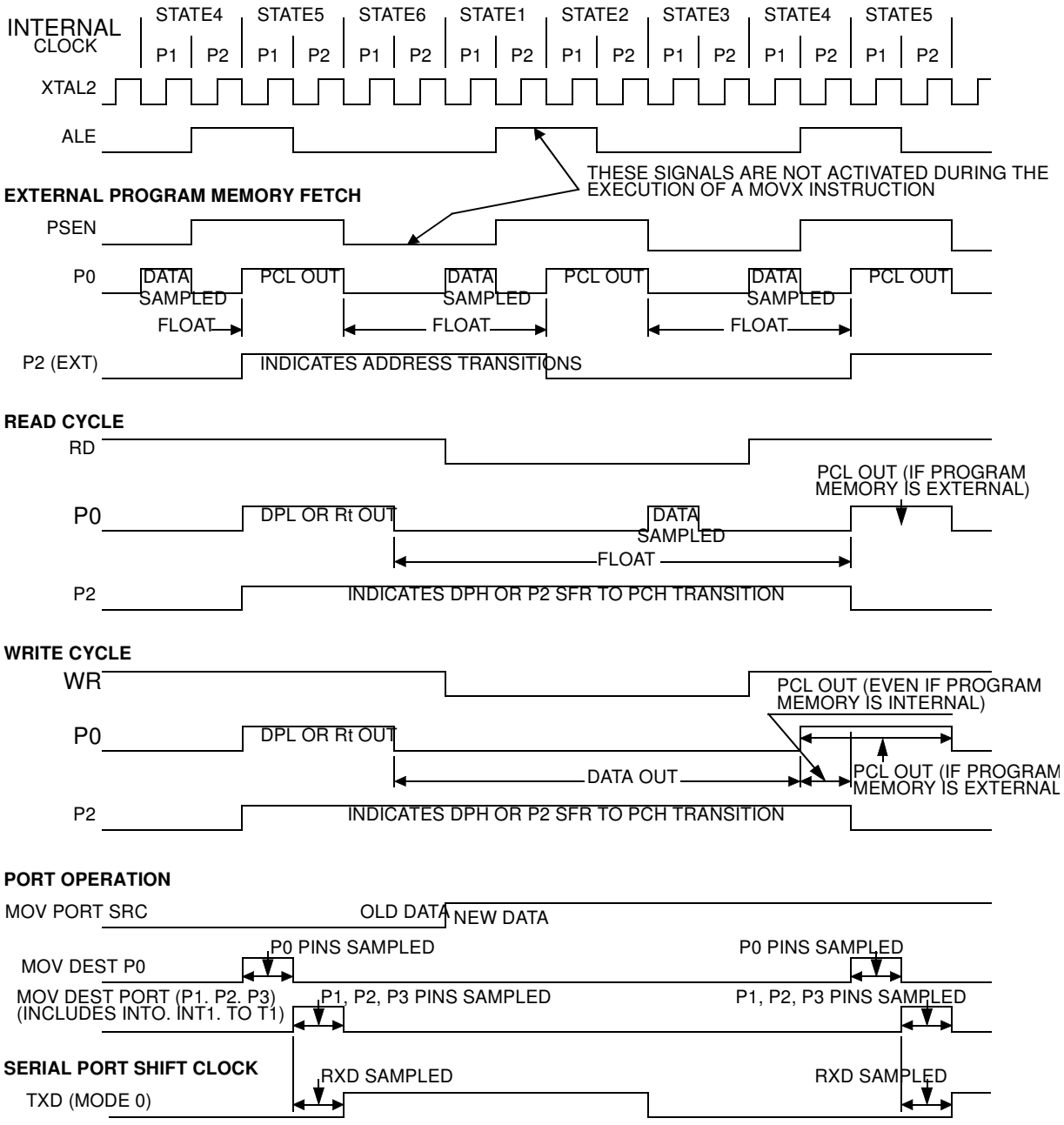
LED's

Table 113. LED Outputs DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{OL}	Output Low Current, P3.6 and P3.7 LED modes	1	2	4	mA	2 mA configuration
		2	4	8	mA	4 mA configuration
		5	10	20	mA	10 mA configuration

Note: 1. (T_A = -20°C to +50°C, V_{CC} - V_{OL} = 2 V ± 20%)

Clock Waveforms Valid in normal clock mode. In X2 mode XTAL2 must be changed to XTAL2/2.



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A = 25°C fully loaded) $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

USB AC Parameters

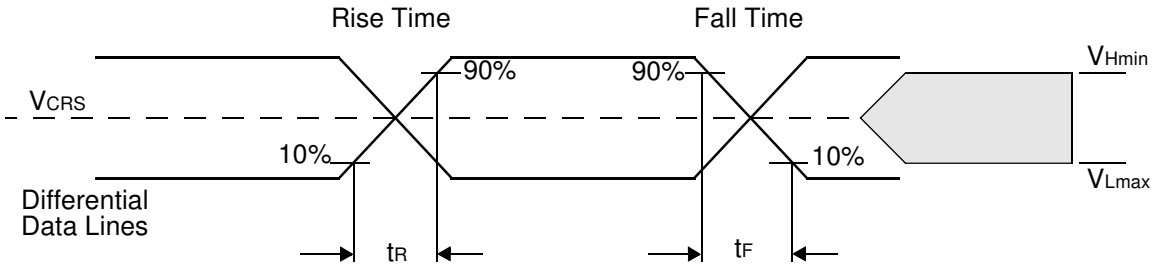


Table 126. USB AC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_R	Rise Time	4		20	ns	
t_F	Fall Time	4		20	ns	
t_{FDRATE}	Full-speed Data Rate	11.9700		12.0300	Mb/s	
V_{CRS}	Crossover Voltage	1.3		2.0	V	
t_{DJ1}	Source Jitter Total to Next Transaction	-3.5		3.5	ns	
t_{DJ2}	Source Jitter Total for Paired Transactions	-4		4	ns	
t_{JR1}	Receiver Jitter to Next Transaction	-18.5		18.5	ns	
t_{JR2}	Receiver Jitter for Paired Transactions	-9		9	ns	

SPI Interface AC Parameters

Definition of Symbols

Table 127. SPI Interface Timing Symbol Definitions

Signals	
C	Clock
I	Data In
O	Data Out

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Ordering Information

Table 129. Possible Order Entries

Part Number	Memory Size (Kbytes)	Supply Voltage	Temperature Range	Package	Packing
AT89C5131A-RDTIL	32	3.0 to 3.6V	Industrial	VQFP64	Tray
AT89C5131A-S3SIL	32	3.0 to 3.6V	Industrial	PLCC52	Stick
AT89C5131A-TISIL	32	3.0 to 3.6V	Industrial	SO28	Stick
AT89C5131A-RDTUL	32	3.0 to 3.6V	Industrial & Green	VQFP64	Tray
AT89C5131A-S3SUL	32	3.0 to 3.6V	Industrial & Green	PLCC52	Stick
AT89C5131A-TISUL	32	3.0 to 3.6V	Industrial & Green	SO28	Stick

Note: 1. Optional Packing and Package options (please consult Atmel sales representative):
-Tape and Reel
-Dry Pack
-Known good dice