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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	2 Core, 64-Bit
Speed	1.3GHz
Co-Processors/DSP	ARM® Cortex®-M4
RAM Controllers	DDR3L, DDR4, LPDDR4
Graphics Acceleration	Yes
Display & Interface Controllers	eDP, HDMI, MIPI-CSI, MIPI-DSI
Ethernet	GbE
SATA	-
USB	USB 3.0 (2)
Voltage - I/O	-
Operating Temperature	-40°C ~ 105°C (TJ)
Security Features	ARM TZ, CAAM, HAB, RDC, RTC, SJC, SNVS
Package / Case	621-FBGA, FCBGA
Supplier Device Package	621-FCPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mimx8md6cvahzaa

1.1 Block diagram

Figure 1 shows the functional modules in the i.MX 8M Dual / 8M QuadLite / 8M Quad processor system.

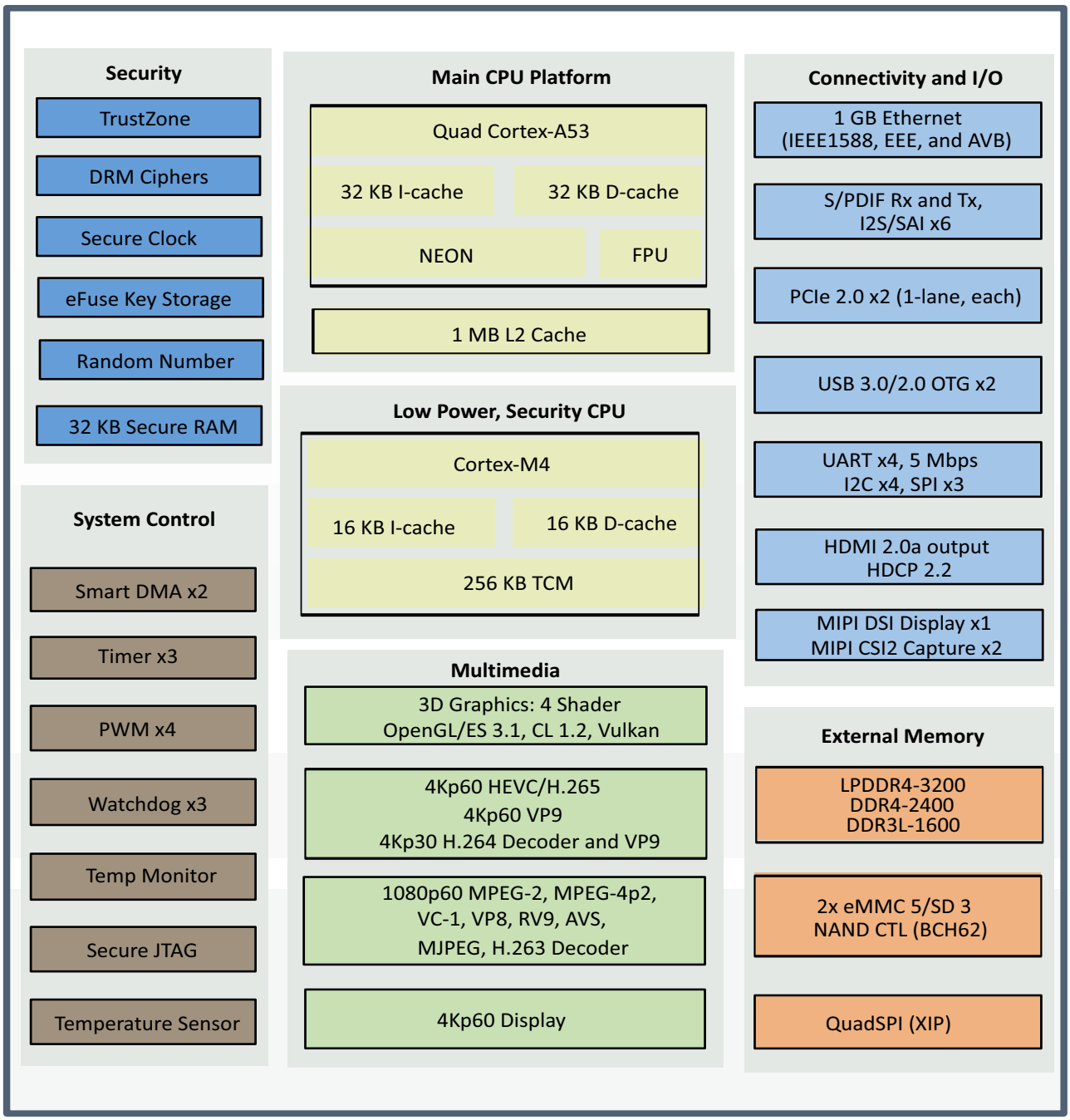

Figure 1. i.MX 8M Dual / 8M QuadLite / 8M Quad system block diagram

1.2 Ordering information

Table 2 shows examples of orderable sample part numbers covered by this data sheet. This table does not include all possible orderable part numbers. If your desired part number is not listed in the table, or you have questions about available parts, contact your NXP representative.

Table 2. Orderable part numbers

Part number[1]	Options	Cortex-A53 CPU speed grade	Qualification tier	Temperature T_j (°C)	Package
MIMX8MQ7CVAHZAA	8M Quad	1.3 GHz	Industrial	-40 to +105	17 x 17 mm, 0.65 mm pitch, FBGA
MIMX8MQ6CVAHZAA	8M Quad	1.3 GHz	Industrial	-40 to +105	17 x 17 mm, 0.65 mm pitch, FBGA
MIMX8MD7CVAHZAA	8M Dual	1.3 GHz	Industrial	-40 to +105	17 x 17 mm, 0.65 mm pitch, FBGA
MIMX8MD6CVAHZAA	8M Dual	1.3 GHz	Industrial	-40 to +105	17 x 17 mm, 0.65 mm pitch, FBGA
MIMX8MQ5CVAHZAA	8M Quad Lite	1.3 GHz	Industrial	-40 to +105	17 x 17 mm, 0.65 mm pitch, FBGA

1 Part number requires a Dolby Vision™ license from Dolby.

Figure 2 describes the part number nomenclature so that the users can identify the characteristics of the specific part number.

Contact an NXP representative for additional details.

Table 3. i.MX 8M Dual / 8M QuadLite / 8M Quad modules list (continued)

Block mnemonic	Block name	Brief description
SDMA	Smart Direct Memory Access	The SDMA is a multichannel flexible DMA engine. It helps in maximizing system performance by offloading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between Arm and SDMA • Very fast Context-Switching with 2-level priority based preemptive multi tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unidirectional and bidirectional flows (Copy mode) • Up to 8-word buffer for configurable burst transfers for EMIv2.5 • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	Secure JTAG Controller	The SJC provides JTAG interface (designed to be compatible with JTAG TAP standards) to internal logic. The i.MX 8M Dual / 8M QuadLite / 8M Quad processors use JTAG port for production, testing, and system debugging. Additionally, the SJC provides BSR (Boundary Scan Register) standard support, designed to be compatible with IEEE 1149.1 and IEEE 1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The SJC of the i.MX 8M Dual / 8M QuadLite / 8M Quad incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, and Master Key Control.
SPDIF1 SPDIF2	Sony Philips Digital Interconnect Format	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality.
TEMPSENSOR	Temperature Sensor	Temperature sensor
TZASC	Trust-Zone Address Space Controller	The TZASC (TZC-380 by Arm) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART1 UART2 UART3 UART4	UART Interface	Each of the UARTv2 modules supports the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud

Table 3. i.MX 8M Dual / 8M QuadLite / 8M Quad modules list (continued)

Block mnemonic	Block name	Brief description
uSDHC1 uSDHC2	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	The i.MX 8M Dual / 8M QuadLite / 8M Quad SoC characteristics: All the MMC/SD/SDIO controller IPs are based on the uSDHC IP. They are designed to support: • SD/SDIO standard, up to version 3.0. • MMC standard, up to version 5.0. • 1.8 V and 3.3 V operation, but do not support 1.2 V operation. • 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit/8-bit MMC mode. One uSDHC controller (SD1) can support up to an 8-bit interface, the other controller (SD2) can only support up to a 4-bit interface.
USB 3.0/2.0	2x USB 3.0/2.0 controllers and PHYs	Two USB controllers and PHYs that support USB 3.0 and USB 2.0. Each USB instance contains: • USB 3.0 core, which can operate in both 3.0 and 2.0 mode
VPU	Video Processing Unit	A high performing video processing unit (VPU), which covers many SD-level and HD-level video decoders. See the *i.MX 8M Quad Applications Processor Reference Manual* (IMX8MDQLQRM) for a complete list of the VPU's decoding and encoding capabilities.
WDOG1 WDOG2 WDOG3	Watchdog	The watchdog (WDOG) timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.
XTALOSC	Crystal Oscillator interface	The XTALOSC module enables connectivity to an external crystal oscillator device.

2.1 Recommended connections for unused interfaces

The recommended connections for unused analog interfaces can be found in the Section, "Unused Input/Output Terminations," in the hardware development guide for the device.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

3.1.3 Operating ranges

Table 7 provides the operating ranges of the i.MX 8M Dual / 8M QuadLite / 8M Quad processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processor Reference Manual* (IMX8MDQLQRM).

Table 7. Operating ranges

Parameter description	Symbol	Min	Typ	Max[1]	Unit	Comment
Power supply for Quad-A53	VDD_ARM	0.81	0.9	1.05	V	Nominal mode—the maximum Arm core frequency supported in this mode is 800 MHz.
		0.9	1.0	1.05	V	Overdrive mode—the maximum Arm core frequency supported in this mode is defined in Table 2.
Power supply for SoC logic	VDD_SOC	0.9	0.95	0.99	V	—
Power supply for GPU	VDD_GPU	0.81	0.9	1.05	V	Nominal mode—the maximum GPU frequency supported in this mode is 800 MHz.
		0.9	1.0	1.05	V	Overdrive mode—the maximum GPU frequency supported in this mode is 1 GHz.
Power supply for VPU	VDD_VPU	0.81	0.9	1.05	V	Nominal mode—the maximum VPU frequency supported in this mode is 550/500/588 MHz.
		0.9	1.0	1.05	V	Overdrive mode—the maximum VPU G2/G1/AXI Bus frequency supported in this mode is 660/600/800 MHz.
Core voltage	VDD_DRAM	0.81	0.9	1.05	V	Nominal mode—the maximum DRAM working frequency supported in this mode is 933 MHz.
		0.99	1.0	1.05	V	Overdrive mode—the maximum DRAM working frequency supported in this mode is 1600 MHz
Power Supply Analog Domain	VDDA_1P8	1.62	1.8	1.98	V	Power for internal analog blocks—must match the range of voltages that the rechargeable backup battery supports.
PLL 1.8 V supply voltage	VDDA_DRAM	1.71	1.8	1.89	V	—

Table 7. Operating ranges (continued)

Parameter description	Symbol	Min	Typ	Max[1]	Unit	Comment
MIPI supply voltage	MIPI_VDDA	0.81	0.9/1.0	1.1	V	Analog core power supply
	MIPI_VDDHA	1.62	1.8	1.98	V	Analog IO power supply
	MIPI_VDD	0.81	0.9/1.0	1.1	V	Digital core power supply
	MIPI_VDDPLL	0.81	0.9/1.0	1.1	V	Analog supply for MIPI PLL
Voltage rails supplied from 1.8 V PHY	PCIE_VPH	1.674 3.069	1.8 3.3	1.98 3.63	V	Supplied from PMIC
	PCIE_VP, PCIE_VPTX	0.837	0.9	0.99	V	Supplied from PMIC
Temperature sensor accuracy	T_{delta}	—	±3	—	°C	Typical accuracy over the range –40°C to 125°C
Fuse power	EFUSE_VQPS	1.71	1.8	1.98	V	Power supply for internal use
Junction temperature, industrial	T_J	-40	—	+105	°C	See Table 2 for complete list of junction temperature capabilities.

1 Applying the maximum voltage results in maximum power consumption and heat generation. A voltage set point = (Vmin + the supply tolerance) is recommended. This result in an optimized power/speed ratio.

3.1.4 External clock sources

A 25 MHz oscillator is used as the primary clock source for the PLLs to generate the clock for CPU, BUS, and high-speed interfaces. For fractional PLLs, the 25 MHz clock from the oscillator can be directly used as the PLL reference clock.

A 27 MHz oscillator is used as the reference clock for HDMI PHY. Also it can be used as the alternative source for the fractional PLLs.

A 32 kHz clock input pin is used as the RTC clock source. It is expected to be supplied by an external 32.768 kHz oscillator. When an external RTC clock input is not present, the 32 kHz clock for internal logic is generated by the 25 MHz oscillator. The frequency of the internal 32 kHz clock will be 31.25 kHz.

Two pairs of differential clock inputs, named as CLK1P and CLK1N, can be used as the reference clock for the PLL. This is mainly used for a high-speed clock input during testing.

Four clock inputs to the CCM from normal GPIO pads via IOMUX can be used as the clock sources in the CCM.

Table 8 shows the interface frequency requirements.

Table 8. External input clock frequency

Parameter description	Symbol	Min	Typ	Max	Unit
RTC[1,2]	f_{ckil}	—	32.768[3]	—	kHz
XTALI_25M/XTALO_25M[2]	f_{xtal}	20	25	40	MHz
XTALI_27M/XTALO_27M[2]	f_{xtal}	20	27	40	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent.

3 Recommended nominal frequency 32.768 kHz.

The typical values shown in Table 8 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC operation, two clock sources are available.The decision of choosing a clock source should be made based on real-time clock use and precision timeout.

3.1.5 Maximum supply currents

Power consumption is highly dependent on the application. Estimating the maximum supply currents required for power supply design is difficult because the use cases that requires maximum supply current is not a realistic use cases.
To help illustrate the effect of the application on power consumption, data was collected while running industry standard benchmarks that are designed to be compute and graphic intensive. The results provided are intended to be used as guidelines for power supply design.

Devices used for the tests were from the high current end of the expected process variation.

Table 9. Maximum supply currents[1]

Power rail	Max current	Unit
VDD_ARM	384 to 3100[1]	mA
VDD_SOC	1400 to 2500[1]	mA
VDD_GPU	0 to 2040[1]	mA
VDD_VPU	0 to 610[1]	mA
VDD_DRAM	600 to 870[1]	mA
VDDA_0P9	50	mA
VDDA_1P8	20	mA
VDDA_DRAM	30	mA
VDD_SNVS	5	mA
NVCC_SNVS	5	mA
NVCC_<XXX>	I_{max} = N x C x V x (0.5 x F) Where: N—Number of IO pins supplied by the power line C—Equivalent external capacitive load V—IO voltage (0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F). In this equation, I_{max} is in Amps, C in Farads, V in Volts, and F in Hertz.	
NVCC_DRAM	375 to 750[1]	mA
DRAM_VFEF	10	mA
USB1_DVDD	9.2	mA
USB2_DVDD	9.2	mA

Table 15. PCIe recommended operating conditions (continued)

Parameter	Description	Min	Max	Unit
T_A	Commercial Temperature Range	0	70	°C
T_J	Simulation Junction Temperature Range	-40	125	°C

Note: V_{DD} should have no more than 40 mVpp AC power supply noise superimposed on the high power supply voltage for the PHY core (1.8 V nominal DC value). At the same time, VDD should have no more than 20 mVpp AC power supply noise superimposed on the low power supply voltage for the PHY core (1.0 V nominal value or 1.1 V overdrive DC value).
The power supply voltage variation for the PHY core should have less than ±5% including the board-level power supply variation and on-chip power supply variation due to the finite impedances in the package.

Table 16. PCIe DC electrical characteristics

Parameter	Description		Min	Typ	Max	Unit
PCIE1_VP, PCIE2_VP	Power Supply Voltage		0.9 - 7%	0.9	0.9 + 10%	V
PD	Power Consumption	Normal	—	40	—	mW
		Partial Mode	—	27	—	mW
		Slumber Mode	—	7	—	mW
		Full Powerdown	—	0.2	—	mW

Table 17. PCIe PHY high-speed characteristics

High Speed I/O Characteristics						
Description	**Symbol**	**Speed**	**Min.**	**Typ.**	**Max.**	**Unit**
Unit Interval	UI	2.5 Gbps	—	400	—	ps
		5.0 Gbps	—	200	—	
TX Serial output rise time (20% to 80%)	T_{TXRISE}	2.5 Gbps	100	—	—	ps
		5.0 Gbps	100	—	—	
TX Serial output fall time (80% to 20%)	T_{TXFALL}	2.5 Gbps	100	—	—	ps
		5.0 Gbps	100	—	—	
TX Serial data output voltage (Differential, pk–pk)	ΔV_{TX}	2.5 Gbps	800	—	1100	mVp–p
		5.0 Gbps	600	—	900	
PCIe Tx deterministic jitter < 1.5 MHz	TRJ	2.5 Gbps	3	—	—	ps, rms
		5.0 Gbps	3	—	—	
PCIe Tx deterministic jitter > 1.5 MHz	TDJ	2.5 Gbps	—	—	20	ps, pk–pk
		5.0 Gbps	—	—	10	

3.3 PLL electrical characteristics

Table 20. PLL electrical parameters

PLL type	Parameter	Value
AUDIO_PLL1	Clock output range	650 MHz ~ 1.3 GHz
	Reference clock	25 MHz
	Lock time	50 µs
	Jitter	±1% of output period, ≥ 50 ps
AUDIO_PLL2	Clock output range	650 MHz ~ 1.3 GHz
	Reference clock	25 MHz
	Lock time	50 µs
	Jitter	±1% of output period, ≥ 50 ps
VIDEO_PLL1	Clock output range	650 MHz ~ 1.3 GHz
	Reference clock	25 MHz
	Lock time	50 µs
VIDEO_PLL2	Clock output range	650 MHz ~ 1.3 GHz
	Reference clock	25 MHz
	Lock time	70 µs
SYS_PLL1	Clock output range	800 MHz
	Reference clock	25 MHz
	Lock time	70 µs
SYS_PLL2	Clock output range	1 GHz
	Reference clock	25 MHz
	Lock time	70 µs
SYS_PLL3	Clock output range	600 MHz ~ 1GHz
	Reference clock	25 MHz
	Lock time	70 µs
ARM_PLL	Clock output range	800 MHz ~1.6 GHz
	Reference clock	25 MHz
	Lock time	50 µs
DRAM_PLL	Clock output range	400 MHz–800 MHz
	Reference clock	25 MHz
	Lock time	70 µs

Table 41. eMMC4.4/4.41 interface timing specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD3	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.3	—	ns

3.9.2.3 HS400 DDR AC timing–eMMC5.0 only

Figure 13 depicts the timing of HS400 mode, and Table 42 lists the HS400 timing characteristics. Be aware that only data is sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for HS400 mode is the same as CMD input/output timing for SDR104 mode. Check SD5, SD6, and SD7 parameters in Table 44 SDR50/SDR104 Interface Timing Specification for CMD input/output timing for HS400 mode.

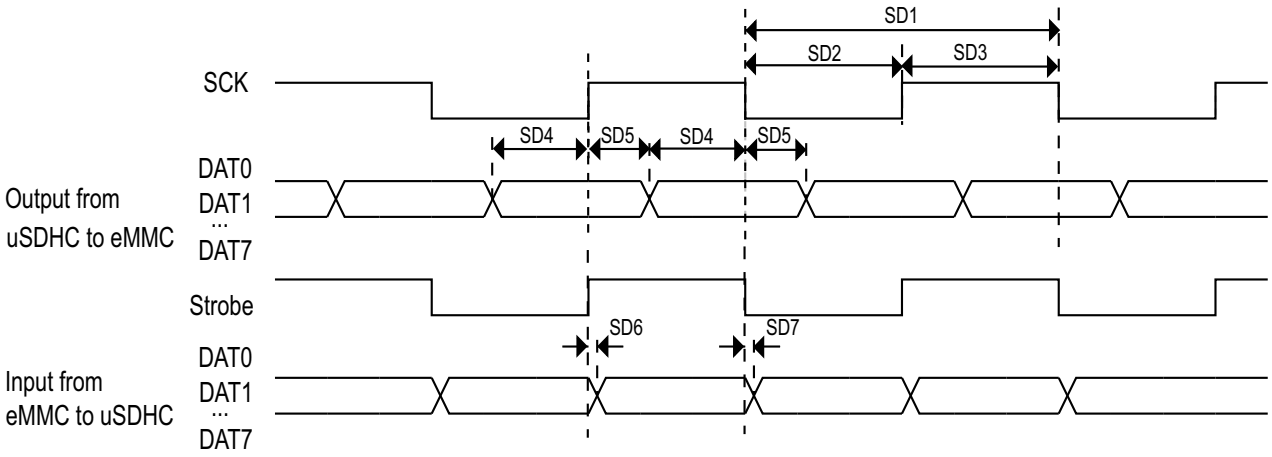

Figure 13. HS400 Mode timing

Table 42. HS400 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock frequency	f_{PP}	0	200	MHz
SD2	Clock low time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock high time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs DAT (Reference to SCK)					
SD4	Output skew from data of edge of SCK	t_{OSkew1}	0.45	—	ns
SD5	Output skew from edge of SCk to data	t_{OSkew2}	0.45	—	ns
uSDHC Input/Card Outputs DAT (Reference to Strobe)					

Table 42. HS400 interface timing specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD6	uSDHC input skew	t_{RQ}	—	0.45	ns
SD7	uSDHC hold skew	t_{RQH}	—	0.45	ns

3.9.2.4 HS200 Mode timing

Figure 14 depicts the timing of HS200 mode, and Table 43 lists the HS200 timing characteristics.

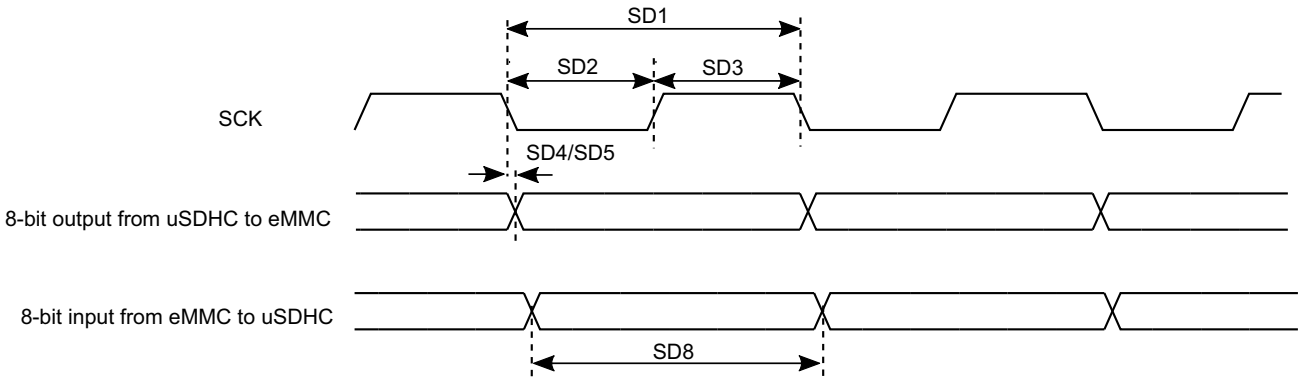

Figure 14. HS200 mode timing

Table 43. HS200 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5	—	ns
SD2	Clock Low Time	t_{CL}	0.3 x t_{CLK}	0.7 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.3 x t_{CLK}	0.7 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	-1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[1]					
SD8	uSDHC Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

1 HS200 is for 8 bits while SDR104 is for 4 bits.

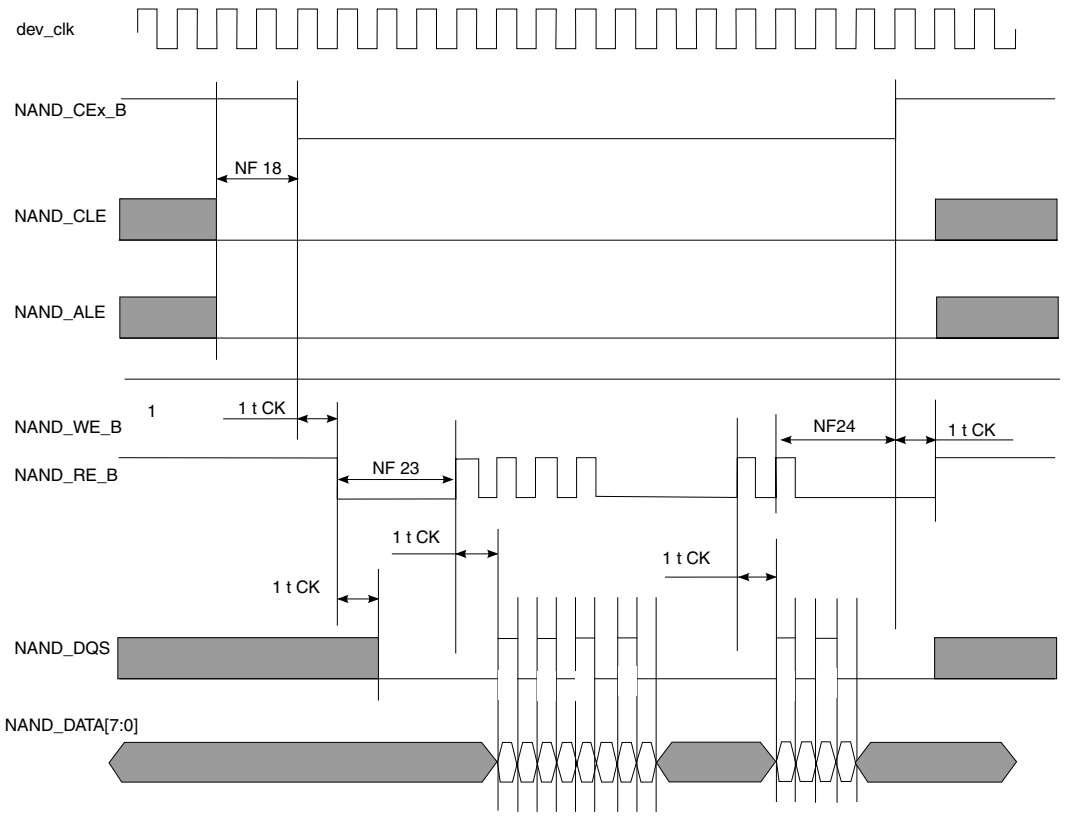

Figure 30. Toggle mode data read timing

Table 49. Toggle mode timing parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see note[2]s,[3]]		
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see note[2]]		
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see notes,[2]]		
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see note[2]]		
NF5	NAND_WE_B pulse width	tWP	DS × T [see note[2]]		
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see notes,[2]]		
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see note[2]]		
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see note[2]]		
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see note[2]]		
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see notes[4,2]]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see notes[5,2]]	—	ns

- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from DQS pad and used to sample input data.

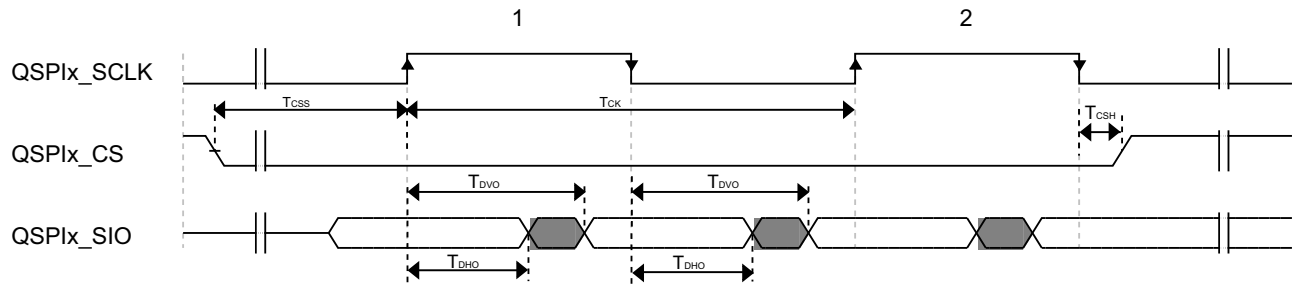

Figure 37. QuadSPI output/write timing (DDR mode)

Table 65. QuadSPI output/write timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output data valid time	—	(0.25 x T_{SCLK}) + 2	ns
T_{DHO}	Output data hold time	(0.25 x T_{SCLK}) - 0.5	—	ns
T_{CK}	SCK clock period	20	—	ns
T_{CSS}	Chip select output setup time	3	—	SCK cycle(s)
T_{CSH}	Chip select output hold time	3	—	ns

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register; the default value of 3 is shown on the timing. See the *i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processor Reference Manual* (IMX8MDQLQRM) for more details.

3.9.11 SAI/I2S switching specifications

This section provides the AC timings for the SAI in Master (clocks driven) and Slave (clocks input) modes. All timings are given for non inverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP] = 0) and non inverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

Table 66. Master mode SAI timing

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	20	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	40	—	ns

4 Boot mode configuration

This section provides information on Boot mode configuration pins allocation and boot devices interfaces allocation.

4.1 Boot mode configuration pins

Table 80 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed Boot mode options configured by the Boot mode pins, see the "System Boot, Fusemap, and eFuse" chapter in the *i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processor Reference Manual* (IMX8MDQLQRM).

Table 80. Fuses and associated pins used for boot

Pin	Direction at Reset	eFuse name	State during reset (POR_B asserted)	State after reset (POR_B deasserted)	Details
BOOT_MODE0	Input	N/A	Input with 95 K pull down	Input with 95 K pull down	Boot mode selection
BOOT_MODE1	Input	N/A	Input with 95 K pull down	Input with 95 K pull down	Boot mode selection
SAI1_RXD0	Input	BOOT_CFG[0]	Input with 95 K pull down	Input with 95 K pull down	Boot options pin value overrides fuse settings for BT_FUSE_SEL = "0". Signal configuration as fuse override input at power up. These are special I/O lines that control the boot configuration during product development. In production, the boot configuration can be controlled by fuses.
SAI1_RXD1	Input	BOOT_CFG[1]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_RXD2	Input	BOOT_CFG[2]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_RXD3	Input	BOOT_CFG[3]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_RXD4	Input	BOOT_CFG[4]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_RXD5	Input	BOOT_CFG[5]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_RXD6	Input	BOOT_CFG[6]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_RXD7	Input	BOOT_CFG[7]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_TXD0	Input	BOOT_CFG[8]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_TXD1	Input	BOOT_CFG[9]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_TXD2	Input	BOOT_CFG[10]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_TXD3	Input	BOOT_CFG[11]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_TXD4	Input	BOOT_CFG[12]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_TXD5	Input	BOOT_CFG[13]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_TXD6	Input	BOOT_CFG[14]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_TXD7	Input	BOOT_CFG[15]	Input with 95 K pull down	Input with 95 K pull down	

4.2 Boot device interface allocation

Table 81 lists the interfaces that can be used by the boot process in accordance with the specific Boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 81. Interface allocation during boot

Interface	IP Instance	Allocated Pads During Boot	Comment
NAND Flash	GPMI	NAND_ALE, NAND_CE0_B, NAND_CLE, NAND_DATA00, NAND_DATA01, NAND_DATA02, NAND_DATA03, NAND_DATA04, NAND_DATA05, NAND_DATA06, NAND_DATA07, NAND_DQS, NAND_RE_B, NAND_READY_B, NAND_WE_B, NAND_WP_B	8-bit, only CS0 is supported.
SD/MMC	USDHC-1	GPIO1_IO03, GPIO1_IO06, GPIO1_IO07, SD1_RESET_B, SD1_CLK, SD1_CMD, SD1_STROBE, SD1_DATA0, SD1_DATA1, SD1_DATA2, SD1_DATA3, SD1_DATA4, SD1_DATA5, SD1_DATA6, SD1_DATA7	1, 4, or 8-bit
SD/MMC	USDHC-2	GPIO1_IO04, GPIO1_IO08, GPIO1_IO07, SD2_RESET_B, SD2_CD_B, SD2_WP, SD2_CLK, SD2_CMD, SD2_DATA0, SD2_DATA1, SD2_DATA2, SD2_DATA3	1 or 4-bit
USB	USB_OTG PHY	—	—

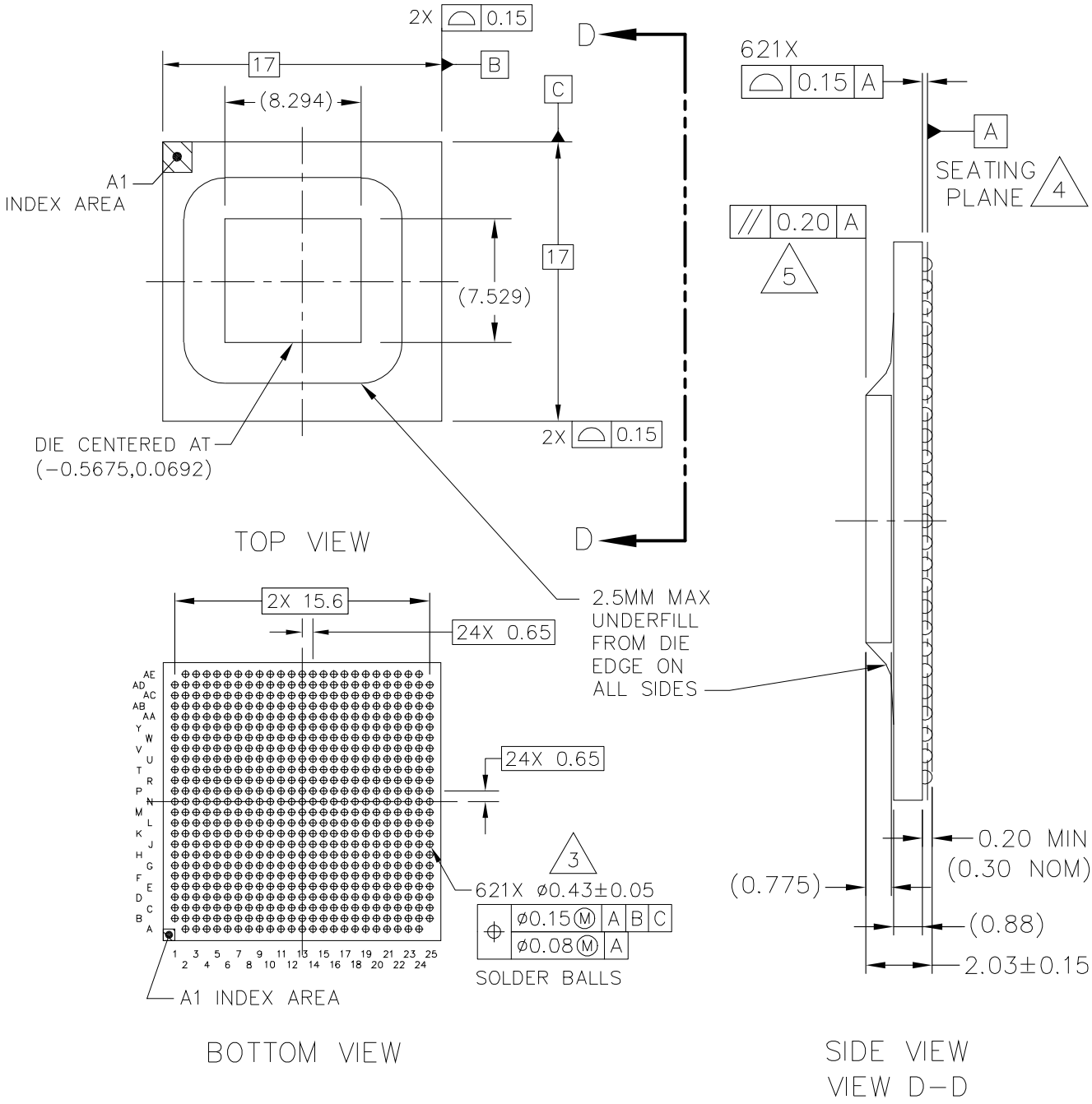

Figure 44. 17 x 17 mm BGA, package top, bottom, and side Views

Table 83. i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type[1]	Reset condition[2]			
				Default mode (Reset mode)	Default function (Signal name)	Input/ Output	Value
DRAM_DQ09	AA22	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ10	AA23	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ11	AA20	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ12	AA18	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ13	AB19	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ14	AA19	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ15	AA17	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ16	AE3	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ17	AD2	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ18	AE4	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ19	AD4	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ20	AA2	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ21	Y1	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ22	AA1	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ23	AB1	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ24	AB4	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ25	AA4	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ26	AA3	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ27	AA6	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ28	AA8	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ29	AB7	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ30	AA7	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ31	AA9	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQS0_N	AC25	NVCC_DRAM	DDRCLK	—	—	—	—
DRAM_DQS0_P	AC24	NVCC_DRAM	DDRCLK	—	—	—	—
DRAM_DQS1_N	AC21	NVCC_DRAM	DDRCLK	—	—	—	—
DRAM_DQS1_P	AB21	NVCC_DRAM	DDRCLK	—	—	—	—
DRAM_DQS2_N	AC1	NVCC_DRAM	DDRCLK	—	—	—	—
DRAM_DQS2_P	AC2	NVCC_DRAM	DDRCLK	—	—	—	—
DRAM_DQS3_N	AC5	NVCC_DRAM	DDRCLK	—	—	—	—

Table 83. i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type[1]	Reset condition[2]			
				Default mode (Reset mode)	Default function (Signal name)	Input/ Output	Value
GPIO1_IO04	P5	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[4]	Input	PD (90 K)
GPIO1_IO05[4]	P7	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[5]	Input	PU (27 K)
GPIO1_IO06	N5	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[6]	Input	PD (90 K)
GPIO1_IO07	N6	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[7]	Input	PD (90 K)
GPIO1_IO08	N7	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[8]	Input	PD (90 K)
GPIO1_IO09	M6	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[9]	Input	PD (90 K)
GPIO1_IO10	M7	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[10]	Input	PD (90 K)
GPIO1_IO11	L6	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[11]	Input	PD (90 K)
GPIO1_IO12	L7	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[12]	Input	PD (90 K)
GPIO1_IO13	K6	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[13]	Input	PD (90 K)
GPIO1_IO14	K7	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[14]	Input	PD (90 K)
GPIO1_IO15	J6	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[15]	Input	PD (90 K)
HDMI_AUX_N	V2	HDMI_AVDDIO	PHY	—	—	—	—
HDMI_AUX_P	V1	HDMI_AVDDIO	PHY	—	—	—	—
HDMI_CEC	W3	HDMI_AVDDIO	PHY	—	—	—	—
HDMI_DDC_SCL	R3	HDMI_AVDDIO	PHY	—	—	—	—
HDMI_DDC_SDA	P3	HDMI_AVDDIO	PHY	—	—	—	—
HDMI_HPD	W2	HDMI_AVDDIO	PHY	—	—	—	—
HDMI_REFCLK_N	R1	HDMI_AVDDIO	PHY	—	—	—	—
HDMI_REFCLK_P	R2	HDMI_AVDDIO	PHY	—	—	—	—
HDMI_REXT	P1	HDMI_AVDDIO	PHY	—	—	—	—
HDMI_TX_N_LN_0	T2	HDMI_AVDDIO	PHY	—	—	—	—
HDMI_TX_N_LN_1	U1	HDMI_AVDDIO	PHY	—	—	—	—
HDMI_TX_N_LN_2	N1	HDMI_AVDDIO	PHY	—	—	—	—
HDMI_TX_N_LN_3	M2	HDMI_AVDDIO	PHY	—	—	—	—
HDMI_TX_P_LN_0	T1	HDMI_AVDDIO	PHY	—	—	—	—
HDMI_TX_P_LN_1	U2	HDMI_AVDDIO	PHY	—	—	—	—
HDMI_TX_P_LN_2	N2	HDMI_AVDDIO	PHY	—	—	—	—
HDMI_TX_P_LN_3	M1	HDMI_AVDDIO	PHY	—	—	—	—
I2C1_SCL	E7	NVCC_I2C	GPIO	ALT5	GPIO5.IO[14]	Input	PD (90 K)

Table 83. i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type[1]	Reset condition[2]			
				Default mode (Reset mode)	Default function (Signal name)	Input/ Output	Value
NAND_READY_B	K20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[16]	Input	PD (90 K)
NAND_WE_B	K22	NVCC_NAND	GPIO	ALT5	GPIO3.IO[17]	Input	PD (90 K)
NAND_WP_B	K21	NVCC_NAND	GPIO	ALT5	GPIO3.IO[18]	Input	PD (90 K)
ONOFF	W21	NVCC_SNVS	GPIO	ALT0	snvsmix.ONOFF	Input	PU (27 K)
PCIE1_REF_PAD_CLK_N	K24	PCIE_VPH	PHY	—	—	—	—
PCIE1_REF_PAD_CLK_P	K25	PCIE_VPH	PHY	—	—	—	—
PCIE1_RESREF	G25	PCIE_VPH	PHY	—	—	—	—
PCIE1_RXN_N	H24	PCIE_VPH	PHY	—	—	—	—
PCIE1_RXN_P	H25	PCIE_VPH	PHY	—	—	—	—
PCIE1_TXN_N	J24	PCIE_VPH	PHY	—	—	—	—
PCIE1_TXN_P	J25	PCIE_VPH	PHY	—	—	—	—
PCIE2_REF_PAD_CLK_N	F24	PCIE_VPH	PHY	—	—	—	—
PCIE2_REF_PAD_CLK_P	F25	PCIE_VPH	PHY	—	—	—	—
PCIE2_RESREF	C25	PCIE_VPH	PHY	—	—	—	—
PCIE2_RXN_N	D24	PCIE_VPH	PHY	—	—	—	—
PCIE2_RXN_P	D25	PCIE_VPH	PHY	—	—	—	—
PCIE2_TXN_N	E24	PCIE_VPH	PHY	—	—	—	—
PCIE2_TXN_P	E25	PCIE_VPH	PHY	—	—	—	—
PMIC_ON_REQ	V20	NVCC_SNVS	GPIO	ALT0	snvsmix.PMIC_ON_REQ	Output	Open-Drain PU (27 K)
PMIC_STBY_REQ	V21	NVCC_SNVS	GPIO	ALT0	ccmsrcgpcmix.PMIC_STBY_REQ	Output	Low
POR_B	W20	NVCC_SNVS	GPIO	ALT0	snvsmix.POR_B	Input	PU (27 K)
RTC	V22	NVCC_SNVS	GPIO	ALT0	snvsmix.RTC	Input	PD (90 K)
RTC_RESET_B	W19	NVCC_SNVS	GPIO	ALT0	snvsmix.RTC_POR_B	Input	PU (27 K)
SAI1_MCLK	A3	NVCC_SAI1	GPIO	ALT5	GPIO4.IO[20]	Input	PD (90 K)
SAI1_RXC	K1	NVCC_SAI1	GPIO	ALT5	GPIO4.IO[1]	Input	PD (90 K)
SAI1_RXD0[5]	K2	NVCC_SAI1	GPIO	ALT5	GPIO4.IO[2]	Input	PD (90 K)

Table 84. 17 x 17 mm, 0.65 mm pitch ball map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
U	HDMI_TX_M_LN_1	HDMI_TX_P_LN_1	HDMI_AVDDCORE	HDMI_AVDDCORE	JTAG_TDO	JTAG_TRST_B	JTAG_MOD	VSS	VSS	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VSS	VSSA_FPLL	VDDA_1P8_FPLL	VSS	ENET_RD0	ENET_RD2	ENET_RD1	CLK2_N	VDDA_1P8_LVDS	XTALO_25M	XTALI_25M
V	HDMI_AUX_P	HDMI_AUX_N	HDMI_AVDDCLK	VSS	JTAG_TMS	BOOT_MODE1	TEST_MODE	VSS	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VSS	VSSA_SPLL	VDDA_0P9	ENET_RD3	PMIC_ON_REQ	PMIC_STBY_REQ	RTC	VSSA_XTAL_25M	XTALO_27M	XTALI_27M
W	VSS	HDMI_HPD	HDMI_CEC	NVCC_JTAG	JTAG_TDI	BOOT_MODE0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDA_1P8_SPLL	NVCC_SNVS	RTC_RESET_B	POR_B	ONOFF	VSSA_XTAL_27M	VDDA_1P8_XTAL_27M	VDDA_1P8_XTAL_25M	VSS
Y	DRAM_DQ21	VSS	VSS	VSS	VSS	VDD_DRAM	VSS	VDD_DRAM	VSS	VDD_DRAM	VSS	NVCC_DRAM	VSS	NVCC_DRAM	VSS	VDD_DRAM	VSS	VDD_DRAM	VSS	VDD_DRAM	VSS	VSS	VSS	VSS	DRAM_DQ05
AA	DRAM_DQ22	DRAM_DQ20	DRAM_DQ26	DRAM_DQ25	VSS	DRAM_DQ27	DRAM_DQ30	DRAM_DQ28	DRAM_DQ31	NVCC_DRAM	VDDA_DRAM	DRAM_AC27	DRAM_ZN	DRAM_VREF	NVCC_DRAM	VSS	DRAM_DQ15	DRAM_DQ12	DRAM_DQ14	DRAM_DQ11	VSS	DRAM_DQ09	DRAM_DQ10	DRAM_DQ04	DRAM_DQ06
AB	DRAM_DQ23	VSS	NVCC_DRAM	DRAM_DQ24	DRAM_DQS3_P	DRAM_DM3	DRAM_DQ29	NVCC_DRAM	VSS	DRAM_AC35	VSS	DRAM_AC26	DRAM_RESET_N	DRAM_AC19	DRAM_AC07	DRAM_AC14	NVCC_DRAM	VSS	DRAM_DQ13	DRAM_DM1	DRAM_DQS1_P	DRAM_DQ08	NVCC_DRAM	VSS	DRAM_DQ07
AC	DRAM_DQS2_N	DRAM_DQS2_P	NVCC_DRAM	VSS	DRAM_DQS3_N	NVCC_DRAM	DRAM_AC28	NVCC_DRAM	DRAM_AC23	DRAM_AC34	DRAM_AC38	DRAM_AC36	DRAM_ALERT_N	NVCC_DRAM	DRAM_AC15	DRAM_AC00	NVCC_DRAM	DRAM_AC03	VSS	NVCC_DRAM	DRAM_DQS1_N	VSS	NVCC_DRAM	DRAM_DQS0_P	DRAM_DQS0_N