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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	4 Core, 64-Bit
Speed	1.3GHz
Co-Processors/DSP	ARM® Cortex®-M4
RAM Controllers	DDR3L, DDR4, LPDDR4
Graphics Acceleration	Yes
Display & Interface Controllers	eDP, HDMI, MIPI-CSI, MIPI-DSI
Ethernet	GbE
SATA	-
USB	USB 3.0 (2)
Voltage - I/O	-
Operating Temperature	-40°C ~ 105°C (TJ)
Security Features	ARM TZ, CAAM, HAB, RDC, RTC, SJC, SNVS
Package / Case	621-FBGA, FCBGA
Supplier Device Package	621-FCPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mimx8mq5cvahzaa

Table 1. Features

Subsystem	Feature
Arm Cortex-A53 MPCore platform	Quad symmetric Cortex-A53 processors: • 32 KB L1 Instruction Cache • 32 KB L1 Data Cache • Support L1 cache RAMs protection with parity/ECC
	Support of 64-bit Armv8-A architecture: • 1 MB unified L2 cache • Support L2 cache RAMs protection with ECC • Frequency of 1.5 GHz
Arm Cortex-M4 core platform	16 KB L1 Instruction Cache
	16 KB L1 Data Cache
	256 KB tightly coupled memory (TCM)
Connectivity	Two PCI Express Gen2 interfaces
	Two USB 3.0/2.0 controllers with integrated PHY interfaces
	Two Ultra Secure Digital Host Controller (uSDHC) interfaces
	One Gigabit Ethernet controller with support for EEE, Ethernet AVB, and IEEE 1588
	Four Universal Asynchronous Receiver/Transmitter (UART) modules
	Four I^2C modules
	Three SPI modules
External memory interface	32/16-bit DRAM interface: LPDDR4-3200, DDR4-2400, DDR3L-1600
	8-bit NAND-Flash
	eMMC 5.0 Flash
	SPI NOR Flash
	QuadSPI Flash with support for XIP
GPIO and pin multiplexing	GPIO modules with interrupt capability
	Input/output multiplexing controller (IOMUXC) to provide centralized pad control
On-chip memory	Boot ROM (128 KB)
	On-chip RAM (128 KB + 32 KB)
Power management	Temperature sensor with programmable trip points
	Flexible power domain partitioning with internal power switches to support efficient power management

Table 1. Features (continued)

Subsystem	Feature
System debug	Arm CoreSight debug and trace architecture
	TPIU to support off-chip real-time trace
	ETF with 4 KB internal storage to provide trace buffering
	Unified trace capability for Quad Cortex-A53 and Cortex-M4 CPUs
	Cross Triggering Interface (CTI)
	Support for 5-pin (JTAG) debug interface

[1] Please contact the NXP sales and marketing team for order details on HDCP enable parts.

NOTE

The actual feature set depends on the part numbers as described in Table 2. Functions such as display and camera interfaces, and connectivity interfaces, may not be enabled for specific part numbers.

1.2 Ordering information

Table 2 shows examples of orderable sample part numbers covered by this data sheet. This table does not include all possible orderable part numbers. If your desired part number is not listed in the table, or you have questions about available parts, contact your NXP representative.

Table 2. Orderable part numbers

Part number[1]	Options	Cortex-A53 CPU speed grade	Qualification tier	Temperature T_j (°C)	Package
MIMX8MQ7CVAHZAA	8M Quad	1.3 GHz	Industrial	-40 to +105	17 x 17 mm, 0.65 mm pitch, FBGA
MIMX8MQ6CVAHZAA	8M Quad	1.3 GHz	Industrial	-40 to +105	17 x 17 mm, 0.65 mm pitch, FBGA
MIMX8MD7CVAHZAA	8M Dual	1.3 GHz	Industrial	-40 to +105	17 x 17 mm, 0.65 mm pitch, FBGA
MIMX8MD6CVAHZAA	8M Dual	1.3 GHz	Industrial	-40 to +105	17 x 17 mm, 0.65 mm pitch, FBGA
MIMX8MQ5CVAHZAA	8M Quad Lite	1.3 GHz	Industrial	-40 to +105	17 x 17 mm, 0.65 mm pitch, FBGA

1 Part number requires a Dolby Vision™ license from Dolby.

Figure 2 describes the part number nomenclature so that the users can identify the characteristics of the specific part number.

Contact an NXP representative for additional details.

remains powered. The M4 core can remain running. Compared with RUN mode, all the external power rails from the PMIC remain the same, and most of the modules still remain in their state.

- Deep Sleep Mode (DSM): The most efficient power saving mode where all the clocks are off and all the unnecessary power supplies are off.
- SNVS Mode: This mode is also called RTC mode. Only the power for the SNVS domain remains on to keep RTC and SNVS logic alive.
- OFF Mode: All power rails are off.

Table 10. Chip power in different LP mode

Mode	Supply	Max.[1]	Unit
SNVS	VDD_SNVS (1.0 V)	1.39	mA
	NVCC_SNVS (3.6 V)	4.25	
	Total[2]	17	mW
Deep Sleep Mode (DSM)	VDD_SOC (1.0 V)	148.50	mA
	VDDA_1P8 (2.0 V)	12.82	
	VDDA_0P9 (1.0 V)	0.30	
	VDDA_DRAM (1.8 V)	0.50	
	VDD_SNVS (1.0 V)	0.25	
	NVCC_SNVS (3.3 V)	4.80	
	NVCC_DRAM (1.17 V)	4.51	
	Total[2]	197	mW
IDLE	VDD_ARM (1.0 V)	152.10	mA
	VDD_SOC (1.0 V)	132.90	
	VDD_DRAM (1.0 V)	44.10	
	VDDA_1P8 (2.0 V)	13.53	
	VDDA_0P9 (1.0 V)	0.30	
	VDDA_DRAM (1.8 V)	1.32	
	VDD_SNVS (1.0 V)	0.25	
	NVCC_SNVS (3.3 V)	4.34	
	NVCC_DRAM (1.17 V)	13.12	
	Total[2]	389	mW
RUN	Total	1 to 4	mW

1 All the power numbers defined in the table are based on typical silicon at 25°C. Use case dependent

2 Sum of the listed supply rails.

Table 11 summarizes the external power supply states in all the power modes.

Table 11. The power supply states

Power rail	OFF	SNVS	SUSPEND	IDLE	RUN
VDD_ARM	OFF	OFF	OFF	ON	ON
VDD_SOC	OFF	OFF	ON	ON	ON
VDD_GPU	OFF	OFF	OFF	OFF	ON/OFF
VDD_VPU	OFF	OFF	OFF	OFF	ON/OFF
VDD_DRAM	OFF	OFF	OFF	ON	ON
VDDA_0P9	OFF	OFF	ON	ON	ON
VDDA_1P8	OFF	OFF	ON	ON	ON
VDDA_DRAM	OFF	OFF	ON	ON	ON
VDD_SNVS	OFF	ON	ON	ON	ON
NVCC_SNVS	OFF	ON	ON	ON	ON
NVCC_<XXX>	OFF	OFF	ON	ON	ON
NVCC_DRAM	OFF	OFF	ON	ON	ON
DRAM_VREF	OFF	OFF	OFF	ON	ON

- Turn on VDD_ARM, VDD_GPU, VDD_VPU, and VDD_DRAM (no sequence between these four rails)
- Turn on VDDA_1P8_XXX, VDDA_DRAM (no sequence between these rails)
- Turn on NVCC_XXX and NVCC_DRAM (no sequence between these rails)
- POR_B release (it should be asserted during the entire power up sequence)

If the GPU/VPU is not used during the ROM boot sequence, VDD_GPU/VDD_VPU can stay off to reduce the power during boot, and then turned on by software afterwards.

During the chip power up, the power of the PCIe PHY, USB PHY, HDMI PHY, and MIPI PHY could stay off. After chip power up, the power of these PHys should be turned on. If any of the PHY power are turned on during the power up sequence, the POR_B can be released after the PHY power is stable.

3.2.2 Power-down sequence

The i.MX 8M Dual / 8M QuadLite / 8M Quad processors have the following power-down sequence requirements:

- Turn off NVCC_SNVS and VDD_SNVS last
- Turn off VDD_SOC after the other power rails or at the same time as other rails
- No sequence for other power rails during power down

3.2.3 Power supplies usage

I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about the I/O power supply of each pin, see “Power Rail” columns in the pin list tables of Section 5, “Package information and contact assignments.”

Table 19 lists the modules in each power domain.

Table 19. The modules in the power domains

Power Domain	Modules in the domain
VDD_ARM	Arm A53
VDD_GPU	GC7000L GPU
VDD_VPU	G1 and G2 VPU
VDD_DRAM	DRAM controller and PHY
VDD_SNVS	SNVS_LP
VDD_SOC	All the other modules

Table 23 shows the input clock specifications.

Table 23. Input clock specification

Parameter	Min	Typ	Max	Unit
Clock Frequency in OSC mode	20	—	40	MHz
Input Clock Frequency in Bypass mode	—	—	50	MHz
Input Clock Rise/Fall Time in Bypass mode	—	—	1	ns
Input Clock Duty Cycle in Bypass mode	47.50	50	52.50	%

Table 24 shows core output clock specification.

Table 24. Core output clock specification

Parameter	Min	Typ	Max	Unit
Output Clock Frequency in OSC mode	20	—	40	MHz
Output Clock Duty Cycle in OSC mode	45	50	55	%
Output Clock Frequency in Bypass mode	—	—	50	MHz
Capacitive Loading on Outputs Clock	—	150	500	fF
Output Clock Rise/Fall Time in Bypass mode	—	0.1	0.5	ns
Output Clock Duty Cycle in Bypass mode	40	50	60	%

Table 25 shows VIL/VIH specification at EXTAL.

Table 25. Transconductance specification of oscillator

Parameter	Condition	Min	Max	Unit
$V_{ILEXTAL}$	V_{REF} = 0.5 x avdd (xosc HV supply)	0	V_{REF} - 0.5	V
$V_{IHEXTAL}$		V_{REF} + 0.5	avdd	

3.5 I/O DC parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR4, DDR4, and DDR3L modes
- Differential I/O (CLKx)

3.5.2.1 LPDDR4 mode I/O DC parameters

Table 30. LPDDR4 I/O DC electrical parameters

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1 mA	0.9 x OVDD	—	V
Low-level output voltage	VOL	Iol= 0.1 mA	—	0.1 x OVDD	V
Input Reference Voltage	Vref	—	0.49 x OVDD	0.51 x OVDD	V
DC High-Level input voltage	Vih_DC	—	VRef + 0.100	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	VRef – 0.100	V
Differential Input Logic High	Vih_diff	—	0.26	See note[1]	—
Differential Input Logic Low	Vil_diff	—	See note	-0.26	—
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	–15	15	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	110	175	KΩ
Input current (no pull-up/down)	Iin	VI = 0, VI = OVDD	-2.5	2.5	µA

[1] The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

3.5.3 Differential I/O port (CLKx_P/N)

The clock I/O interface is designed to be compatible with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits* (2001), for details.

The CLK1_P/CLK1_N is input only, while CLK2_P/CLK2_N is output only.

3.6 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for DDR3L/DDR4/LPDDR4 modes
- Differential I/O (CLKx)

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 3 and Figure 4.

Table 34 shows the AC parameters for clock I/O.

Table 34. I/O AC parameters of LVDS pad

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Notes
Tphld	Output Differential propagation delay high to low	Rload = 100 Ω between padp and padn, Cload = 2pF, at 125 °C, TYP, 1.62 V OVDD, and 0.9 V VDDI	—	—	0.92	ns	1
Tplhd	Output Differential propagation delay low to high		—	—	0.92		
Ttlh	Output Transition time low to high		—	—	0.58		2
Tthl	Output Transition time high to low		—	—	0.73		
Tphlr	Input Differential propagation delay high to low	Rload = 100 Ω between padp and padn, at 125 °C, TYP, 1.62 V OVDD, and 0.9 V VDDI	—	—	0.83	ns	3
Tplhr	Input Differential propagation delay low to high		—	—	0.83		
Ttx	Transmitter startup time (ipp-obe low to high)	—	—	—	40	ns	4
F	Operating frequency	—	—	600	1000	MHz	—

1 At TYP, 125 °C, 1.62 V OVDD, and 0.9 V VDDI. Measurement levels are 50 - 50%. Output differential signal measured.

2 At TYP, 125 °C, 1.62 V OVDD, and 0.9 V VDDI. Measurement levels are 20 - 80%. Output differential signal measured.

3 At TYP, 125 °C, 1.62 V OVDD, and 0.9 V VDDI. Measurement levels are 50 - 50%.

4 TX startup time is defined as the time taken by transmitter for settling after its ipp_obe has been asserted. It is to stabilize the current reference. Functionality is guaranteed only after the startup time.

3.7 Output buffer impedance parameters

This section defines the I/O impedance parameters of the i.MX 8M Dual / 8M QuadLite / 8M Quad processors for the following I/O types:

- Double Data Rate I/O (DDR) for LPDDR4, DDR4, and DDR3L modes
- Differential I/O (CLKx)
- USB battery charger detection open-drain output (USB_OTG1_CHD_B)

NOTE

DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 6).

3.9.3.2 RGMII signal switching specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 46. RGMII signal switching specifications[1]

Symbol	Description	Min.	Max.	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-500	500	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	85	%
Duty_T[4]	Duty cycle for 10/100T	40	90	%
Tr/Tf	Rise/fall time (20–80%)	—	0.98	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; this implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

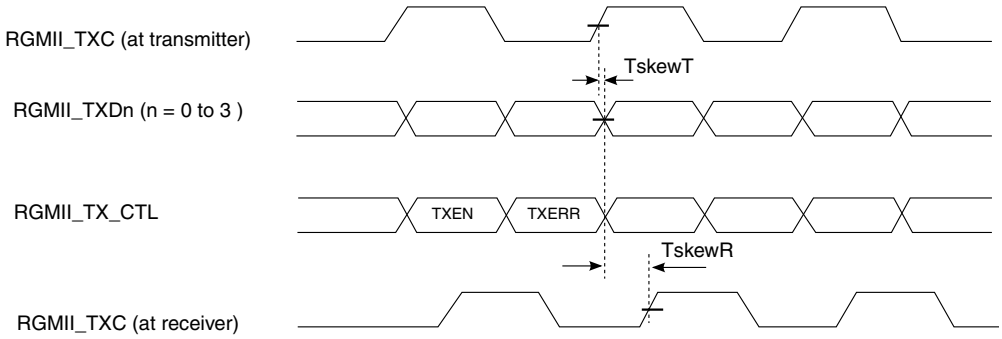

Figure 17. RGMII transmit signal timing diagram original

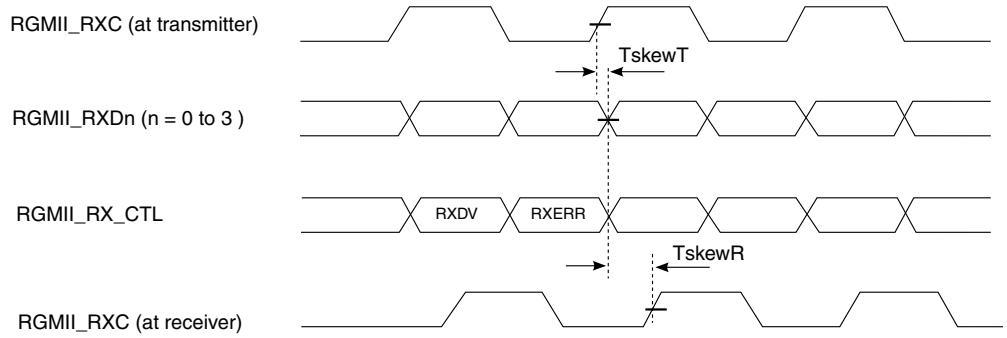

Figure 18. RGMII receive signal timing diagram original

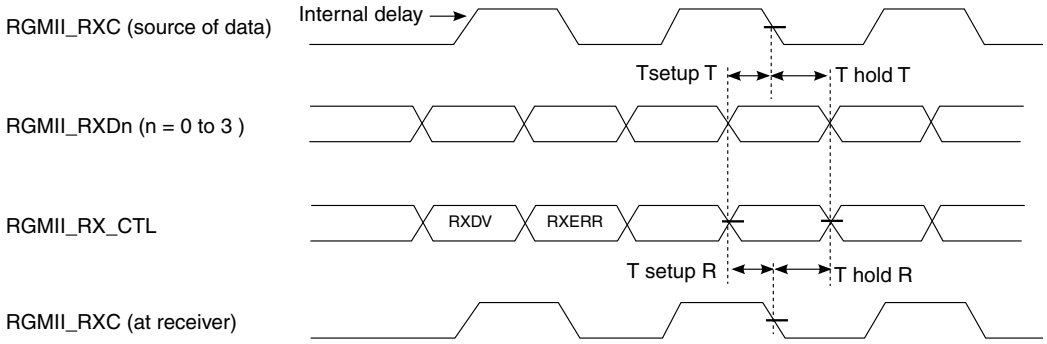

Figure 19. RGMII receive signal timing diagram with internal delay

3.9.4 General-purpose media interface (GPMI) timing

The GPMI controller of the i.MX 8M Dual / 8M QuadLite / 8M Quad is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous Timing mode, Source Synchronous Timing mode and Toggle Timing mode separately, as described in the following subsections.

3.9.4.1 Asynchronous mode AC timing (ONFI 1.0 compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 20 through Figure 23 depicts the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 47 describes the timing parameters (NF1–NF17) that are shown in the figures.

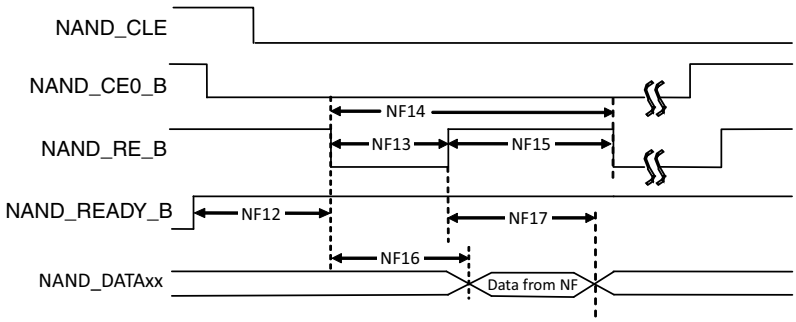

Figure 24. Read Data Latch cycle timing diagram (EDO mode)

Table 47. Asynchronous mode timing parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see notes[2,3]]		ns
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see note[2]]		ns
NF3	NAND_CE0_B setup time	tCS	(AS + DS + 1) × T [see notes[3,2]]		ns
NF4	NAND_CE0_B hold time	tCH	(DH+1) × T - 1 [see note[2]]		ns
NF5	NAND_WE_B pulse width	tWP	DS × T [see note[2]]		ns
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see notes[3,2]]		ns
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see note[2]]		ns
NF8	Data setup time	tDS	DS × T - 0.26 [see note[2]]		ns
NF9	Data hold time	tDH	DH × T - 1.37 [see note[2]]		ns
NF10	Write cycle time	tWC	(DS + DH) × T [see note[2]]		ns
NF11	NAND_WE_B hold time	tWH	DH × T [see note[2]]		ns
NF12	Ready to NAND_RE_B low	tRR[4]	(AS + 2) × T [see [3,2]]	—	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see note[2]]		ns
NF14	READ cycle time	tRC	(DS + DH) × T [see note[2]]		ns
NF15	NAND_RE_B high hold time	tREH	DH × T [see note[2]]		ns
NF16	Data setup on read	tDSR	—	(DS × T -0.67)/18.38 [see notes[5,6]]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see notes[5,6]]	—	ns

1 GPMI's Asynchronous mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = GPMI clock period -0.075 ns (half of maximum p-p jitter).

4 NF12 is guaranteed by the design.

5 Non-EDO mode.

6 EDO mode, GPMI clock ≈ 100 MHz (AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 23), NF16/NF17 are different from the definition in non-EDO mode (Figure 22). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical values for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI samples NAND_DATAxx at the rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the *i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processor Reference Manual* [IMX8MDQLQRM]). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

3.9.4.2 Source synchronous mode AC timing (ONFI 2.x compatible)

Figure 25 to Figure 27 show the write and read timing of Source Synchronous mode.

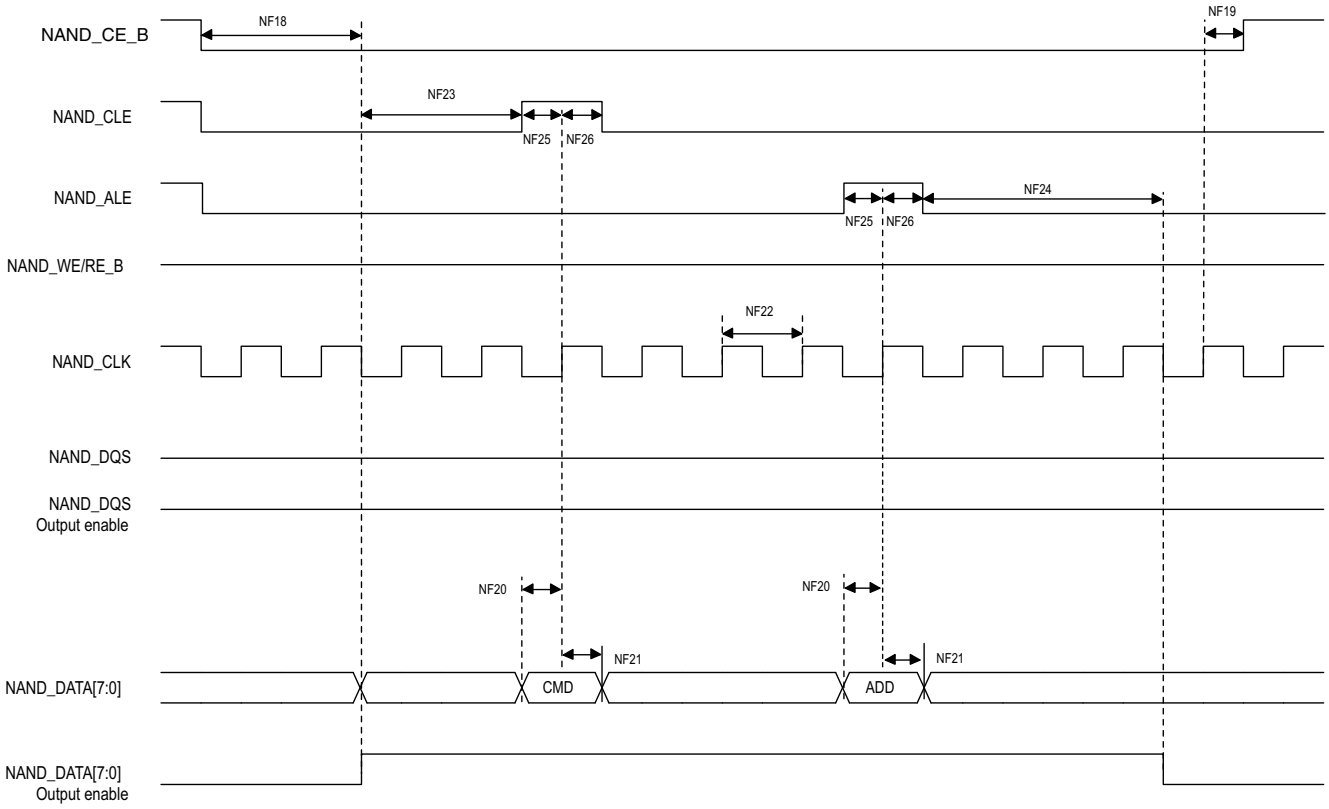

Figure 25. Source Synchronous mode command and address timing diagram

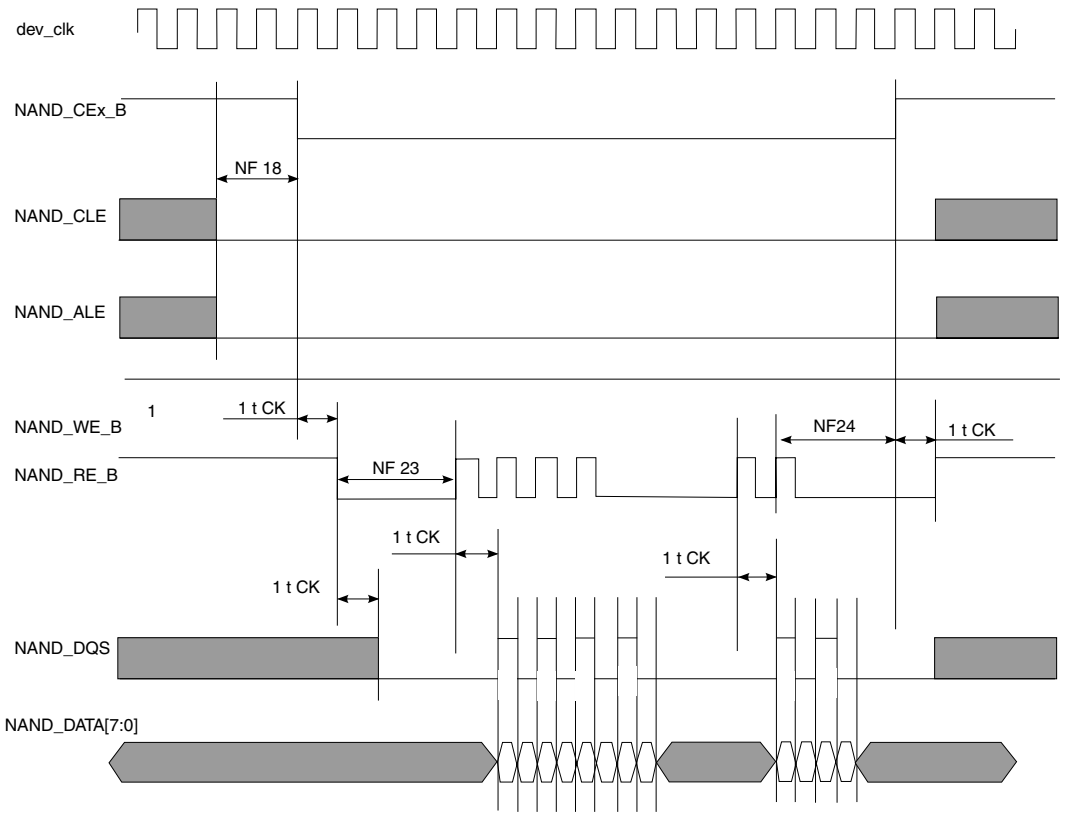

Figure 30. Toggle mode data read timing

Table 49. Toggle mode timing parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see note[2]s,[3]]		
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see note[2]]		
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see notes,[2]]		
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see note[2]]		
NF5	NAND_WE_B pulse width	tWP	DS × T [see note[2]]		
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see notes,[2]]		
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see note[2]]		
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see note[2]]		
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see note[2]]		
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see notes[4,2]]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see notes[5,2]]	—	ns

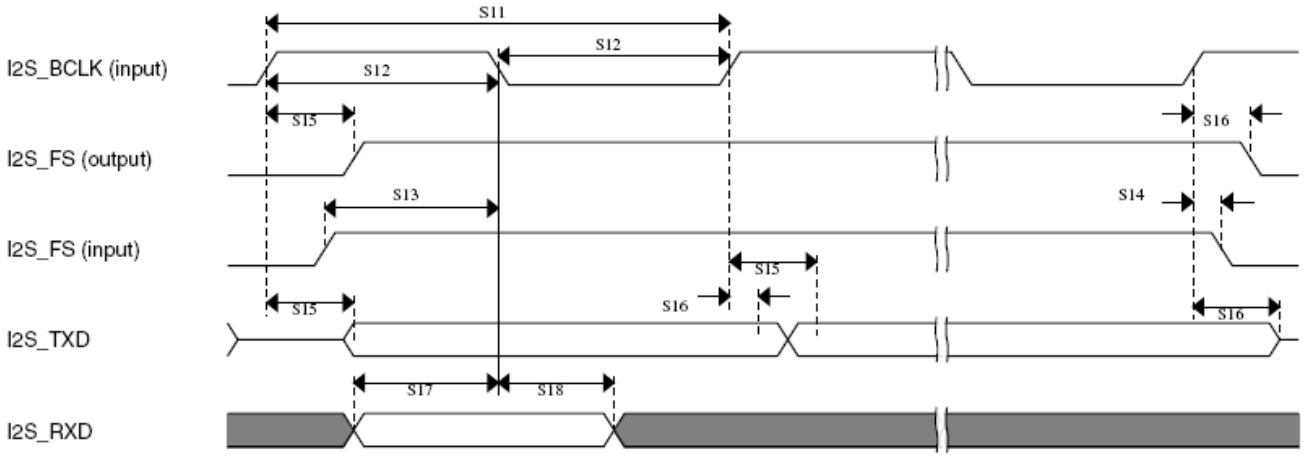

Figure 39. SAI Timing — Slave Modes

3.9.12 SPDIF timing parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 68 and Figure 40 and Figure 41 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 68. SPDIF timing parameters

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50 pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT output (Load = 30 pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

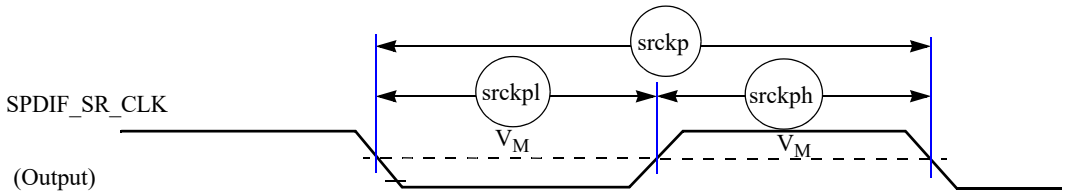

Figure 40. SPDIF_SR_CLK timing diagram

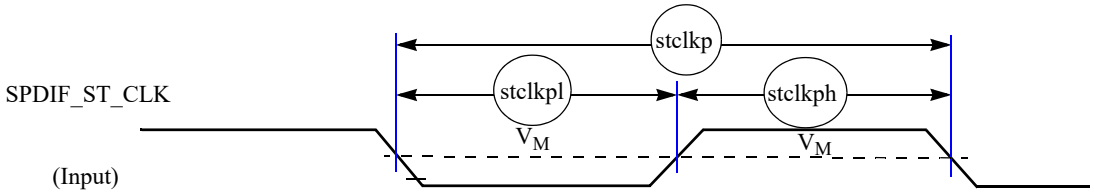

Figure 41. SPDIF_ST_CLK timing diagram

3.9.13 UART I/O configuration and timing parameters

3.9.13.1 UART RS-232 I/O configuration in different modes

The UART interfaces of the i.MX 8M Dual / 8M QuadLite / 8M Quad can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0—DCE mode). Table 69 shows the UART I/O configuration based on the enabled mode.

Table 69. UART I/O configuration vs. mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	UARTx_RTS_B from DTE to DCE	Input	UARTx_RTS_B from DTE to DCE
UARTx_CTS_B	Input	UARTx_CTS_B from DCE to DTE	Output	UARTx_CTS_B from DCE to DTE
UARTx_TX_ DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX _DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

3.9.13.2 UART RS-232 Serial mode timing

This section describes the electrical information of the UART module in the RS-232 mode.

4 Boot mode configuration

This section provides information on Boot mode configuration pins allocation and boot devices interfaces allocation.

4.1 Boot mode configuration pins

Table 80 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed Boot mode options configured by the Boot mode pins, see the "System Boot, Fusemap, and eFuse" chapter in the *i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processor Reference Manual* (IMX8MDQLQRM).

Table 80. Fuses and associated pins used for boot

Pin	Direction at Reset	eFuse name	State during reset (POR_B asserted)	State after reset (POR_B deasserted)	Details
BOOT_MODE0	Input	N/A	Input with 95 K pull down	Input with 95 K pull down	Boot mode selection
BOOT_MODE1	Input	N/A	Input with 95 K pull down	Input with 95 K pull down	Boot mode selection
SAI1_RXD0	Input	BOOT_CFG[0]	Input with 95 K pull down	Input with 95 K pull down	Boot options pin value overrides fuse settings for BT_FUSE_SEL = "0". Signal configuration as fuse override input at power up. These are special I/O lines that control the boot configuration during product development. In production, the boot configuration can be controlled by fuses.
SAI1_RXD1	Input	BOOT_CFG[1]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_RXD2	Input	BOOT_CFG[2]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_RXD3	Input	BOOT_CFG[3]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_RXD4	Input	BOOT_CFG[4]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_RXD5	Input	BOOT_CFG[5]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_RXD6	Input	BOOT_CFG[6]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_RXD7	Input	BOOT_CFG[7]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_TXD0	Input	BOOT_CFG[8]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_TXD1	Input	BOOT_CFG[9]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_TXD2	Input	BOOT_CFG[10]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_TXD3	Input	BOOT_CFG[11]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_TXD4	Input	BOOT_CFG[12]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_TXD5	Input	BOOT_CFG[13]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_TXD6	Input	BOOT_CFG[14]	Input with 95 K pull down	Input with 95 K pull down	
SAI1_TXD7	Input	BOOT_CFG[15]	Input with 95 K pull down	Input with 95 K pull down	

5.1.2 17 x 17 mm supplies contact assignments and functional contact assignments

Table 82 shows supplies contact assignments for the 17 x 17 mm package.

Table 82. i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm supplies contact assignments

Supply Rail Name	Ball(s) Postion(s)	Remark
EFUSE_VQPS	R17	Supply for eFuse Programming
HDMI_AVDDCLK	V3	Supply for HDMI PHY
HDMI_AVDDCORE	U3, U4	Supply for HDMI PHY
HDMI_AVDDIO	P2	Supply for HDMI PHY
MIPI_VDD	E15, F15	Supply for MIPI PHY
MIPI_VDDA	E17, E18, F17, F18	Supply for MIPI PHY
MIPI_VDDHA	C18, D17, D18	Supply for MIPI PHY
MIPI_VDDPLL	F19	Supply for MIPI PHY
NVCC_DARAM	Y12, Y14, AA10, AA15, AB3, AB8, AB17, AB23, AC3, AC6, AC8, AC14, AC17, AC20, AC23, AD5, AD18, AD21	Supply for DRAM Interface
NVCC_ECSPI	F5	Supply for ESCPI Interface
NVCC_ENET	T18	Supply for ENET Interface
NVCC_GPIO1	R5, R6	Supply for GPIO1 Interface
NVCC_I2C	H7	Supply for I2C Interface
NVCC_JTAG	W4	Supply for JTAG Interface
NVCC_NAND	L18, M18	Supply for NAND Interface
NVCC_SAI1	K3, L3	Supply for SAI Interface
NVCC_SAI2	J7	Supply for SAI Interface
NVCC_SAI3	E3	Supply for SAI Interface
NVCC_SAI5	M3	Supply for SAI Interface
NVCC_SD1	L23, M23	Supply for SD Interface
NVCC_SD2	N23	Supply for SD Interface
NVCC_SNVS	W18	Supply for SNVS Interface
NVCC_UART	D8	Supply for UART Interface
PCIE_VP	F22, G22	Supply for PCIe PHY
PCIE_VPH	H23, J23	Supply for PCIe PHY
PCIE_VPTX	F23, G23	Supply for PCIe PHY
USB1_DVDD	E12	Supply for USB PHY
USB1_VDD33	G12	Supply for USB PHY
USB1_VP	D12	Supply for USB PHY

Table 82. i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm supplies contact assignments (continued)

VSS	A2, A24, B1, B25, C8, C10, C13, C15, C24, D10, D13, D15, D23, E4, E10, E13, E14, E16, E19, E20, E21, E22, E23, F10, F13, F14, F16, F20, G9, G10, G13, G17, G18, G24, H8, H9, H10, H11, H12, H13, H17, H18, J3, J8, J11, J12, J13, J14, J17, J18, J19, K8, K11, K17, K18, K23, L8, L11, L14, L17, M8, M11, M14, M17, N3, N14, N15, N16, N17, N18, P6, P8, P11, P14, P17, P18, P23, R7, T3, T4, T9, T10, T11, T12, T13, U8, U9, U15, U18, V4, V8, V16, W1, W7, W8, W9, W10, W11, W12, W13, W14, W15, W16, W25, Y2, Y3, Y4, Y5, Y7, Y9, Y11, Y13, Y15, Y17, Y19, Y21, Y22, Y23, Y24, AA5, AA16, AA21, AB2, AB9, AB11, AB18, AB24, AC4, AC19, AC22, AD1, AD7, AD9, AD11, AD13, AD16, AD25, AE2, AE5, AE21, AE24	—
VSSA_FPLL	U16	Return path of VDDA_1P8_FPLL
VSSA_FPLL_ARM	K13	Return path of VDDA_1P8_FPLL_ARM
VSSA_SPLL	V17	Return path of VDDA_1P8_SPLL
VSSA_SPLL_DRAM	T14	Return path of VDDA_1P8_SPLL_DRAM
VSSA_SPLL_VIDEO2	N12	Return path of VDDA_1P8_SPLL_VIDEO2
VSSA_XTAL_25M	V23	Return path of VDDA_1P8_XTAL_25M
VSSA_XTAL_27M	W22	Return path of VDDA_1P8_XTAL_27M

Table 85. DDR pin function list for 17 x 17 mm package (continued)

DRAM_AC08	CA0_A	A12	A12 / BC#	AD17
DRAM_AC09	CA1_A	A11	A11	AE16
DRAM_AC10	CA2_A	A7	A7	AD20
DRAM_AC11	CA3_A	A8	A8	AE20
DRAM_AC12	CA4_A	A6	A6	AD19
DRAM_AC13	CA5_A	A5	A5	AE19
DRAM_AC14	—	A4	A4	AB16
DRAM_AC15	—	A3	A3	AC15
DRAM_AC16	—	CK_t_A	CK_A	AE15
DRAM_AC17	—	CK_c_A	CK#_A	AD15
DRAM_AC19	MTEST	MTEST	MTEST	AB14
DRAM_AC20	CKE0_B	CK_t_B	CK_B	AD10
DRAM_AC21	CKE1_B	CK_c_B	CK#_B	AE10
DRAM_AC22	CS1_B	—	—	AD8
DRAM_AC23	CS0_B	—	—	AC9
DRAM_AC24	CK_t_B	A2	A2	AD12
DRAM_AC25	CK_c_B	A1	A1	AE12
DRAM_AC26	—	BA1	BA1	AB12
DRAM_AC27	—	PARITY	—	AA12
DRAM_AC28	CA2_B	A13	A13	AC7
DRAM_AC29	CA3_B	BA0	BA0	AE7
DRAM_AC30	CA4_B	A10 / AP	A10 / AP	AE6
DRAM_AC31	CA5_B	A0	A0	AD6
DRAM_AC32	CA0_B	C2	—	AE8
DRAM_AC33	CA1_B	CAS_n / A15	CAS#	AE9
DRAM_AC34	—	WE_n / A14	WE#	AC10
DRAM_AC35	—	RAS_n / A16	RAS#	AB10
DRAM_AC36	—	ODT0	ODT0	AC12
DRAM_AC37	—	ODT1	ODT1	AE11
DRAM_AC38	—	CS1_n	CS1#	AC11
DRAM_ZN	ZQ	ZQ	ZQ	AA13
DRAM_VREF	VREF	VREF	VREF	AA14