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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	4 Core, 64-Bit
Speed	1.3GHz
Co-Processors/DSP	ARM® Cortex®-M4
RAM Controllers	DDR3L, DDR4, LPDDR4
Graphics Acceleration	Yes
Display & Interface Controllers	eDP, HDMI, MIPI-CSI, MIPI-DSI
Ethernet	GbE
SATA	-
USB	USB 3.0 (2)
Voltage - I/O	-
Operating Temperature	-40°C ~ 105°C (TJ)
Security Features	ARM TZ, CAAM, HAB, RDC, RTC, SJC, SNVS
Package / Case	621-FBGA, FCBGA
Supplier Device Package	621-FCPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mimx8mq6cvahzaa

1.1 Block diagram

Figure 1 shows the functional modules in the i.MX 8M Dual / 8M QuadLite / 8M Quad processor system.

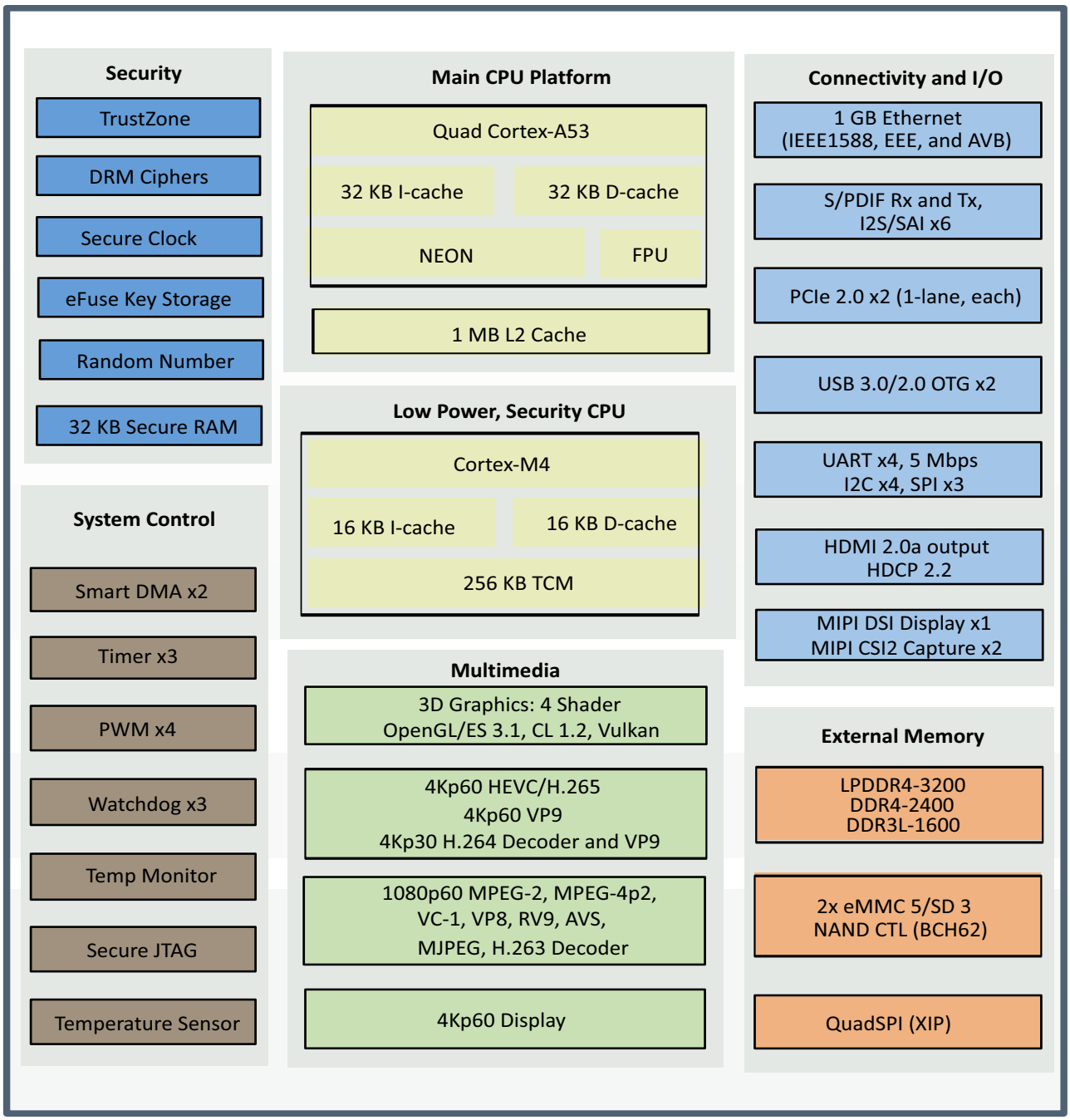

Figure 1. i.MX 8M Dual / 8M QuadLite / 8M Quad system block diagram

2 Modules list

The i.MX 8M Dual / 8M QuadLite / 8M Quad processors contain a variety of digital and analog modules. Table 3 describes these modules in alphabetical order.

Table 3. i.MX 8M Dual / 8M QuadLite / 8M Quad modules list

Block mnemonic	Block name	Brief description
APBH-DMA	NAND Flash and BCH ECC DMA Controller	DMA controller used for GPMI2 operation.
Arm	Arm Platform	The Arm Core Platform includes a quad Cortex-A53 core and a Cortex-M4 core. The Cortex-A53 core includes associated sub-blocks, such as the Level 2 Cache Controller, Snoop Control Unit (SCU), General Interrupt Controller (GIC), private timers, watchdog, and CoreSight debug modules. The Cortex-M4 core is used as a customer microcontroller.
BCH	Binary-BCH ECC Processor	The BCH module provides up to 62-bit ECC encryption/decryption for NAND Flash controller (GPMI)
CAAM	Cryptographic accelerator and assurance module	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, entropy source generator, and a Pseudo Random Number Generator (PRNG). The PRNG is certifiable by the Cryptographic Algorithm Validation Program (CAVP) of the National Institute of Standards and Technology (NIST). CAAM also implements a Secure Memory mechanism. In i.MX 8M Dual / 8M QuadLite / 8M Quad processors, the secure memory provided is 32 KB.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSU	Central Security Unit	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 8M Dual / 8M QuadLite / 8M Quad platform.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interface	Cross Trigger Interface (CTI) allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A53 core platform.
DAP	Debug Access Port	The DAP provides real-time access for the debugger without halting the core to access: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains.
DC	Display Controller	Dual display controller
DDRC	Double Data Rate Controller	The DDR Controller has the following features: • Supports 32/16-bit LPDDR4-3200, DDR4-2400, and DDR3L-1600 • Supports up to 8 Gbyte DDR memory space
eCSPI1 eCSPI2 eCSPI3	Configurable SPI	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. Configurable to support Master/Slave modes, four chip selects to support multiple peripherals.

Table 3. i.MX 8M Dual / 8M QuadLite / 8M Quad modules list (continued)

Block mnemonic	Block name	Brief description
EIM	NOR-Flash / PSRAM interface	The EIM NOR-FLASH / PSRAM provides: • Support for 16-bit (in Muxed I/O mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support for 16-bit (in muxed and non muxed I/O modes) NOR-Flash memories, at slow frequency • Multiple chip selects
ENET1	Ethernet Controller	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the *i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processor Reference Manual* (IMX8MDQLQRM) for details.
GIC	Generic Interrupt Controller	The GIC handles all interrupts from the various subsystems and is ready for virtualization.
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5	General Purpose I/O Modules	Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPMI	General Purpose Memory Interface	The GPMI module supports up to 8x NAND devices and 62-bit ECC encryption/decryption for NAND Flash Controller (GPMI2). GPMI supports separate DMA channels for each NAND device.
GPT1 GPT2 GPT3 GPT4 GPT5 GPT6	General Purpose Timer	Each GPT is a 32-bit “free-running” or “set-and-forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set-and-forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU3D	Graphics Processing Unit-3D	The GPU3D provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays.
HDMI Tx	HDMI Tx interface	The HDMI module provides an HDMI standard interface port to an HDMI 2.0a-compliant display.
I2C1 I2C2 I2C3 I2C4	I^2C Interface	I^2C provides serial interface for external devices.
IOMUXC	IOMUX Control	This module enables flexible I/O multiplexing. Each IO pad has a default as well as several alternate functions. The alternate functions are software configurable.
LCDIF	LCD interface	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability.

Table 9. Maximum supply currents[1] (continued)

Power rail	Max current	Unit
USB1_VP	35.7	mA
USB2_VP	35.7	mA
USB1_VPTX	21.2	mA
USB2_VPTX	21.2	mA
USB1_VDD33	24.5	mA
USB2_VDD33	24.5	mA
USB1_VPH	20.3	mA
USB2_VPH	20.3	mA
PCIE_VP (PCIE1)	38.1	mA
PCIE_VP (PCIE2)	38.1	mA
PCIE_VPH (PCIE1)	43	mA
PCIE_VPH (PCIE2)	43	mA
PCIE_VPTX (PCIE1)	14.3	mA
PCIE_VPTX (PCIE2)	14.3	mA
HDMI_AVDDCLK	95.89	mA
HDMI_AVDDCORE		
HDMI_AVDDIO	6.551	mA
MIPI_VDDA (DSI)	17.1	mA
MIPI_VDDHA (DSI)	4.2	mA
MIPI_VDD (DSI)	14.4	mA
MIPI_VDDPLL (DSI)	3.8	mA
MIPI_VDDA (CSI1/2)	18.79	mA
MIPI_VDDHA (CSI1/2)	2.97	mA
EFUSE_VQPS	96.35	mA

1 Use case dependent

3.1.6 Power modes

The i.MX 8M Dual / 8M QuadLite / 8M Quad processor support the following power modes:

- RUN Mode: All external power rails are on, CPU is active and running; other internal modules can be on/off based on application.
- IDLE Mode: When there is no thread running and all high-speed devices are not active, the CPU can automatically enter this mode. The CPU can be in the power-gated state but with L2 data retained, DRAM and the bus clock are reduced. Most of the internal logic is clock gated but still

3.5.2.1 LPDDR4 mode I/O DC parameters

Table 30. LPDDR4 I/O DC electrical parameters

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1 mA	0.9 x OVDD	—	V
Low-level output voltage	VOL	Iol= 0.1 mA	—	0.1 x OVDD	V
Input Reference Voltage	Vref	—	0.49 x OVDD	0.51 x OVDD	V
DC High-Level input voltage	Vih_DC	—	VRef + 0.100	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	VRef – 0.100	V
Differential Input Logic High	Vih_diff	—	0.26	See note[1]	—
Differential Input Logic Low	Vil_diff	—	See note	-0.26	—
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	–15	15	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	110	175	KΩ
Input current (no pull-up/down)	Iin	VI = 0, VI = OVDD	-2.5	2.5	µA

[1] The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

3.5.3 Differential I/O port (CLKx_P/N)

The clock I/O interface is designed to be compatible with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits* (2001), for details.

The CLK1_P/CLK1_N is input only, while CLK2_P/CLK2_N is output only.

3.6 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for DDR3L/DDR4/LPDDR4 modes
- Differential I/O (CLKx)

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 3 and Figure 4.

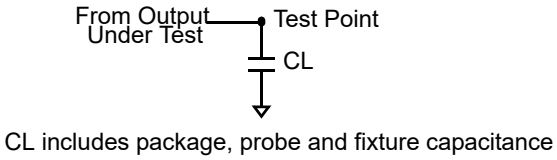

Figure 3. Load circuit for output

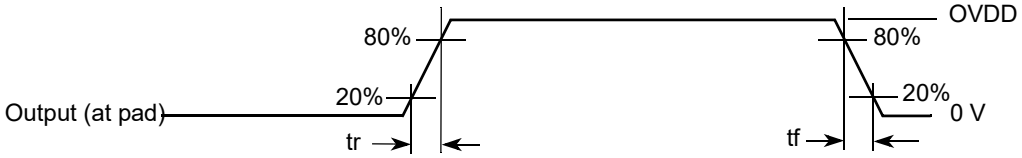

Figure 4. Output transition time waveform

3.6.1 General purpose I/O AC parameters

This section presents the I/O AC parameters for GPIO in different modes. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 31. Maximum input cell delay time

Cell name	Max Delay PAD → Y (ns)		
	V_{DD} = 1.62 V T = 125°C WCS model	—	V_{DD} = 3.0V T = 125°C WCS model
PBIJGTOV36PUD_MCLAMP_LVGPIO_EW	1.54	—	1.3

Table 32. Output cell delay time for fixed load

Parameter			Simulated Cell Delay A → PAD (ns)	
			VDD = 1.62 V, T = 125°C	VDD = 2.97 V, T = 125°C
dse[2:0]	fsel[1:0]	Driver Type	CL = 15 pF	CL = 15 pF
011	00	3 x Slow Slew	3.1	3.3
011	11	3 x Fast Slew	2.1	2.6
100	00	4 x Slow Slew	3.7	3.9
100	11	4 x Fast Slew	2.3	2.8
101	00	5 x Slow Slew	3.1	3.5
101	11	5 x Fast Slew	2.1	2.5

3.7.1 DDR I/O output buffer impedance

Table 35 shows DDR I/O output buffer impedance of i.MX 8M Dual / 8M QuadLite / 8M Quad processors.

Table 35. DDR I/O output buffer impedance

Parameter	Symbol	Test Conditions DSE (Drive Strength)	Typical			Unit
			NVCC_DRAM = 1.35 V (DDR3L) DDR_SEL = 11	NVCC_DRAM = 1.2 V (DDR4)	NVCC_DRAM = 1.1 V (LPDDR4) DDR_SEL = 10	
Output Driver Impedance	Rdrv	000000	Hi-Z	Hi-Z	Hi-Z	Ω
		000010	240	240	240	
		000110	120	120	120	
		001010	80	80	80	
		001110	60	60	60	
		011010	48	48	48	
		011110	40	40	40	
		111010	34	34	34	

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

3.7.2 Differential I/O output buffer impedance

The Differential CCM interface is designed to be compatible with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits* (2001) for details.

3.7.3 USB battery charger detection driver impedance

The USB_OTG1_CHD_B open-drain output pin can be used to signal to power management and monitoring device results of USB Battery Charger detection routines for the USB_OTG1 PHY instance. Use of this pin requires an external pullup resistor, for more information see Table 5.

3.8 System modules timing

This section contains the timing and electrical parameters for the modules in each i.MX 8M Dual / 8M QuadLite / 8M Quad processor.

3.9.2.5 SDR50/SDR104 AC timing

Figure 15 depicts the timing of SDR50/SDR104, and Table 44 lists the SDR50/SDR104 timing characteristics.

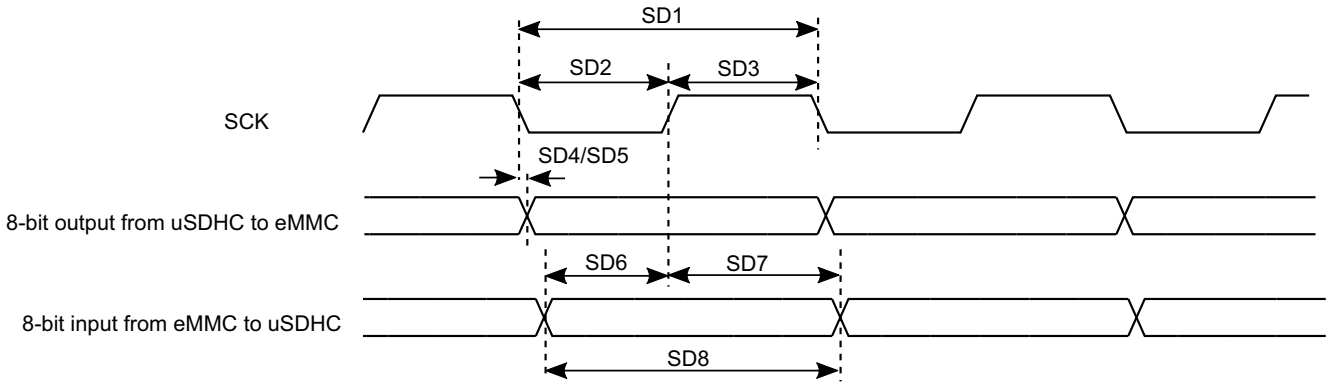

Figure 15. SDR50/SDR104 timing

Table 44. SDR50/SDR104 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	-3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	-1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in DDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.4	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	uSDHC Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1] Data window in SDR100 mode is variable.

3.9.2.6 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2 and NVCC_SD3 supplies are identical to those shown in Table 26, "GPIO DC parameters," on page 29.

5 When the output voltage is between 15% and 85% of the fully settled LP signal levels.
6 Measured as average across any 50 mV segment of the output signal transition.
7 This value represents a corner point in a piecewise linear curve.

3.9.7.3 MIPI LP-RX specifications

Table 55. MIPI low power receiver DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Logic 1 input voltage	880	—	1.3	mV
V_{IL}	Logic 0 input voltage, not in ULP state	—	—	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage, ULP state	—	—	300	mV
V_{HYST}	Input hysteresis	25	—	—	mV

Table 56. MIPI low power receiver AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
e_{SPIKE}[1,2]	Input pulse rejection	—	—	300	V.ps
T_{MIN-RX}[3]	Minimum pulse width response	20	0	0	ns
V_{INT}	Peak Interference amplitude	—	—	200	mV
f_{INT}	Interference frequency	450	—	—	MHz

1 Time-voltage integration of a spike above V_{IL} when in LP-0 state or below V_{IH} when in LP-1 state.
2 An impulse below this value will not change the receiver state.
3 An input pulse greater than this value shall toggle the output.

3.9.7.4 MIPI LP-CD specifications

Table 57. MIPI contention detector DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IHCD}	Logic 1 contention threshold	450	—	—	mV
V_{ILCD}	Logic 0 contention threshold	—	—	200	mV

3.9.7.5 MIPI DC specifications

Table 58. MIPI input characteristics DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{PIN}	Pad signal voltage range	-50	—	1350	mV
I_{LEAK}[1]	Pin leakage current	-30	—	30	µA
V_{GNDSH}	Ground shift	-50	—	50	mV

- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from DQS pad and used to sample input data.

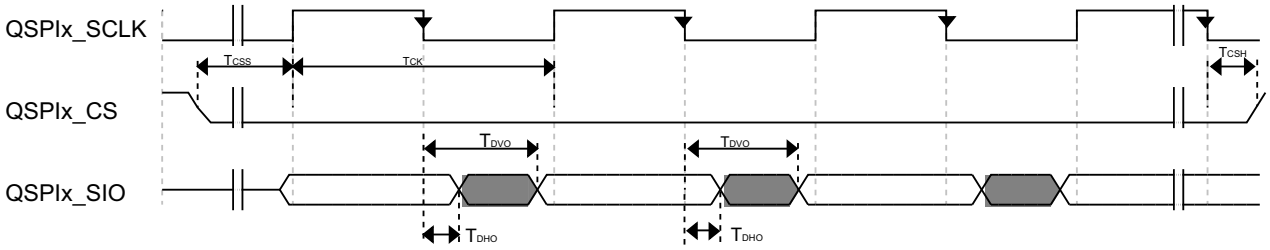

Figure 34. QuadSPI output/write timing (SDR mode)

Table 62. QuadSPI output/write timing (SDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output data valid time	—	2	ns
T_{DHO}	Output data hold time	-0.5	—	ns
T_{CK}	SCK clock period	10	—	ns
T_{CSS}	Chip select output setup time	3	—	ns
T_{CSH}	Chip select output hold time	3	—	ns

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register; the default value of 3 is shown on the timing. See the *i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processor Reference Manual* (IMX8MDQLQRM) for more details.

- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from DQS pad and used to sample input data.

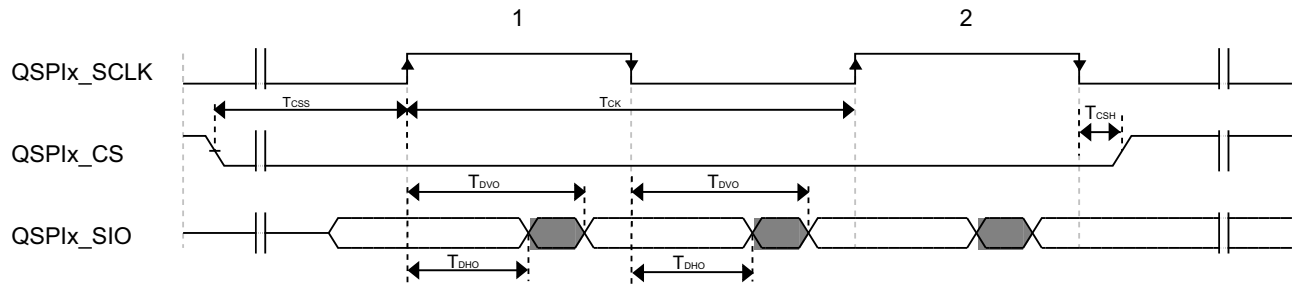

Figure 37. QuadSPI output/write timing (DDR mode)

Table 65. QuadSPI output/write timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output data valid time	—	(0.25 x T_{SCLK}) + 2	ns
T_{DHO}	Output data hold time	(0.25 x T_{SCLK}) - 0.5	—	ns
T_{CK}	SCK clock period	20	—	ns
T_{CSS}	Chip select output setup time	3	—	SCK cycle(s)
T_{CSH}	Chip select output hold time	3	—	ns

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register; the default value of 3 is shown on the timing. See the *i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processor Reference Manual* (IMX8MDQLQRM) for more details.

3.9.11 SAI/I2S switching specifications

This section provides the AC timings for the SAI in Master (clocks driven) and Slave (clocks input) modes. All timings are given for non inverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP] = 0) and non inverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

Table 66. Master mode SAI timing

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	20	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	40	—	ns

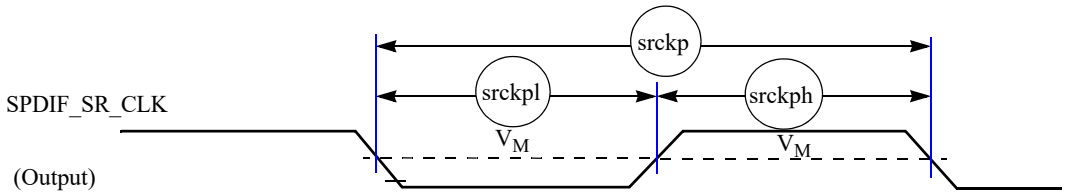

Figure 40. SPDIF_SR_CLK timing diagram

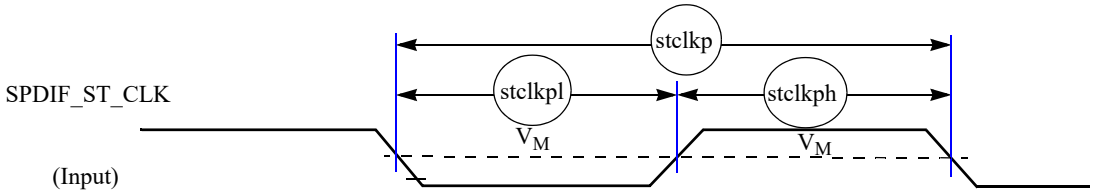

Figure 41. SPDIF_ST_CLK timing diagram

3.9.13 UART I/O configuration and timing parameters

3.9.13.1 UART RS-232 I/O configuration in different modes

The UART interfaces of the i.MX 8M Dual / 8M QuadLite / 8M Quad can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0—DCE mode). Table 69 shows the UART I/O configuration based on the enabled mode.

Table 69. UART I/O configuration vs. mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	UARTx_RTS_B from DTE to DCE	Input	UARTx_RTS_B from DTE to DCE
UARTx_CTS_B	Input	UARTx_CTS_B from DCE to DTE	Output	UARTx_CTS_B from DCE to DTE
UARTx_TX_ DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX _DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

3.9.13.2 UART RS-232 Serial mode timing

This section describes the electrical information of the UART module in the RS-232 mode.

3.9.14 USB PHY parameters

This section describes the USB-OTG PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 3.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 3.0 Specification is not applicable to Host port):

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0, version 1.1a, July 27, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

3.9.14.1 USB_OTG*_REXT reference resistor connection

The bias generation and impedance calibration process for the USB OTG PHYs requires connection of reference resistors 200 Ω 1% precision on each of USB_OTG1_REXT and USB_OTG2_REXT pads to ground.

3.9.14.2 USB_OTG_CHD_B USB battery charger detection external pullup resistor connection

The usage and external resistor connection for the USB_OTG_CHD_B pin are described in Table 5, and Section 3.7.3, “USB battery charger detection driver impedance.”

3.9.15 USB 2.0 PHY parameters

USB 2.0 PHY parameters are compatible with USB 3.0 PHY. See Section 3.9.16, “USB 3.0 PHY parameters for more detailed information.

Table 76. USB power pin supplies (continued)

Pin Name	Description	Value
USB1/2_VPTX	PHY transmit supply	0.9 V (+22.2%, -7%)
USB1/2_VDD33	High supply for high-speed operation IO	3.3 V (+10%, -7%)
USB1/2_VPH	High supply for SuperSpeed operation IO	3.3 V (+10%, -7%)

Table 77 shows the external component values.

Table 77. External component values

Component	Pin Name	Value
External resistor (resref)	USB1_RESREF/USB2_RESREF	200 Ω (±1%)

Table 78 shows the minimum ESD protection target levels.

Table 78. Minimum ESD protection target levels

ESD Category	Minimum Protection Level	JEDEC Class
Human Body Model (HBM) (JS-001-2014)	2 KV	2
Charged Device Model (CDM) (JESD22-C101F)	6 A peak discharge current	C2/C1 (500 V/ 250 V)[1]
Machine Model (MM) (JESD22_A115C)	100 V	N/A

1 Support for either 500 V or 250 V CDM target level is dependent on maximum discharge current generated in final SoC/package implementation.

Table 79 shows the supply impedance requirements.

Table 79. Supply impedance requirements

$L_{gd} + L_{vp}$(nH)	L_{VSSA}<#> + L_{DVDD}(nH)	$L_{gd} + L_{vptx}$<#>(nH)	L_{VSSA}<#> + L_{VDD33} <#>(nH)	$L_{gd} + L_{vph}$(nH)
< 2.4	< 2.4	< 2.4	< 2.8	< 2.8

5.1.2 17 x 17 mm supplies contact assignments and functional contact assignments

Table 82 shows supplies contact assignments for the 17 x 17 mm package.

Table 82. i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm supplies contact assignments

Supply Rail Name	Ball(s) Postion(s)	Remark
EFUSE_VQPS	R17	Supply for eFuse Programming
HDMI_AVDDCLK	V3	Supply for HDMI PHY
HDMI_AVDDCORE	U3, U4	Supply for HDMI PHY
HDMI_AVDDIO	P2	Supply for HDMI PHY
MIPI_VDD	E15, F15	Supply for MIPI PHY
MIPI_VDDA	E17, E18, F17, F18	Supply for MIPI PHY
MIPI_VDDHA	C18, D17, D18	Supply for MIPI PHY
MIPI_VDDPLL	F19	Supply for MIPI PHY
NVCC_DARAM	Y12, Y14, AA10, AA15, AB3, AB8, AB17, AB23, AC3, AC6, AC8, AC14, AC17, AC20, AC23, AD5, AD18, AD21	Supply for DRAM Interface
NVCC_ECSPI	F5	Supply for ESCPI Interface
NVCC_ENET	T18	Supply for ENET Interface
NVCC_GPIO1	R5, R6	Supply for GPIO1 Interface
NVCC_I2C	H7	Supply for I2C Interface
NVCC_JTAG	W4	Supply for JTAG Interface
NVCC_NAND	L18, M18	Supply for NAND Interface
NVCC_SAI1	K3, L3	Supply for SAI Interface
NVCC_SAI2	J7	Supply for SAI Interface
NVCC_SAI3	E3	Supply for SAI Interface
NVCC_SAI5	M3	Supply for SAI Interface
NVCC_SD1	L23, M23	Supply for SD Interface
NVCC_SD2	N23	Supply for SD Interface
NVCC_SNVS	W18	Supply for SNVS Interface
NVCC_UART	D8	Supply for UART Interface
PCIE_VP	F22, G22	Supply for PCIe PHY
PCIE_VPH	H23, J23	Supply for PCIe PHY
PCIE_VPTX	F23, G23	Supply for PCIe PHY
USB1_DVDD	E12	Supply for USB PHY
USB1_VDD33	G12	Supply for USB PHY
USB1_VP	D12	Supply for USB PHY

Table 83. i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type[1]	Reset condition[2]			
				Default mode (Reset mode)	Default function (Signal name)	Input/ Output	Value
DRAM_DQ09	AA22	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ10	AA23	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ11	AA20	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ12	AA18	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ13	AB19	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ14	AA19	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ15	AA17	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ16	AE3	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ17	AD2	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ18	AE4	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ19	AD4	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ20	AA2	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ21	Y1	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ22	AA1	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ23	AB1	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ24	AB4	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ25	AA4	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ26	AA3	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ27	AA6	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ28	AA8	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ29	AB7	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ30	AA7	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQ31	AA9	NVCC_DRAM	DDR	—	—	—	—
DRAM_DQS0_N	AC25	NVCC_DRAM	DDRCLK	—	—	—	—
DRAM_DQS0_P	AC24	NVCC_DRAM	DDRCLK	—	—	—	—
DRAM_DQS1_N	AC21	NVCC_DRAM	DDRCLK	—	—	—	—
DRAM_DQS1_P	AB21	NVCC_DRAM	DDRCLK	—	—	—	—
DRAM_DQS2_N	AC1	NVCC_DRAM	DDRCLK	—	—	—	—
DRAM_DQS2_P	AC2	NVCC_DRAM	DDRCLK	—	—	—	—
DRAM_DQS3_N	AC5	NVCC_DRAM	DDRCLK	—	—	—	—

Table 83. i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type[1]	Reset condition[2]			
				Default mode (Reset mode)	Default function (Signal name)	Input/ Output	Value
DRAM_DQS3_P	AB5	NVCC_DRAM	DDRCLK	—	—	—	—
DRAM_RESET_N	AB13	NVCC_DRAM	DDR	—	—	—	—
DRAM_VREF	AA14	NVCC_DRAM	DDR	—	—	—	—
DRAM_ZN	AA13	NVCC_DRAM	DDR	—	—	—	—
ECSPI1_MISO	B4	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[8]	Input	PD (90 K)
ECSPI1_MOSI	A4	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[7]	Input	PD (90 K)
ECSPI1_SCLK	D5	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[6]	Input	PD (90 K)
ECSPI1_SS0	D4	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[9]	Input	PD (90 K)
ECSPI2_MISO	B5	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[12]	Input	PD (90 K)
ECSPI2_MOSI	E5	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[11]	Input	PD (90 K)
ECSPI2_SCLK	C5	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[10]	Input	PD (90 K)
ECSPI2_SS0	A5	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[13]	Input	PD (90 K)
ENET_MDC	N20	NVCC_ENET	GPIO	ALT5	GPIO1.IO[16]	Input	PD (90 K)
ENET_MDIO	N19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[17]	Input	PD (90 K)
ENET_RD0	U19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[26]	Input	PD (90 K)
ENET_RD1	U21	NVCC_ENET	GPIO	ALT5	GPIO1.IO[27]	Input	PD (90 K)
ENET_RD2	U20	NVCC_ENET	GPIO	ALT5	GPIO1.IO[28]	Input	PD (90 K)
ENET_RD3	V19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[29]	Input	PD (90 K)
ENET_RXC	T20	NVCC_ENET	GPIO	ALT5	GPIO1.IO[25]	Input	PD (90 K)
ENET_RX_CTL	T21	NVCC_ENET	GPIO	ALT5	GPIO1.IO[24]	Input	PD (90 K)
ENET_TD0	R20	NVCC_ENET	GPIO	ALT5	GPIO1.IO[21]	Input	PD (90 K)
ENET_TD1	R21	NVCC_ENET	GPIO	ALT5	GPIO1.IO[20]	Input	PD (90 K)
ENET_TD2	R19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[19]	Input	PD (90 K)
ENET_TD3	P20	NVCC_ENET	GPIO	ALT5	GPIO1.IO[18]	Input	PD (90 K)
ENET_TXC	T19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[23]	Input	PD (90 K)
ENET_TX_CTL	P19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[22]	Input	PD (90 K)
GPIO1_IO00	T6	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[0]	Input	PD (90 K)
GPIO1_IO01[3]	T7	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[1]	Input	PD (90 K)
GPIO1_IO02	R4	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[2]	Input	PD (27 K)
GPIO1_IO03	P4	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[3]	Input	PD (90 K)

Table 83. i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type[1]	Reset condition[2]			
				Default mode (Reset mode)	Default function (Signal name)	Input/ Output	Value
MIPI_CSI2_D2_P	B21	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI2_D3_N	C19	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI2_D3_P	D19	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_CLK_N	C16	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_CLK_P	D16	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D0_N	A17	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D0_P	B17	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D1_N	A16	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D1_P	B16	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D2_N	A18	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D2_P	B18	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D3_N	A15	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D3_P	B15	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_REXT	C17	MIPI_VDDHA	PHY	—	—	—	—
NAND_ALE	G19	NVCC_NAND	GPIO	ALT5	GPIO3.IO[0]	Input	PD (90 K)
NAND_CE0_B	H19	NVCC_NAND	GPIO	ALT5	GPIO3.IO[1]	Input	PD (90 K)
NAND_CE1_B	G21	NVCC_NAND	GPIO	ALT5	GPIO3.IO[2]	Input	PD (90 K)
NAND_CE2_B	F21	NVCC_NAND	GPIO	ALT5	GPIO3.IO[3]	Input	PD (90 K)
NAND_CE3_B	H20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[4]	Input	PD (90 K)
NAND_CLE	H21	NVCC_NAND	GPIO	ALT5	GPIO3.IO[5]	Input	PD (90 K)
NAND_DATA00	G20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[6]	Input	PD (90 K)
NAND_DATA01	J20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[7]	Input	PD (90 K)
NAND_DATA02	H22	NVCC_NAND	GPIO	ALT5	GPIO3.IO[8]	Input	PD (90 K)
NAND_DATA03	J21	NVCC_NAND	GPIO	ALT5	GPIO3.IO[9]	Input	PD (90 K)
NAND_DATA04	L20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[10]	Input	PD (90 K)
NAND_DATA05	J22	NVCC_NAND	GPIO	ALT5	GPIO3.IO[11]	Input	PD (90 K)
NAND_DATA06	L19	NVCC_NAND	GPIO	ALT5	GPIO3.IO[12]	Input	PD (90 K)
NAND_DATA07	M19	NVCC_NAND	GPIO	ALT5	GPIO3.IO[13]	Input	PD (90 K)
NAND_DQS	M20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[14]	Input	PD (90 K)
NAND_RE_B	K19	NVCC_NAND	GPIO	ALT5	GPIO3.IO[15]	Input	PD (90 K)

Table 84. 17 x 17 mm, 0.65 mm pitch ball map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
U	HDMI_TX_M_LN_1	HDMI_TX_P_LN_1	HDMI_AVDDCORE	HDMI_AVDDCORE	JTAG_TDO	JTAG_TRST_B	JTAG_MOD	VSS	VSS	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VSS	VSSA_FPLL	VDDA_1P8_FPLL	VSS	ENET_RD0	ENET_RD2	ENET_RD1	CLK2_N	VDDA_1P8_LVDS	XTALO_25M	XTALI_25M
V	HDMI_AUX_P	HDMI_AUX_N	HDMI_AVDDCLK	VSS	JTAG_TMS	BOOT_MODE1	TEST_MODE	VSS	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VSS	VSSA_SPLL	VDDA_0P9	ENET_RD3	PMIC_ON_REQ	PMIC_STBY_REQ	RTC	VSSA_XTAL_25M	XTALO_27M	XTALI_27M
W	VSS	HDMI_HPD	HDMI_CEC	NVCC_JTAG	JTAG_TDI	BOOT_MODE0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDA_1P8_SPLL	NVCC_SNVS	RTC_RESET_B	POR_B	ONOFF	VSSA_XTAL_27M	VDDA_1P8_XTAL_27M	VDDA_1P8_XTAL_25M	VSS
Y	DRAM_DQ21	VSS	VSS	VSS	VSS	VDD_DRAM	VSS	VDD_DRAM	VSS	VDD_DRAM	VSS	NVCC_DRAM	VSS	NVCC_DRAM	VSS	VDD_DRAM	VSS	VDD_DRAM	VSS	VDD_DRAM	VSS	VSS	VSS	VSS	DRAM_DQ05
AA	DRAM_DQ22	DRAM_DQ20	DRAM_DQ26	DRAM_DQ25	VSS	DRAM_DQ27	DRAM_DQ30	DRAM_DQ28	DRAM_DQ31	NVCC_DRAM	VDDA_DRAM	DRAM_AC27	DRAM_ZN	DRAM_VREF	NVCC_DRAM	VSS	DRAM_DQ15	DRAM_DQ12	DRAM_DQ14	DRAM_DQ11	VSS	DRAM_DQ09	DRAM_DQ10	DRAM_DQ04	DRAM_DQ06
AB	DRAM_DQ23	VSS	NVCC_DRAM	DRAM_DQ24	DRAM_DQS3_P	DRAM_DM3	DRAM_DQ29	NVCC_DRAM	VSS	DRAM_AC35	VSS	DRAM_AC26	DRAM_RESET_N	DRAM_AC19	DRAM_AC07	DRAM_AC14	NVCC_DRAM	VSS	DRAM_DQ13	DRAM_DM1	DRAM_DQS1_P	DRAM_DQ08	NVCC_DRAM	VSS	DRAM_DQ07
AC	DRAM_DQS2_N	DRAM_DQS2_P	NVCC_DRAM	VSS	DRAM_DQS3_N	NVCC_DRAM	DRAM_AC28	NVCC_DRAM	DRAM_AC23	DRAM_AC34	DRAM_AC38	DRAM_AC36	DRAM_ALERT_N	NVCC_DRAM	DRAM_AC15	DRAM_AC00	NVCC_DRAM	DRAM_AC03	VSS	NVCC_DRAM	DRAM_DQS1_N	VSS	NVCC_DRAM	DRAM_DQS0_P	DRAM_DQS0_N

Table 85. DDR pin function list for 17 x 17 mm package (continued)

DRAM_DQ15	DQ15_A	DQU7_A	DQU7_A	AA17
DRAM_DQS2_P	DQS0_t_B	DQSL_t_B	DQSL_B	AC2
DRAM_DQS2_N	DQS0_c_B	DQSL_c_B	DQSL#_B	AC1
DRAM_DM2	DMI0_B	DML_n_B / DBIL_n_B	DML_B	AD3
DRAM_DQ16	DQ0_B	DQL0_B	DQL0_B	AE3
DRAM_DQ17	DQ1_B	DQL1_B	DQL1_B	AD2
DRAM_DQ18	DQ2_B	DQL2_B	DQL2_B	AE4
DRAM_DQ19	DQ3_B	DQL3_B	DQL3_B	AD4
DRAM_DQ20	DQ4_B	DQL4_B	DQL4_B	AA2
DRAM_DQ20	DQ4_B	DQL4_B	DQL4_B	AA2
DRAM_DQ21	DQ5_B	DQL5_B	DQL5_B	Y1
DRAM_DQ22	DQ6_B	DQL6_B	DQL6_B	AA1
DRAM_DQ23	DQ7_B	DQL7_B	DQL7_B	AB1
DRAM_DQS3_P	DQS1_t_B	DQSU_t_B	DQSU_B	AB5
DRAM_DQS3_N	DQS1_c_B	DQSU_c_B	DQSU#_B	AC5
DRAM_DM3	DMI1_B	DMU_n_B / DBIU_n_B	DMU_B	AB6
DRAM_DQ24	DQ08_B	DQU0_B	DQU0_B	AB4
DRAM_DQ25	DQ09_B	DQU1_B	DQU1_B	AA4
DRAM_DQ26	DQ10_B	DQU2_B	DQU2_B	AA3
DRAM_DQ27	DQ11_B	DQU3_B	DQU3_B	AA6
DRAM_DQ28	DQ12_B	DQU4_B	DQU4_B	AA8
DRAM_DQ29	DQ13_B	DQU5_B	DQU5_B	AB7
DRAM_DQ30	DQ14_B	DQU6_B	DQU6_B	AA7
DRAM_DQ31	DQ15_B	DQU7_B	DQU7_B	AA9
DRAM_RESET_N	RESET_N	RESET_N	RESET#	AB13
DRAM_ALERT_N	MTEST1	ALERT_n / MTEST1	MTEST1	AC13
DRAM_AC00	CKE0_A	CKE0	CKE0	AC16
DRAM_AC01	CKE1_A	CKE1	CKE1	AE17
DRAM_AC02	CS0_A	CS0_n	CS0#	AE18
DRAM_AC03	CS1_A	C0	—	AC18
DRAM_AC04	CK_t_A	BG0	BA2	AD14
DRAM_AC05	CK_c_A	BG1	A14	AE14
DRAM_AC06	—	ACT_n	A15	AE13
DRAM_AC07	—	A9	A9	AB15