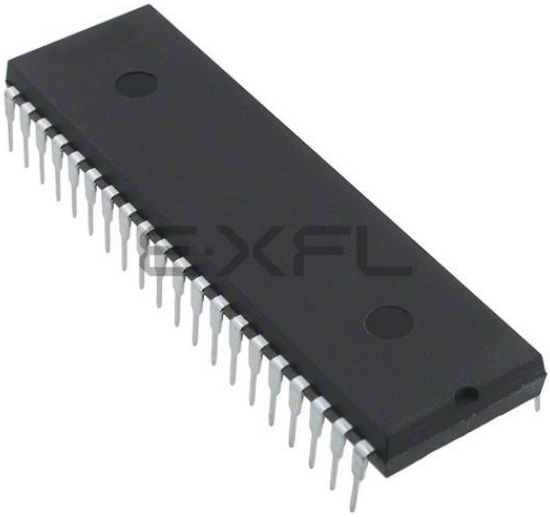

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Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
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Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n78e059adg

5.2 External Program Memory

N78E059A/N78E055A is a 16-bit address-width CPU. It can address 64k-byte program code. Besides the internal Program Memory, the external additional Program Memory is also can be used. The external program addressing will be executed under cases below,

1. The PC (Program Counter) value is beyond the boundary size address of APROM or LDROM while $\overline{EA}$ pin is pulled high during power on. The CPU will continue to fetch the external Program Memory.

2. While $\overline{EA}$ pin is pulled low during power on period, The CPU will run totally 64k-byte code externally.

While the external mode is running, the P0 and P2 will produce address and data signals to fetching external Program Memory. In this case, P0 and P2 cannot be general purpose I/O anymore. $\overline{PSEN}$ will also toggle out to strobe the external Program Memory. For the hardware circuit for external program execution, see Figure 5–2. Program Memory Interface.

For security $\overline{EA}$ pin state will be locked after power on. The user cannot switch the program running internally or externally by $\overline{EA}$ after power on. The other design for data security is MOVC lock enable (MOVCL, CONFIG0.2). While this bit is set 0, The external Program Memory code is inhibited to read internal APROM or LDROM contents through MOVC instruction.

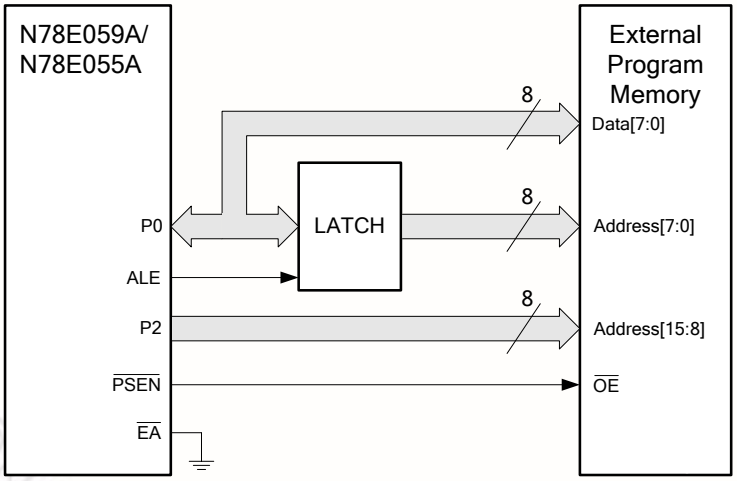

Figure 5–2. Program Memory Interface

5.3 Internal Data Memory

Figure 5–3 shows the internal and external Data Memory spaces available on N78E059A/N78E055A. Internal Data Memory can be divided into three blocks. They are the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128 bytes of SFR space. Internal Data Memory addresses are always 8-bit wide, which implies an address space of only 256 bytes. Direct addressing higher than 7FH will access the special function registers (SFRs) space and indirect addressing higher than 7FH will access the upper 128 bytes of RAM. Although the SFR space and the upper 128 bytes of RAM share the same logic address, 80H through FFH, actually they are physically separate entities. Direct addressing to distinguish with the higher 128 bytes of RAM can only access these SFRs. Sixteen addresses in SFR space are both byte and bit-addressable. The bit-addressable SFRs are those whose addresses end in 0H or 8H.

The lower 128 bytes of internal RAM are present in all 8051 devices. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call these registers as R0 through R7. Two bits RS0 and RS1 in the Program Status Word (PSW[3:4]) select which Register Bank is used. This benefits more efficiency of code space, since register instructions are shorter than instructions that use direct addressing. The next 16 bytes above the Register Banks (byte-address 20H through 2FH) form a block of bit-addressable memory space (bit-address 00H through 7FH). The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All bytes in the lower 128-byte space can be accessed by either direct or indirect addressing. Indirect addressing can only access the upper 128.

Another application implemented with the whole block of internal 256-byte RAM is for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a JMP, CALL or interrupt is invoked, the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07H at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

Table 6–2. N78E059A/N78E055A SFR Descriptions and Reset Values

Symbol	Definition	Address	MSB							LSB[1]	Reset Value[2]
SPDR	SPI data	F5H									0000 0000b
SPSR	SPI status	F4H	SPIF	WCOL	SPIOVF	MODF	DISMODF	-	-	-	0000 0000b
SPCR	SPI control	F3H	SSOE	SPIEN	LSBFE	MSTR	CPOL	CPHA	SPR1	SPR0	0000 0000b
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	0000 0000b
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	0000 0000b
PWM3	PWM3 duty	DEH									0000 0000b
PWM2	PWM2 duty	DDH									0000 0000b
PWMCON0	PWM control 0	DCH	PWM3OE	PWM2OE	PWM3EN	PWM2EN	PWM1OE	PWM0OE	PWM1EN	PWM0EN	0000 0000b
PWM1	PWM1 duty	DBH									0000 0000b
PWM0	PWM0 duty	DAH									0000 0000b
PWMP	PWM period	D9H									0000 0000b
P4	Port 4	D8H	(DF)	(DE)	(DD)	(DC)	(DB) $\overline{\text{INT2}}$	(DA) $\overline{\text{INT3}}$	(D9)	(D8)	1111 1111b
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	0000 0000b
PWM4	PWM4 duty	CFH									0000 0000b
PWMCON1	PWM control 1	CEH	-	-	-	-	-	PWM4OE	-	PWM4EN	0000 0000b
TH2	Timer 2 high byte	CDH									0000 0000b
TL2	Timer 2 low byte	CCH									0000 0000b
RCAP2H	Timer 2 reload/capture high byte	CBH									0000 0000b
RCAP2L	Timer 2 reload/capture low byte	CAH									0000 0000b
T2MOD	Timer 2 mode	C9H	-	-	-	-	-	-	T2OE	-	0000 0000b
T2CON	Timer 2 control	C8H	(CF) TF2	(CE) EXF2	(CD) RCLK	(CC) TCLK	(CB) EXEN2	(CA) TR2	(C9) $\overline{\text{C/T2}}$	(C8) $\overline{\text{CP/RL2}}$	0000 0000b
TA	Timed access protection	C7H									0000 0000b
XICON	External interrupt control	C0H	(C7) PX3	(C6) EX3	(C4) IE3	(C4) IT3	(C3) PX2	(C2) EX2	(C1) IE2	(C0) 1IT2	0000 0000b
EIE	Extensive interrupt enable	BDH	-	-	-	-	-	EBOD	EPDT	ESPI	0000 0000b
EIP	Extensive interrupt priority	BCH	-	-	-	-	-	PBOV	PPDT	PSPI	0000 0000b
EIPH	Extensive interrupt priority high	BBH	-	-	-	-	-	PBODH	PPDTH	PSPIH	0000 0000b
IPH	Interrupt priority high	BAH	PX3H	PX2H	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	0000 0000b
IP	Interrupt priority	B8H	(BF) -	(BE) -	(BD) PT2	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	0000 0000b
P3	Port 3	B0H	(B7) $\overline{\text{RD}}$	(B6) $\overline{\text{WR}}$	(B5) T1	(B4) T0	(B3) $\overline{\text{INT1}}$	(B2) $\overline{\text{INT0}}$	(B1) TXD	(B0) RXD	1111 1111b
ISPCN	ISP flash control	AFH	ISPA17	ISPA16	FOEN	FCEN	FCTRL3	FCTRL2	FCTRL1	FCTRL0	0000 0000b
ISPFD	ISP flash data	AEH									0000 0000b
PMC[3]	Power monitoring control	ACH	BODEN	-	-	BORST	BOF[4]	LPBOD	-	BOS[5]	Power-on[6], XXXX X00Xb Brown-out, XXXX 100Xb Others, XXXX 000Xb
PDCON	Power Down waking-up timer control	ABH	PDTEN	PDTCK	PDTF	-	-	PPS2	PPS1	PPS0	0000 0000b
WDCON[3]	Watchdog Timer control	AAH	WDTEN	WDCLR	-	WIDPD	WDTRF	WPS2	WPS1	WPS0	Power-on[6], X000 0000b Watchdog, X00U 1UUUb Others, X00U UUUUb
IE	Interrupt enable	A8H	(AF) EA	(AE) -	(AD) ET2	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000b
ISPAH	ISP address high byte	A7H									0000 0000b
ISPAL	ISP address low byte	A6H									0000 0000b
ISPTRG[3]	ISP trigger	A4H	-	-	-	-	-	-	-	ISPGO	0000 0000b
XRAMAH	Auxiliary RAM address high byte	A1H	-	-	-	-	-	-	XRAMAH.1	XRAMAH.0	0000 0000b
P2	Port 2	A0H	(A7) A15	(A6) A14	(A5) A13	(A4) A12	(A3) A11	(A2) A10	(A1) A9	(A0) A8	1111 1111b

DPH – Data Pointer High Byte

7	6	5	4	3	2	1	0
DPH[7:0]							
r/w							

Address: 83H reset value: 0000 0000b

Bit	Name	Description
7:0	DPH[7:0]	**Data pointer high byte.** This is the high byte of the standard 8051 16-bit data pointer. DPH combined with DPL serve as a 16-bit data pointer DPTR to address non-scratch-pad memory or Program Memory.

PSW – Program Status Word (bit-addressable)

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	P
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r

Address: D0H reset value: 0000 0000b

Bit	Name	Description
7	CY	**Carry flag.** For a adding or subtracting operation, CY will be set when the previous operation resulted in a carry-out from or a borrow-in to the Most Significant bit, otherwise cleared. If the previous operation is MUL or DIV, CY is always 0. CY is affected by DA A instruction which indicates that if the original BCD sum is greater than 100. For a CJNE branch, CY will be set if the first unsigned integer value is less than the second one. Otherwise, CY will be cleared.
6	AC	**Auxiliary carry.** Set when the previous operation resulted in a carry-out from or a borrow-in to the 4th bit of the low order nibble, otherwise cleared.
5	F0	**User flag 0.** The general purpose flag that can be set or cleared by the user.
4	RS1	**Register Bank selecting bits.** These two bits select one of four banks in which R0~R7 locate.
3	RS0	

RS1	RS0	Register Bank	RAM Address
0	0	0	00~07H
0	1	1	08~0FH
1	0	2	10~17H
1	1	3	18~1FH

Table 11–1. Watchdog Timer-Out Interval under different pre-scalars

WPS2	WPS1	WPS0	Clock Divider Scale	Typical Watchdog Time-out Interval (F_{ILRC} ~= 10kHz)
0	0	0	1/1	6.40ms
0	0	1	1/2	12.80ms
0	1	0	1/8	51.20ms
0	1	1	1/16	102.40ms
1	0	0	1/32	204.80ms
1	0	1	1/64	409.60ms
1	1	0	1/128	819.20ms
1	1	1	1/256	1.638s

11.2 Applications of Watchdog Timer

The main application of the Watchdog Timer is for the system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, the processor may begin to execute erroneous codes and operate in an unpredictable state. If this is left unchecked the entire system may crash. Using the Watchdog Timer during software development will require the user to select ideal watchdog reset locations for inserting instructions to reset the Watchdog Timer. By inserting the instruction setting WDCLR, it will allow the code to run without any Watchdog Timer reset. However If any erroneous code executes by any power of other interference, the instructions to clear the Watchdog Timer counter will not be executed at the required instants. Thus the Watchdog Timer reset will occur to reset the system start from an erroneously executing condition. The user should remember that WDCON requires a timed access writing.

13. SERIAL PORT

N78E059A/N78E055A includes one enhanced full duplex serial port. The serial port supports three modes of full duplex UART (Universal Asynchronous Receiver and Transmitter) in Mode 1, 2, and 3. This means it can transmit and receive simultaneously. The serial port is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. The serial port receive and transmit registers are both accessed at SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register. There are four operation modes in serial port. In all four modes, transmission initiates by any instruction that uses SBUF as a destination register. Note that before serial port function works, the port latch bits of P3.0 and P3.1 (for RXT and TXD pins) have to be set to 1.

SCON – Serial Port Control (bit-addressable)

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: 98H reset value: 0000 0000b

Bit	Name	Description
7	SM0	**Serial port mode select.** See Table 13–1. Serial Port Mode Description for details.
6	SM1	
5	SM2	**Multiprocessor communication mode enable.** The function of this bit is dependent on the serial port mode. Mode 0: This bit has no effect. Mode 1: This bit checks valid stop bit. 0 = Reception is always valid no matter the logic level of stop bit. 1 = Reception is ignored if the received stop bit is not logic 1. Mode 2 or 3: For multiprocessor communication. 0 = Reception is always valid no matter the logic level of the 9th bit. 1 = Reception is ignored if the received 9th bit is not logic 1.
4	REN	**Receive enable.** 0 = Disable serial port reception. 1 = Enable serial port reception in Mode 1,2, and 3. In Mode 0, clearing and then setting REN initiates one-byte reception. After reception is complete, this bit will not be cleared via hardware. The user should clear and set REN again via software to triggering the next byte reception.
3	TB8	**9th transmit bit.** This bit defines the state of the 9th transmission bit in serial port Mode 2 and 3. It is not used in Mode0 and 1.

Transmission is initiated by any writing instructions to SBUF. Transmission takes place on TXD pin. First the start bit comes out, the 8-bit data and bit TB8 (SCON.3) follows to be shifted out and then ends with a stop bit. After the stop bit appears, TI will be set to indicate the transmission complete.

While REN is set, the reception is allowed at any time. A falling edge of a start bit on RXD will initiate the reception progress. Data will be sampled and shifted in at the selected baud rate. In the midst of the 9th bit, certain conditions must be met to load SBUF with the received data:

1. RI (SCON.0) = 0, and

2. Either SM2(SCON.5) = 0, or the received 9th bit = 1 while SM2 = 1.

If these conditions are met, then the SBUF will be loaded with the received data, the RB8(SCON.2) with TB8 bit and RI will be set. If these conditions fail, there will be no data loaded and RI will remain 0. After above receiving progress, the serial control will look forward another 1-0 transition on RXD pin in order to start next data reception.

13.4 Mode 3

Mode 3 has the same operation as Mode 2, except its baud rate clock source. As shown is Figure 13–4, Mode 3 uses Timer 1 or Timer 2 overflow as its baud rate clock.

TH1 reload value	Oscillator Frequency (MHz)				
	11.0592	14.7456	18.432	22.1184	36.864
Baud Rate					
9600	FDh	FCh	FBh	FAh	F6h
4800	FAh	F8h	F6h	F4h	ECh
2400	F4h	F0h	ECh	E8h	D8h
1200	E8h	E0h	D8h	D0h	B0h
300	A0h	80h	60h	40h	

Table 13–4. Timer 2 Generated Commonly Used Baud Rates

RCAP2H, RCAP2L reload value	Oscillator Frequency (MHz)				
	11.0592	14.7456	18.432	22.1184	36.864
Baud Rate					
115200	FFh, FDh	FFh, FCh	FFh, FBh	FFh, FAh	FFh, F6h
57600	FFh, FAh	FFh, F8h	FFh, F6h	FFh, F4h	FFh, ECh
38400	FFh, F7h	FFh, F4h	FFh, F1h	FFh, EEh	FFh, E2h
19200	FFh, EEh	FFh, E8h	FFh, E2h	FFh, DCh	FFh, C4h
9600	FFh, DCh	FFh, D0h	FFh, C4h	FFh, B8h	FFh, 88h
4800	FFh, B8h	FFh, A0h	FFh, 88h	FFh, 70h	FFh, 10h
2400	FFh, 70h	FFh, 40h	FFh, 10h	FEh, E0h	FEh, 20h
1200	FEh, E0h	FEh, 80h	FEh, 20h	FDh, C0h	FCh, 40h
300	FBh, 80h	FAh, 00h	F8h, 80h	F7h, 00h	F1h, 00h

13.6 Multiprocessor Communication

N78E059A/N78E055A multiprocessor communication feature of UART lets a Master device send a multiple frame serial message to a Slave device in a multi-slave configuration. It does this without interrupting other slave devices that may be on the same serial line. This feature can be used only in UART mode 2 or 3 mode. After 9 data bits are received. The 9th bit value is written to RB8 (SCON.2). The user can enable this function by setting SM2 (SCON.5) as a logic 1 so that when the stop bit is received, the serial interrupt will be generated only if RB8 is 1. When the SM2 bit is 1, serial data frames that are received with the 9th bit as 0 do not generate an interrupt. In this case, the 9th bit simply separates the address from the serial data.

When the Master device wants to transmit a block of data to one of several slaves on a serial line, it first sends out an address byte to identify the target slave. Note that in this case, an address byte differs from a data byte: In an address byte, the 9th bit is 1 and in a data byte, it is 0. The address byte interrupts all slaves so that each slave can examine the received byte and see if it is being addressed. The addressed slave then clears its SM2

Most of interrupt flags must be cleared by writing it as a logic 0 via software. Without clearing the flag, the ISR of corresponding interrupt source will execute again and again non-stopped.

17.1 Priority Level Structure

There are four priority levels for the interrupts, highest, high, low, and lowest. The interrupt sources can be individually set to one of four priority levels by setting their own priority bits. Table 17–2 lists four priority setting. Naturally, a low priority interrupt can itself be interrupted by a high priority interrupt, but not by another same level interrupt or lower level. A highest priority can't be interrupted by any other interrupt source. In addition, there exists a pre-defined hierarchy among the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown on Table 17–3. It also summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, natural priority and the permission to wake up the CPU from Power Down mode. For details of waking CPU up from Power Down mode, please see Section 19.2 "Power Down Mode" on page 100.

Table 17–2. Interrupt Priority Level Setting

Interrupt Priority Control Bits		Interrupt Priority Level
IPH / EIPH	IP / EIP / XICON[7,3]	
0	0	Level 0 (lowest)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest)

Table 17–3. Characteristics of Each Interrupt Source

Source	Vector Address	Flag	Enable Bit	Natural Priority	Priority Control Bits	Power Down Waking up
External interrupt 0	0003H	IE0[1]	EX0	1	PX0, PX0H	Yes
Timer 0 overflow	000BH	TF0[2]	ET0	2	PT0, PT0H	No
External interrupt 1	0013H	IE1[1]	EX1	3	PX1, PX1H	Yes
Timer 1 overflow	001BH	TF1[2]	ET1	4	PT1, PT1H	No
Serial port (UART)	0023H	RI + TI	ES	5	PS, PSH	No
Timer 2 overflow / capture / reload	002BH	TF2[2] + EXF2	ET2	6	PT2, PT2H	No
External interrupt 2	0033H	IE2[1]	EX2	7	PX2, PX2H	Yes
External interrupt 3	003BH	IE3[1]	EX3	8	PX3, PX3H	Yes

18. IN SYSTEM PROGRAMMING (ISP)

The internal Program Memory and on-chip Data Flash support both hardware programming and in system programming (ISP). Hardware programming mode uses gang-writers to reduce programming costs and time to market while the products enter into the mass production state. However, if the product is just under development or the end product needs firmware updating in the hand of an end user, the hardware programming mode will make repeated programming difficult and inconvenient. ISP method makes it easy and possible. N78E059A/N78E055A supports ISP mode allowing a device to be reprogrammed under software control. Furthermore, the capability to update the application firmware makes wide range of applications possible.

ISP is performed without removing the microcontroller from the system. The most common method to perform ISP is via UART along with the firmware in LDROM. General speaking, PC transfers the new APROM code through serial port. Then LDROM firmware receives it and re-programs into APROM through ISP commands. Nuvoton provides ISP firmware, USB ISP writer and PC application program for N78E059A/N78E055A. It makes users quite easy perform ISP through Nuvoton standard ISP tool. Please explore Nuvoton 8-bit Microcontroller website: Nuvoton 80C51 Microcontroller Development Tool.

18.1 ISP Procedure

Unlike RAM's real-time operation, to update flash data often takes long time. Furthermore, it is a quite complex timing procedure to erase, program, or read flash data. Fortunately, N78E059A/N78E055A carried out the flash operation with convenient mechanism to help the user update the flash content. After ISP enabled by setting ISPEN (CHPCON.0 with TA protected), the user can easily fill the 16-bit target address in ISPAH and ISPAL, data in ISPFD and command in ISPCN. Then the ISP is ready to begin by setting a triggering bit ISPGO (ISPTRG.0). Note that ISPTRG is also TA protected. At this moment, the CPU holds the Program Counter and the built-in ISP automation takes over to control the internal charge-pump for high voltage and the detail signal timing. After ISP action completed, the Program Counter continues to run the following instructions. The ISPGO bit will be automatically cleared. The user may repeat steps above for next ISP action if necessary. Through this progress, the user can easily erase, program, and verify the embedded flash by just taking care of the pure software.

The following registers relate to ISP processing.

CHPCON – Chip Control (TA protected)

7	6	5	4	3	2	1	0
SWRST	ISPF	LDUEN	XRAMEN	-	-	BS	ISPEN
w	r/w	r/w	r/w	-	-	r/w	r/w

Address: 9FH reset value: see Table 6–2. N78E059A/N78E055A SFR Descriptions and Reset Values

Bit	Name	Description
6	ISPF	**ISP fault flag.** The hardware will set this bit when any of the following condition is met: 1. The accessing area is illegal, such as, (a) Erasing or programming APROM itself when APROM code runs. (b) Erasing or programming LDROM when APROM code runs but LDUEN is 0. (c) Erasing, programming, or reading CONFIG bytes when APROM code runs. (d) Erasing or programming LDROM itself when LDROM code runs. (e) Accessing oversize. 2. The ISP operating runs from internal Program Memory into external one. This bit should be cleared via software.
5	LDUEN	**Updating LDROM enable.** 0 = The LDROM is inhibited to be erased or programmed when APROM code runs. LDROM remains read-only. 1 = The LDROM is allowed to be fully accessed when APROM code runs.
0	ISPEN	**ISP enable.** 0 = Enable ISP function. 1 = Disable ISP function. To enable ISP function will start the internal 22.1184MHz RC oscillator for timing control. To clear ISPEN should always be the last instruction after ISP operation in order to stop internal RC for reducing power consumption.

ISPCN – ISP Control

7	6	5	4	3	2	1	0
ISPA.17	ISPA.16	FOEN	FCEN	FCTRL.3	FCTRL.2	FCTRL.1	FCTRL.0
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: AFH reset value: 0000 0000b

Bit	Name	Description
7:6	ISPA[17:16]	**ISP control.** This byte is for ISP controlling command to decide ISP destinations and actions. For details, see Table 18–1. ISP Modes and Command Codes.
5	FOEN	
4	FCEN	
3:0	FCTRL[3:0]	

18.2 ISP Commands

N78E059A/N78E055A provides a wide application to perform ISP to APROM, LDROM or on-chip Data Flash. The ISP action mode and the destination of the flash block are defined by ISP control register ISPCN.

Table 18–1. ISP Modes and Command Codes

ISP Mode	ISPCN				ISPAH, ISPAL ISPA[15:0]	ISPFD[7:0]
	ISPA.17, ISPA.16	FOEN	FCEN	FCTRL[3:0]		
Standby	X, X[1]	1	1	X	X	X
APROM and Data Flash Page Erase	0, 0	1	0	0010	Address in[2]	X
LDROM Page Erase	0, 1	1	0	0010	Address in[2]	X
APROM and Data Flash Program	0, 0	1	0	0001	Address in	Data in
LDROM Program	0, 1	1	0	0001	Address in	Data in
APROM and Data Flash Read	0, 0	0	0	0000	Address in	Data out
LDROM Read	0, 1	0	0	0000	Address in	Data out
All CONFIG bytes Erase	1, 1	1	0	0010	00XXH	X
CONFIG Program	1, 1	1	0	0001	CONFIG0: 0000H CONFIG2: 0002H CONFIG3: 0003H	Data in
CONFIG Read	1, 1	0	0	0000	CONFIG0: 0000H CONFIG2: 0002H CONFIG3: 0003H	Data out

[1] "x" means "don't care".
[2] Each page is 256-byte size. Therefore, the address for Page Erase should be 0000H, 0100H, 0200H, 0300H, etc., which is incremented by one of high byte address.

18.3 User Guide of ISP

ISP facilitates the updating flash contents in a convenient way; however, the user should follow some restricted laws in order that the ISP operates correctly. Without noticing warnings will possible cause undetermined results even serious damages of devices. Be attention of these notices. Furthermore, this paragraph will also support useful suggestions during ISP procedures.

(1) If no more ISP operation needs, the user must clear ISPEN (CHPCON.0) to zero. It will make the system void to trigger ISP unaware. Furthermore, ISP requires internal 22.1184MHZ RC oscillator running. If the external clock source is chosen, disabling ISP will stop internal 22.1184MHz RC for saving power consumption. Note that a write to ISPEN is TA protected.

19. POWER SAVING MODES

N78E059A/N78E055A has several features that help the user to control the power consumption of the device. The power saved features have the Power Down mode and the Idle mode of operation. For a stable current consumption, states of P0 pins should be taken care of. P0 should be set as 0 if floating or external pull-downs exist. Or P0 should be set as 1 if external pull-ups exist or internal pull-ups are enabled by P0UP (P0OR.0).

In system power saving modes, the Watchdog Timer should be specially taken care. The hardware will clear WDT counter automatically after entering into or being woken-up from Idle or Power Down mode. It prevents unconscious system reset.

PCON – Power Control

7	6	5	4	3	2	1	0
SMOD	-	-	POF	GF1	GF0	PD	IDL
r/w	-	-	r/w	r/w	r/w	r/w	r/w

Address: 87H reset value: see Table 6–2. N78E059A/N78E055A SFR Descriptions and Reset Values

Bit	Name	Description
1	PD	**Power Down mode.** Setting this bit puts MCU into Power Down mode. Under this mode, both CPU and peripheral clocks stop and Program Counter (PC) suspends. It provides the lowest power consumption. After CPU is woken up from Power Down, this bit will be automatically cleared via hardware and the program continue executing the interrupt service routine (ISR) of the very interrupt source that woke the system up before. After return from the ISR, the device continues execution at the instruction which follows the instruction that put the system into Power Down mode. Note that If IDL bit and PD bit are set simultaneously, the MCU will enter into Power Down mode. Then it does not go to Idle mode after exiting Power Down.
0	IDL	**Idle mode.** Setting this bit puts MCU into Idle mode. Under this mode, the CPU clock stops and Program Counter (PC) suspends. After CPU is woken up from Idle, this bit will be automatically cleared via hardware and the program continue executing the ISR of the very interrupt source that woke the system up before. After return from the ISR, the device continues execution at the instruction which follows the instruction that put the system into Idle mode.

19.1 Idle Mode

Idle mode suspends CPU processing by holding the Program Counter. No program code are fetched and run in Idle mode. This forces the CPU state to be frozen. The Program Counter (PC), the Stack Pointer (SP), the Program Status Word (PSW), the Accumulator (ACC), and the other registers hold their contents during Idle mode. The port pins hold the logical states they had at the time Idle was activated. Generally, it saves considerable power of typical half of the full operating power.

nal. The reset circuitry then synchronously applies the internal reset signal. Thus the reset is a synchronous operation and requires the clock to be running to cause an external reset.

Once the device is in reset condition, it will remain so as long as RST pin is 1. After the RST high is removed, the CPU will exit the reset state with in two machine-cycles and begin code executing from address 0000H. There is no flag associated with the RST pin reset condition. However since the other reset sources have flags, the external reset can be considered as the default reset if those reset flags are cleared.

If a RST pin reset applies while CPU is in Power Down mode, the way to trigger a hardware reset is slightly different. Since the Power Down mode stops system clock, the reset signal will asynchronously cause the system clock resuming. After the system clock is stable, CPU will enter into the reset state.

22.4 Watchdog Timer Reset

The Watchdog Timer is a free running timer with programmable time-out intervals. The user can clear the Watchdog Timer at any time, causing it to restart the count. When the selected time-out occurs, the Watchdog Timer will reset the system directly. The reset condition is maintained via hardware for two machine-cycles. After the reset is removed, the device will begin execution from 0000H.

Once a reset due to Watchdog Timer occurs the Watchdog Timer reset flag WDTRF (WDCON.3) will be set. This bit keeps unchanged after any reset other than a power-on reset. The user may clear WDTRF via software.

22.5 Software Reset

N78E059A/N78E055A is enhanced with a software reset. This allows the program code to reset the whole system in software approach. It is quite useful in the end of an ISP progress. For example, if an LDROM updating APROM ISP finishes and the code in APROM is correctly updated, a software reset can be asserted to reboot CPU from the APROM in order to check the result of the updated APROM program code immediately. Writing 1 to SWRST (CHPCON.7) will trigger a software reset. Note that this bit is timed access protection. See demo code below. After a software reset the SWRF (RSR.0) will be automatically set via hardware. This bit will be preserved its value after all resets except power-on reset. SWRF can also be cleared via software.

is forced to 0000H and held as long as the reset condition is applied. Note that the Stack Pointer is also reset to 07H, therefore the stack contents may be effectively lost during the reset event even though the RAM contents are not altered.

After a reset, interrupts and Timers are disabled. The I/O port SFRs have FFH written into them which puts the port pins in a high state.

CONFIG3

7	6	5	4	3	2	1	0
CWDTEN	EN6T	ROG	CKF	INTOSCFS	-	FOSC	-
r/w	r/w	r/w	r/w	r/w	-	r/w	-

unprogrammed value: 1111 1111b

Bit	Name	Description
7	CWDTEN	**CONFIG Watchdog Timer enable.** 1 = Disable Watchdog Timer after all resets. 0 = Enable Watchdog Timer after all resets.
6	EN6T	**Enable 6T mode.** This bit switches MCU between 12T and 6T mode. See Figure 20–1. Clock System Block Diagram for definitions in details. 1 = MCU runs at 12T mode. Each machine-cycle is equal to 12 clocks of system oscillator. The operating mode is the same as a standard 8051 MCU. (F_{CPU} and F_{PERIPH} is a half of F_{OSC}.) 0 = MCU runs at 6T mode. Each machine-cycle is equal to 6 clocks of system oscillator. This mode doubles the whole chip operation compared with the standard 8051. (F_{CPU} and F_{PERIPH} is equal to F_{OSC}.)
5	ROG	**Reducing oscillator gain.** 1 = Use normal gain for crystal oscillating. The frequency can be up to 40MHz. 0 = Use reduced gain for crystal oscillating. The frequency should be lower than 24MHz. In reduced gain mode, it will also help to decrease EMI.
4	CKF	**Clock filter enable.** 1 = Enable clock filter. It increases noise immunity and EMC capacity. 0 = Disable clock filter. ***Note that the clock filter should be always disabled if the crystal frequency is above 24MHz.***
3	INTOSCFS	**Internal RC oscillator frequency select.** 1 = Select 22.1184MHz as the system clock if internal RC oscillator mode is used. It bypasses the divided-by-2 path of internal oscillator to select 22.1184MHz output as the system clock source. 0 = Select 11.0592MHz as the system clock if internal RC oscillator mode is used. The internal RC divided-by-2 path is selected. The internal oscillator is equivalent to 11.0592MHz output used as the system clock.
2	-	**Reserved.**
1	FOSC	**Oscillator selection bit.** This bit selects the source of the system clock. 1 = Crystal, resonator, or external clock input. 0 = Internal RC oscillator.
0	-	**Reserved.**

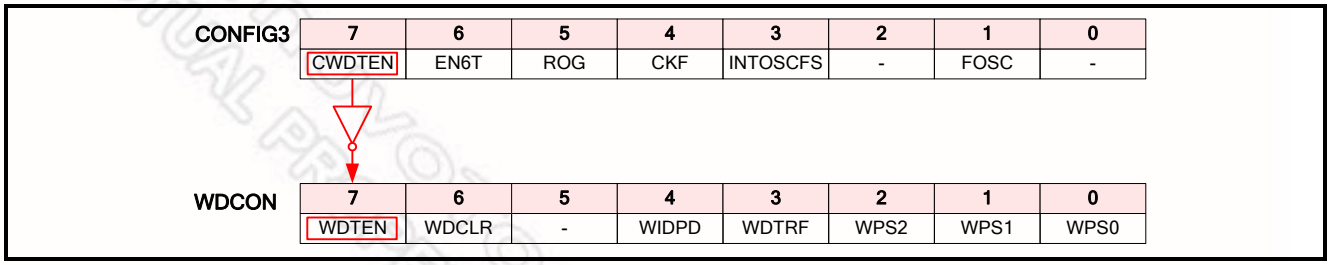

Figure 24–3. CONFIG3 Reset Reloading

25. INSTRUCTION SET

N78E059A/N78E055A executes all the instructions of the standard 8051 family. All instructions are coded within an 8-bit field called an OPCODE. This single byte must be fetched from Program Memory. The OPCODE is decoded by the CPU. It determines what action the microcontroller will take and whether more operation data is needed from memory. If no other data is needed, then only one byte was required. Thus the instruction is called a one byte instruction. In some cases, more data is needed. These will be two or three byte instructions.

Table 25–1 lists all instructions in details. Note of the instruction set and addressing modes are shown below.

Rn (n = 0~7)	Register R0~R7 of the currently selected Register Bank.
direct	8-bit internal data location's address. This could be an internal data RAM location (0~127) or a SFR (e.g., I/O port, control register, status register, etc. (128~255)).
@Ri (i = 0, 1)	8-bit internal data RAM location (0~255) addressed indirectly through register R0 or R1.
#data	8-bit constant included in the instruction.
#data16	16-bit constant included in the instruction.
addr16	16-bit destination address. Used by LCALL and LJMP. A branch can be anywhere within the 64k-byte Program Memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2k-byte page of Program Memory as the first byte of the following instruction.
rel	Signed (2's complement) 8-bit offset byte. Used by SJMP and all conditional branches. Range is -128 to +127 bytes relative to first byte of the following instruction.
bit	Direct addressed bit in internal data RAM or SFR.

Table 25–1. Instruction Set for N78E059A/N78E055A

Instruction	OPCODE	Bytes	Clock Cycles in 12T Mode	Clock Cycles in 6T Mode
NOP	00	1	12	6
ADD A, Rn	28~2F	1	12	6
ADD A, @Ri	26, 27	1	12	6
ADD A, direct	25	2	12	6
ADD A, #data	24	2	12	6
ADDC A, Rn	38~3F	1	12	6
ADDC A, @Ri	36, 37	1	12	6
ADDC A, direct	35	2	12	6
ADDC A, #data	34	2	12	6
SUBB A, Rn	98~9F	1	12	6
SUBB A, @Ri	96, 97	1	12	6
SUBB A, direct	95	2	12	6
SUBB A, #data	94	2	12	6

26. ELECTRICAL CHARACTERISTICS

26.1 Absolute Maximum Ratings

Parameter	Rating	Unit
Operating temperature under bias	-40 to +85	°C
Storage temperature range	-55 to +150	°C
Voltage on VDD pin to V_{SS}	-0.3 to +6.5	V
Voltage on any other pin to V_{SS}	-0.3 to (V_{DD}+0.3)	V

Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

26.2 DC Electrical Characteristics

Temperature = -40℃~85℃; V_{SS} = 0V;

V_{DD} = 4.5V to 5.5V @ F = 0 to 40MHz (12T mode), F = 0 to 33MHz (6T mode)

V_{DD} = 2.4V to 5.5V @ F = 0 to 27MHz (12T mode), F = 0 to 20MHz (6T mode)

V_{DD} = 3.0V to 5.5V for ISP erasing or programming.

Table 26–1. DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage				$0.2V_{DD}$ – 0.1	V
V_{IH}	Input high voltage (Ports 0 ~ 4, $\overline{EA}$)		$0.2V_{DD}$ + 0.9			V
V_{IH1}	Input high voltage (RST, XTAL1)		$0.7V_{DD}$			V
V_{OL}	Output low voltage[1]	V_{DD} = 4.5V, I_{OL} = 8.2mA V_{DD} = 3.0V, I_{OL} = 5.8mA V_{DD} = 2.4V, I_{OL} = 4.4mA			0.4	V
V_{OH}	Output high voltage (Ports 1 ~ 4 and Port 0 with internal pull-up enabled)	V_{DD} = 4.5V, I_{OH} = -300μA V_{DD} = 3.0V, I_{OH} = -75μA V_{DD} = 2.4V, I_{OH} = -35μA	2.4 2.4 2.0			V
V_{OH1}	Output high voltage (Ports 0 and 2 in external bus mode, ALE, $\overline{PSEN}$)	V_{DD} = 4.5V, I_{OH} = -9mA V_{DD} = 3.0V, I_{OH} = -2.4mA V_{DD} = 2.4V, I_{OH} = -1.3mA	2.4 2.4 2.0			V

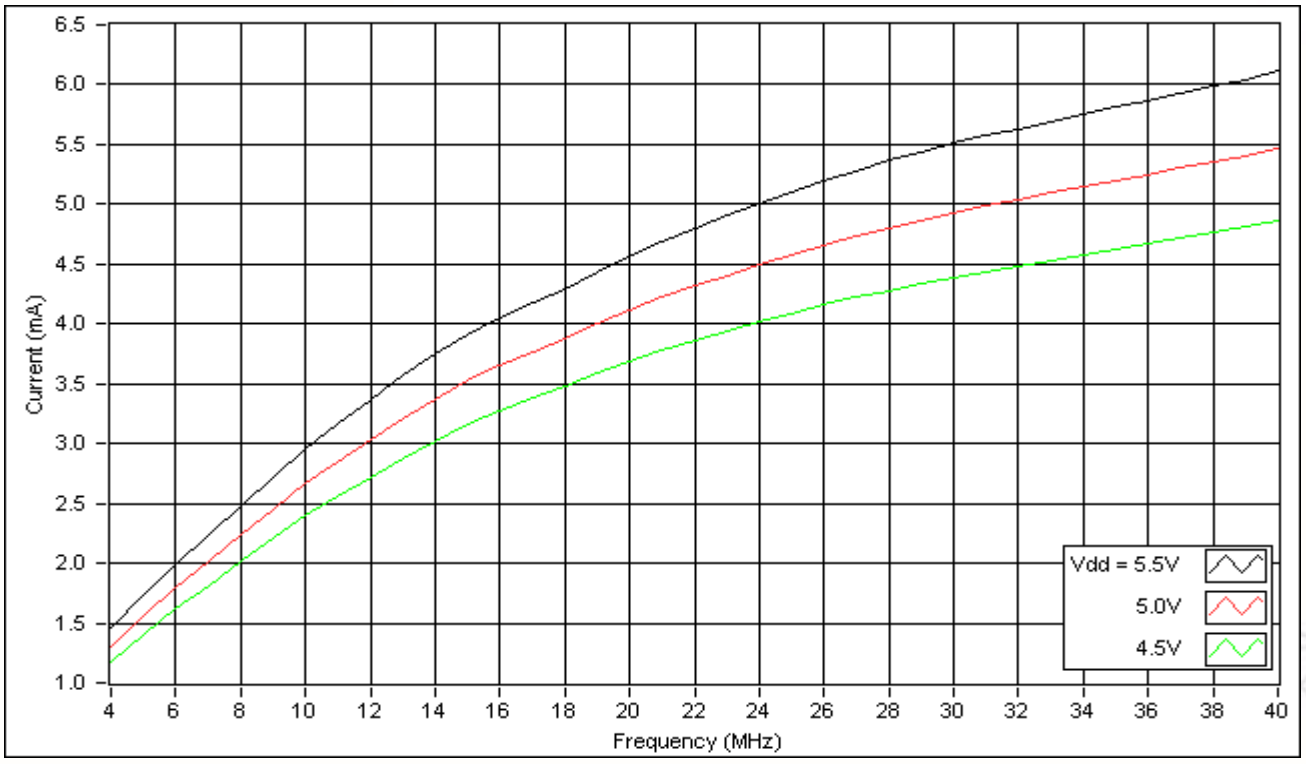

Figure 26–5. Idle Mode Current Under 12T Mode, External Clock (1)

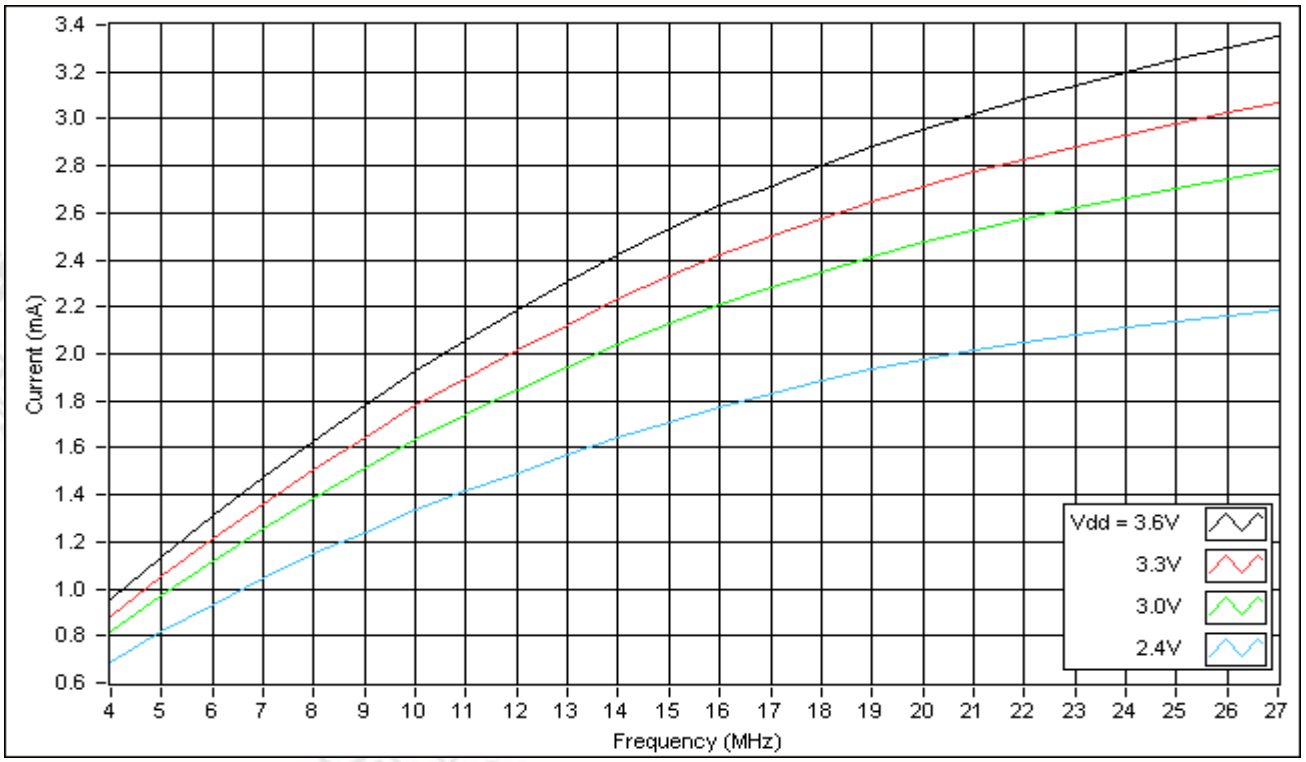

Figure 26–6. Idle Mode Current Under 12T Mode, External Clock (2)

26.3 AC Electrical Characteristics

Table 26–2. AC Characteristics

Symbol	Parameter	12T mode		6T mode		Unit
		Min.	Max.	Min.	Max.	
External Clock						
1/ t_{CLCL}	External clock input frequency	0	40	0	33	MHz
	Crystal/resonator frequency	4	40	4	33	
t_{CHCX}	High time	12		15		ns
t_{CLCX}	Low time	12		15		ns
t_{CLCH}	Rise time		8		5	ns
t_{CHCL}	Fall time		8		5	ns
Program Memory						
t_{LHLL}	ALE pulse width	2 t_{CLCL} -15		t_{CLCL} -15		ns
t_{AVLL}	Address valid to ALE low	t_{CLCL} -15		0.5 t_{CLCL} -15		ns
t_{LLAX}	Address hold after ALE low	t_{CLCL} -15		0.5 t_{CLCL} -15		ns
t_{LLIV}	ALE low to valid instruction in		4 t_{CLCL} -45		2 t_{CLCL} -45	ns
t_{LLPL}	ALE low to $\overline{PSEN}$ low	t_{CLCL} -15		0.5 t_{CLCL} -15		ns
t_{PLPH}	$\overline{PSEN}$ pulse width	3 t_{CLCL} -15		1.5 t_{CLCL} -15		ns
t_{PLIV}	$\overline{PSEN}$ low to valid instruction in		3 t_{CLCL} -50		1.5 t_{CLCL} -50	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input instruction float after $\overline{PSEN}$		t_{CLCL} -15		0.5 t_{CLCL} -15	ns
t_{AVIV}	Address to valid instruction in		5 t_{CLCL} -60		2.5 t_{CLCL} -60	ns
t_{PLAZ}	$\overline{PSEN}$ low to address float		10		10	ns
Data Memory						
t_{RLRH}	$\overline{RD}$ pulse width	6 t_{CLCL} -30		3 t_{CLCL} -30		ns
t_{WLWH}	$\overline{WR}$ pulse width	6 t_{CLCL} -30		3 t_{CLCL} -30		ns
t_{RLDV}	$\overline{RD}$ low to valid data in		5 t_{CLCL} -50		2.5 t_{CLCL} -50	ns
t_{RHDX}	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	Data float after $\overline{RD}$		2 t_{CLCL} -12		t_{CLCL} -12	ns
t_{LLDV}	ALE low to valid data in		8 t_{CLCL} -50		4 t_{CLCL} -50	ns
t_{AVDV}	Address to valid data in		9 t_{CLCL} -75		4.5 t_{CLCL} -75	ns
t_{LLWL}	ALE low to $\overline{RD}$ or $\overline{WR}$ low	3 t_{CLCL} -15	3 t_{CLCL} +15	1.5 t_{CLCL} -15	1.5 t_{CLCL} +15	ns