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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n78e059afg

Table 4–1. Pin Description

Pin number				Symbol	Alternate Function		Type[1]	Description
DIP	PLCC	PQFP	LQFP		1	2		
19	21	15	16	XTAL1			I (ST)	**CRYSTAL1:** This is the input pin to the internal inverting amplifier. The system clock is from external crystal or resonator when FOSC (CONFIG3.1) is logic 1 by default. ***A 0.1μF capacitor is recommended to be added on XTAL1 pin to gain the more precise frequency of the internal RC oscillator frequency if it is selected as the system clock source.***
18	20	14	15	XTAL2			O	**CRYSTAL2:** This is the output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1. While on-chip RC oscillator is used, float XTAL2 pin always.
40	44	38	41	VDD			P	**POWER SUPPLY:** Supply voltage V_{DD} for operation.
20	22	16	17	VSS			P	**GROUND:** Ground potential.
31	35	29	31	$\overline{EA}$			I	**EXTERNAL ACCESS ENABLE:** To force $\overline{EA}$ low will make the CPU execute the external Program Memory. The address and data will be presented on the bus P0 and P2. If the $\overline{EA}$ pin is high, CPU will fetch internal code unless the Program Counter addresses the area out of the internal Program Memory. This will make CPU run external Program Memory continuously. $\overline{EA}$ possesses reset lock. After all reset, the $\overline{EA}$ state will be latched and any state change of this pin after reset will not switch between internal and external Program Memory execution. ***The user should take care of this pin from floating but connecting to V_{DD} directly if internal Program Memory is used.***
30	33	27	29	ALE			O	**ADDRESS LATCH ENABLE:** ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6 of the Fosc[2]. An ALE pulse is omitted always. The user can turn ALE off by setting ALEOFF (AUXR.0) to reduce EMI. Setting ALEOFF will just make ALE activating only during external memory access through a MOVC or MOVX instruction. ALE will stay high in other conditions.
29	32	26	28	$\overline{PSEN}$			O	**PROGRAM STORE ENABLE:** $\overline{PSEN}$ strobes the external Program Memory. When internal Program Memory access is performed, there will be no $\overline{PSEN}$ strobe signal output from this pin.
9	10	4	4	RST			I (ST)	**RESET:** RST pin is a Schmitt trigger input pin for hardware device reset. A high on this pin for two machine-cycles while the system clock is running will reset the device. RST pin has an internal pull-down resistor allowing power-on reset by simply connecting

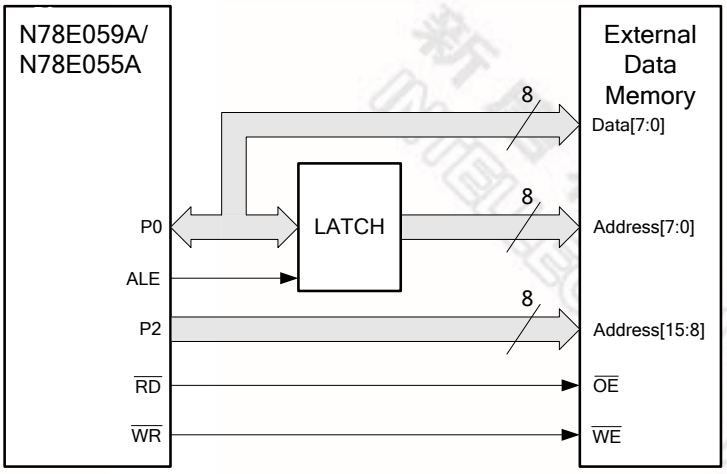

Figure 5–5. Data Memory Interface

5.6 On-chip Non-volatile Data Flash

N78E059A/N78E055A additionally has Data Flash. The Data Flash is non-volatile so that it remains its content even after the power is off. Therefore, in general application the user can write or read data which rules as parameters or constants. Be aware of Data Flash writing endurance of 10,000 cycles. By the software path, the Data Flash can be accessed only through ISP mode. Note that the erasing or writing of Data Flash should not operates under V_{DD} 3.0V for ISP limitation. For Data Flash accessing with ISP, please see Section 18. "IN SYSTEM PROGRAMMING (ISP)" on page 91 for details. For the design for security, ISP is invalid while external Program Memory executes. The Data Flash, therefore, cannot be accessed with external memory code. Of course the Data Flash can be accessed via hardware with parallel Programmer/Writer.

The Data Flash size is fixed as 4k-byte size on N78E059A/N78E055A.

Table 6–2. N78E059A/N78E055A SFR Descriptions and Reset Values

Symbol	Definition	Address	MSB							LSB[1]	Reset Value[2]
SPDR	SPI data	F5H									0000 0000b
SPSR	SPI status	F4H	SPIF	WCOL	SPIOVF	MODF	DISMODF	-	-	-	0000 0000b
SPCR	SPI control	F3H	SSOE	SPIEN	LSBFE	MSTR	CPOL	CPHA	SPR1	SPR0	0000 0000b
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	0000 0000b
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	0000 0000b
PWM3	PWM3 duty	DEH									0000 0000b
PWM2	PWM2 duty	DDH									0000 0000b
PWMCON0	PWM control 0	DCH	PWM3OE	PWM2OE	PWM3EN	PWM2EN	PWM1OE	PWM0OE	PWM1EN	PWM0EN	0000 0000b
PWM1	PWM1 duty	DBH									0000 0000b
PWM0	PWM0 duty	DAH									0000 0000b
PWMP	PWM period	D9H									0000 0000b
P4	Port 4	D8H	(DF)	(DE)	(DD)	(DC)	(DB) $\overline{\text{INT2}}$	(DA) $\overline{\text{INT3}}$	(D9)	(D8)	1111 1111b
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	0000 0000b
PWM4	PWM4 duty	CFH									0000 0000b
PWMCON1	PWM control 1	CEH	-	-	-	-	-	PWM4OE	-	PWM4EN	0000 0000b
TH2	Timer 2 high byte	CDH									0000 0000b
TL2	Timer 2 low byte	CCH									0000 0000b
RCAP2H	Timer 2 reload/capture high byte	CBH									0000 0000b
RCAP2L	Timer 2 reload/capture low byte	CAH									0000 0000b
T2MOD	Timer 2 mode	C9H	-	-	-	-	-	-	T2OE	-	0000 0000b
T2CON	Timer 2 control	C8H	(CF) TF2	(CE) EXF2	(CD) RCLK	(CC) TCLK	(CB) EXEN2	(CA) TR2	(C9) $\overline{\text{C/T2}}$	(C8) $\overline{\text{CP/RL2}}$	0000 0000b
TA	Timed access protection	C7H									0000 0000b
XICON	External interrupt control	C0H	(C7) PX3	(C6) EX3	(C4) IE3	(C4) IT3	(C3) PX2	(C2) EX2	(C1) IE2	(C0) 1IT2	0000 0000b
EIE	Extensive interrupt enable	BDH	-	-	-	-	-	EBOD	EPDT	ESPI	0000 0000b
EIP	Extensive interrupt priority	BCH	-	-	-	-	-	PBOV	PPDT	PSPI	0000 0000b
EIPH	Extensive interrupt priority high	BBH	-	-	-	-	-	PBODH	PPDTH	PSPIH	0000 0000b
IPH	Interrupt priority high	BAH	PX3H	PX2H	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	0000 0000b
IP	Interrupt priority	B8H	(BF) -	(BE) -	(BD) PT2	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	0000 0000b
P3	Port 3	B0H	(B7) $\overline{\text{RD}}$	(B6) $\overline{\text{WR}}$	(B5) T1	(B4) T0	(B3) $\overline{\text{INT1}}$	(B2) $\overline{\text{INT0}}$	(B1) TXD	(B0) RXD	1111 1111b
ISPCN	ISP flash control	AFH	ISPA17	ISPA16	FOEN	FCEN	FCTRL3	FCTRL2	FCTRL1	FCTRL0	0000 0000b
ISPFD	ISP flash data	AEH									0000 0000b
PMC[3]	Power monitoring control	ACH	BODEN	-	-	BORST	BOF[4]	LPBOD	-	BOS[5]	Power-on[6], XXXX X00Xb Brown-out, XXXX 100Xb Others, XXXX 000Xb
PDCON	Power Down waking-up timer control	ABH	PDTEN	PDTCK	PDTF	-	-	PPS2	PPS1	PPS0	0000 0000b
WDCON[3]	Watchdog Timer control	AAH	WDTEN	WDCLR	-	WIDPD	WDTRF	WPS2	WPS1	WPS0	Power-on[6], X000 0000b Watchdog, X00U 1UUUb Others, X00U UUUUb
IE	Interrupt enable	A8H	(AF) EA	(AE) -	(AD) ET2	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000b
ISPAH	ISP address high byte	A7H									0000 0000b
ISPAL	ISP address low byte	A6H									0000 0000b
ISPTRG[3]	ISP trigger	A4H	-	-	-	-	-	-	-	ISPGO	0000 0000b
XRAMAH	Auxiliary RAM address high byte	A1H	-	-	-	-	-	-	XRAMAH.1	XRAMAH.0	0000 0000b
P2	Port 2	A0H	(A7) A15	(A6) A14	(A5) A13	(A4) A12	(A3) A11	(A2) A10	(A1) A9	(A0) A8	1111 1111b

Table 6–2. N78E059A/N78E055A SFR Descriptions and Reset Values

Symbol	Definition	Address	MSB							LSB[1]	Reset Value[2]
CHPCON[3]	Chip control	9FH	SWRST	ISPF	LDUEN	XRAMEN	-	-	BS	ISPEN	Software[6], 0001 00U0b Others, 0001 00X0b
SBUF	Serial buffer	99H									0000 0000b
SCON	Serial control	98H	(9F) SM0	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000b
RSR	Reset status register	96H	-	-	-	-	-	BORF	-	SWRF	Power-on, 0000 0000b Brown-out, 0000 010Ub Software, 0000 0U01b Others, 0000 0U0Ub
P1	Port 1	90H	(97) PWM4 SPCLK	(96) PWM3 MISO	(95) PWM2 MOSI	(94) PWM1 $\overline{SS}$	(93) PWM0	(92)	(91) T2EX	(90) T2	1111 1111b
AUXR	Auxiliary register	8EH	-	-	-	-	-	-	-	ALEOFF	0000 0000b
TH1	Timer 1 high byte	8DH									0000 0000b
TH0	Timer 0 high byte	8CH									0000 0000b
TL1	Timer 1 low byte	8BH									0000 0000b
TL0	Timer 0 low byte	8AH									0000 0000b
TMOD	Timer 0 and 1 mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	0000 0000b
TCON	Timer 0 and 1control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0000 0000b
PCON	Power control	87H	SMOD	-	-	POF	GF1	GF0	PD	IDL	Power-on, 0001 0000b Others, 000U 0000b
P0OR	P0 option register	86H	-	-	-	-	-	-	-	P0UP	0000 0000b
DPH	Data pointer high byte	83H									0000 0000b
DPL	Data pointer low byte	82H									0000 0000b
SP	Stack pointer	81H									0000 0111b
P0	Port 0	80H	(87) A7	(86) A6	(85) A5	(84) A4	(83) A3	(82) A2	(81) A1	(80) A0	1111 1111b

[1] ( ) item means the bit address in bit-addressable SFRs.
[2] Reset value symbol description. 0: logic 0, 1: logic 1, U: unchanged, X: see **[4]** ~ **[7]**.
[3] These SFRs have TA protected writing.
[4] BOF has different power-on reset value according to CBODEN (CONFIG2.7) and CBORST (CONFIG2.4). See Table 21–1. BOF Reset Value.
[5] BOS is a read-only flag decided by V_{DD} level while Brown-out detection is enabled.
[6] These SFRs have bits which are initialized after specified reset by loading certain bits in CONFIG bytes. See Section 24. "CONFIG BYTES" on page 116 for details.

Note that bits marked in "-" must be kept in their own initial states. Users should never change their values.

P0UP (P0OR.0) P0 will switch on its weak pull-up internally and behave the same as the quasi bi-directional I/O pins.

P0 and P2 also serve as address/data bus when external memory is running or is accessed by MOVC or MOVX instruction. In these cases, it has strong pull-up and pull-down. In this application, there is no need of any external pull-up resistor. While external mode execution, P0 and P2 cannot be used as general purpose I/O anymore.

In standard 8051 instruction set, one kind of instructions, read-modify-write instructions, should be specially taken care of. Instead of the normal instructions, the read-modify-write instructions read the internal port latch (Px in SFRs) rather than the external port pin state. This kind of instructions read the port SFR value, modify it and write back to the port SFR. Read-modify-write instructions are listed as follows.

Instruction		Description
ANL		Logical AND. (ANL Px,A and ANL Px,direct)
ORL		Logical OR. (ORL Px,A and ORL Px,direct)
XRL		Logical exclusive OR. (XRL Px,A and XRL Px,direct)
JBC		Jump if bit = 1 and clear it. (JBC Px.y,LABEL)
CPL		Complement bit. (CPL Px.y)
INC		Increment. (INC Px)
DEC		Decrement. (DEC Px)
DJNZ		Decrement and jump if not zero. (DJNZ Px,LABEL)
MOV	Px.y,C	Move carry bit to Px.y.
CLR	Px.y	Clear bit Px.y.
SETB	Px.y	Set bit Px.y.

The last three seems not obviously read-modify-write instructions but actually they are. They read the entire port latch value, modify the changed bit, then write the new value back to the port latch.

10. TIMERS/COUNTERS

N78E059A/N78E055A has three 16-bit programmable timers/counters.

10.1 Timer/Counters 0 and 1

Timer/Counter 0 and 1 on N78E059A/N78E055A are two 16-bit Timer/Counters. Each of them has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. TCON and TMOD can configure modes of Timer/Counter 0 and 1.

The Timer or Counter function is selected by the C/$\overline{T}$ bit in TMOD. Each Timer/Counter has its own selection bit. TMOD.2 selects the function for Timer/Counter 0 and TMOD.6 selects the function for Timer/Counter 1

When configured as a “Timer”, the timer counts clock cycles. The timer clock is 1/6 of the peripheral clock (F_{PERIPH}). In the “Counter” mode, the register increases on the falling edge of the external input pins T0 for Timer 0 and T1 for Timer 1. If the sampled value is high in one machine-cycle and low in the next, a valid 1 to 0 transition on the pin is recognized and the count register increases.

In addition, each Timer/Counter can be set to operate in any one of four possible modes. Bits M0 and M1 in TMOD do the mode selection.

TMOD – Timer 0 and 1 Mode

7	6	5	4	3	2	1	0
GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: 89H reset value: 0000 0000b

Bit	Name	Description
7	GATE	**Timer 1 gate control.** 0 = Timer 1 will clock when TR1 = 1 regardless of $\overline{INT1}$ logic level. 1 = Timer 1 will clock only when TR1 = 1 and $\overline{INT1}$ is logic 1.
6	C/$\overline{T}$	**Timer 1 Counter/Timer select.** 0 = Timer 1 is incremented by internal peripheral clocks. 1 = Timer 1 is incremented by the falling edge of the external pin T1.
5	M1	**Timer 1 mode select.**
4	M0	M1 M0 Timer 1 Mode 0 0 Mode 0: 8-bit Timer/Counter with 5-bit pre-scalar (TL1[4:0]) 0 1 Mode 1: 16-bit Timer/Counter 1 0 Mode 2: 8-bit Timer/Counter with auto-reload from TH1 1 1 Mode 3: Timer 1 halted

TH0 – Timer 0 High Byte

7	6	5	4	3	2	1	0
TH0[7:0]							
r/w							

Address: 8CH reset value: 0000 0000b

Bit	Name	Description
7:0	TH0[7:0]	**Timer 0 high byte.** The TH0 register is the high byte of the 16-bit Timer 0.

TL1 – Timer 1 Low Byte

7	6	5	4	3	2	1	0
TL1[7:0]							
r/w							

Address: 8BH reset value: 0000 0000b

Bit	Name	Description
7:0	TL1[7:0]	**Timer 1 low byte.** The TL1 register is the low byte of the 16-bit Timer 1.

TH1 – Timer 1 High Byte

7	6	5	4	3	2	1	0
TH1[7:0]							
r/w							

Address: 8DH reset value: 0000 0000b

Bit	Name	Description
7:0	TH1[7:0]	**Timer 1 high byte.** The TH1 register is the high byte of the 16-bit Timer 1.

10.1.1 Mode 0 (13-bit Timer)

In Mode 0, the Timer/Counter is a 13-bit counter. The 13-bit counter consists of THx and the five lower bits of TLx. The upper three bits of TLx are ignored. The Timer/Counter is enabled when TRx is set and either GATE is 0 or $\overline{INTx}$ is 1. Gate = 1 allows the Timer to calculate the pulse width on external input pin $\overline{INTx}$. When the 13-bit value moves from 1FFFH to 0000H, the Timer overflow flag TFx is set and an interrupt occurs if enabled. Note that the peripheral clock is $F_{OSC}/2$ in 12T mode and is F_{OSC} in 6T mode. See Section 20. "CLOCK SYSTEM" on page 102.

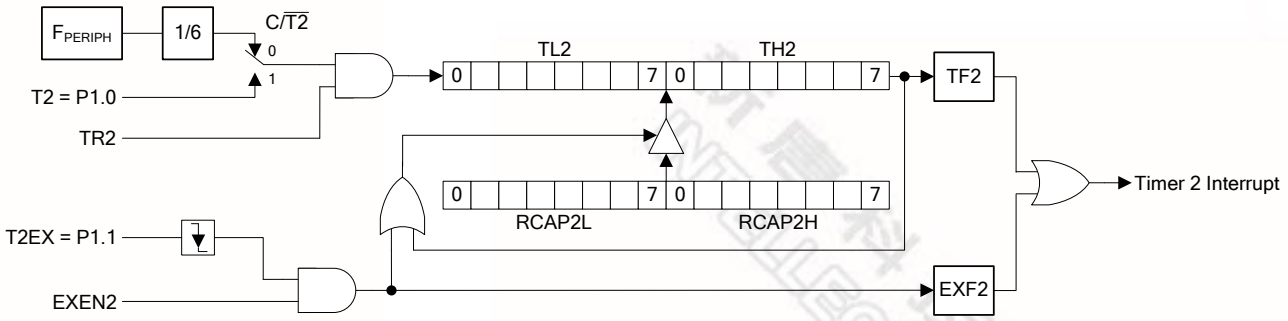

Figure 10–6. Timer/Counter 2 in Auto-reload Mode

10.2.3 Baud Rate Generator Mode

The Timer 2 can generate the baud rate for UART in its Mode 1 and 3. The baud rate generator mode is enabled by setting either the RCLK or TCLK bits in T2CON register. While in the baud rate generator mode, Timer/Counter 2 is a 16 bit counter with auto-reload when the count rolls over from FFFFH. However, rolling over is used to generate the shift clock for UART data rather than to set the TF2 bit. If EXEN2 bit is set, then a negative transition of the T2EX pin will set EXF2 bit in the T2CON register and cause an interrupt request. It simply provides a external interrupt. Note that TCLK and RCLK are selected individually, the serial port transmit rate can be different from the receive rate. For example the transmit clock can be generated from Timer 2 by setting TCLK and the receive clock from Timer 1 by clearing RCLK.

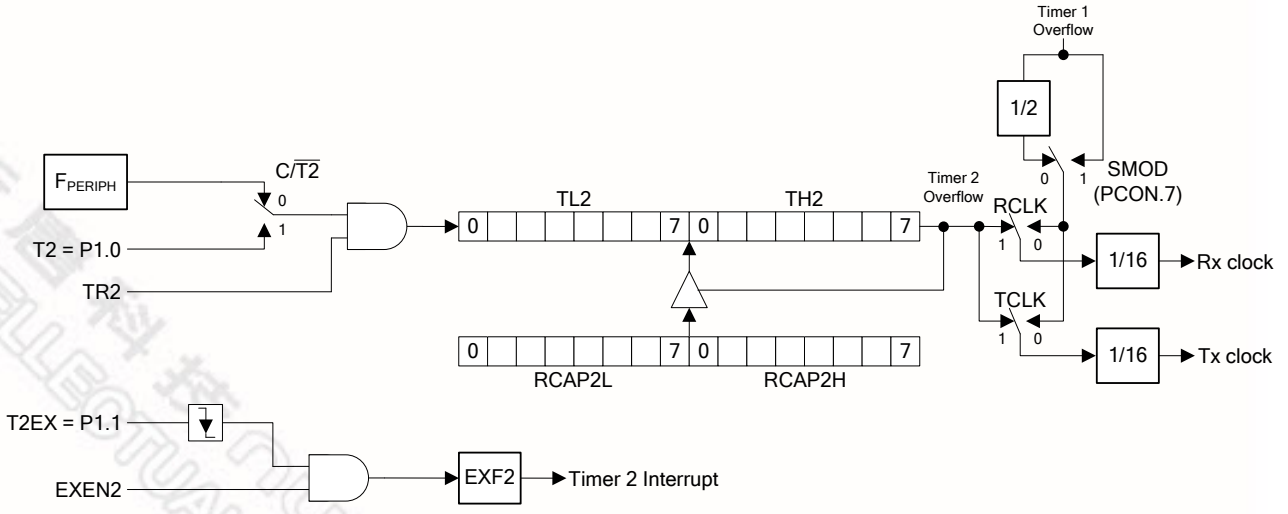

Figure 10–7. Timer/Counter 2 in Baud Rate Generator Mode

Bit	Name	Description
5	PDTF	**Power Down waking-up timer Interrupt Flag.** This bit will be set via hardware when PDT counter overflows. This bit must be cleared via software.
4:3	-	**Reserved.**
2	PPS2	**Power Down waking-up timer clock pre-scalar select.** These bits determine the scale of the clock divider for PDT counter. The scale is from 1/1 through 1/1024. See Table 12–1.
1	PPS1	
0	PPS0	

The Power Down waking-up time-out interval is determined by the formula $\frac{1}{F_{LOSC} \times clockdividerscalar} \times 64$ where F_{ILRC} is the frequency of internal 10kHz RC. The following table shows an example of the Power Down waking-up time-out interval under different pre-scalars.

Table 12–1. Power Down Waking-up Timer-Out Interval under different pre-scalars

PPS2	PPS1	PPS0	Clock Divider Scale	Typical Power Down Waking-up Time-out Interval (F_{ILRC} ~= 10kHz)
0	0	0	1/1	6.40ms
0	0	1	1/4	25.60ms
0	1	0	1/8	51.20ms
0	1	1	1/32	204.80ms
1	0	0	1/64	409.60ms
1	0	1	1/256	1.638s
1	1	0	1/512	3.277s
1	1	1	1/1024	6.554s

12.2 Applications of Power Down Waking-up Timer

The main application of the Power Down waking-up timer is a simple timer. The PDTF flag will be set while the Power Down waking-up timer completes the selected time interval. The software polls the PDTF flag to detect a time-out and the PDCLR allows software to restart the timer. The Power Down waking-up timer can also be used as a very long timer. Every time the time-out occurs, an interrupt will occur if the individual interrupt EPDT (EIE.1) and global interrupt enable EA is set.

In some application of low power consumption, the CPU usually stays in Idle mode when nothing needs to be served to save power consumption. After a while the CPU will be woken up to check if anything needs to be served at an interval of programmed period implemented by Timer 0, 1 or 2. However, the current consumption

Bit	Name	Description
0	PWM0EN	**PWM0 enable.** 0 = PWM0 is disabled and stops. 1 = PWM0 is enabled and runs.

PWMCON1 – PWM Control 1

7	6	5	4	3	2	1	0
-	-	-	-	-	PWM4OE	-	PWM4EN
-	-	-	-	-	r/w	-	r/w

Address: CEH reset value: 0000 0000b

Bit	Name	Description
7:3	-	**Reserved.**
2	PWM4OE	**PWM4 output enable.** 0 = P1.7 serves as general purpose I/O. 1 = P1.7 serves as output pin of PWM4 signal.
1	-	**Reserved.**
0	PWM4EN	**PWM0 enable.** 0 = PWM4 is disabled and stops. 1 = PWM4 is enabled and runs.

PWMP – PWM Period

7	6	5	4	3	2	1	0
PWMP[7:0]							
r/w							

Address: D9H reset value: 0000 0000b

Bit	Name	Description
7:0	PWMP[7:0]	**PWM period.** This byte controls the period of the PWM output of PWM0~PWM4 channels.

PWM0 – PWM0 Duty

7	6	5	4	3	2	1	0
PWM0[7:0]							
r/w							

Address: DAH reset value: 0000 0000b

Bit	Name	Description
7:0	PWM0[7:0]	**PWM0 duty.** This byte controls the duty of the PWM0 output.

CHPCON – Chip Control (TA protected)

7	6	5	4	3	2	1	0
SWRST	ISPF	LDUEN	XRAMEN	-	-	BS	ISPEN
w	r/w	r/w	r/w	-	-	r/w	r/w

Address: 9FH reset value: see Table 6–2. N78E059A/N78E055A SFR Descriptions and Reset Values

Bit	Name	Description
6	ISPF	**ISP fault flag.** The hardware will set this bit when any of the following condition is met: 1. The accessing area is illegal, such as, (a) Erasing or programming APROM itself when APROM code runs. (b) Erasing or programming LDROM when APROM code runs but LDUEN is 0. (c) Erasing, programming, or reading CONFIG bytes when APROM code runs. (d) Erasing or programming LDROM itself when LDROM code runs. (e) Accessing oversize. 2. The ISP operating runs from internal Program Memory into external one. This bit should be cleared via software.
5	LDUEN	**Updating LDROM enable.** 0 = The LDROM is inhibited to be erased or programmed when APROM code runs. LDROM remains read-only. 1 = The LDROM is allowed to be fully accessed when APROM code runs.
0	ISPEN	**ISP enable.** 0 = Enable ISP function. 1 = Disable ISP function. To enable ISP function will start the internal 22.1184MHz RC oscillator for timing control. To clear ISPEN should always be the last instruction after ISP operation in order to stop internal RC for reducing power consumption.

ISPCN – ISP Control

7	6	5	4	3	2	1	0
ISPA.17	ISPA.16	FOEN	FCEN	FCTRL.3	FCTRL.2	FCTRL.1	FCTRL.0
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: AFH reset value: 0000 0000b

Bit	Name	Description
7:6	ISPA[17:16]	**ISP control.** This byte is for ISP controlling command to decide ISP destinations and actions. For details, see Table 18–1. ISP Modes and Command Codes.
5	FOEN	
4	FCEN	
3:0	FCTRL[3:0]	

CONFIG2

7	6	5	4	3	2	1	0
CBODEN	CBOV1	CBOV0	CBORST	-	-	-	-
r/w	r/w	r/w	r/w	-	-	-	-

unprogrammed value: 1111 1111b

Bit	Name	Description
7	CBODEN	**CONFIG Brown-out detect enable.** 1 = Enable Brown-out detection. 0 = Disable Brown-out detection.
6 5	CBOV1 CBOV0	**CONFIG Brown-out voltage select.** These two bits select one of four Brown-out voltage level. CBOV1 CBOV0 Brown-out Voltage 1 1 2.2V 1 0 2.7V 0 1 3.8V 0 0 4.5V
4	CBORST	**CONFIG Brown-out reset enable.** This bit decides if a Brown-out reset is caused after a Brown-out event. 1 = Enable Brown-out reset when V_{DD} drops below V_{BOD}. 0 = Disable Brown-out reset when V_{DD} drops below V_{BOD}.

PMC – Power Monitoring Control (TA protected)

7	6	5	4	3	2	1	0
BODEN[1]	-	-	BORST[1]	BOF	LPBOD	-	BOS
r/w	-	-	r/w	r/w	r/w	-	r

Address: ACH reset value: see Table 6–2. N78E059A/N78E055A SFR Descriptions and Reset Values

Bit	Name	Description
7	BODEN	**Brown-out detect enable.** 0 = Disable Brown-out detection. 1 = Enable Brown-out detection.
6:5	-	**Reserved.**
4	BORST	**Brown-out reset enable.** This bit decides if a Brown-out reset is caused after a Brown-out event. 0 = Disable Brown-out reset when V_{DD} drops below V_{BOD}. 1 = Enable Brown-out reset when V_{DD} drops below V_{BOD}.
3	BOF	**Brown-out flag.** This flag will be set as a logic 1 via hardware after a V_{DD} dropping below or rising above V_{BOD} event occurs. If both EBOD (EIE.2) and EA (IE.7) are set, a Brown-out interrupt requirement will be generated. This bit must be cleared via software.
3	LPBOD	**Low power Brown-out detection enable.** This bit switches the Brown-out detection into a power saving mode. This bit is only effective while BODEN = 1. 0 = Disable Brown-out power saving mode. Brown-out detection operates in normal mode if enabled. The detection is always on. 1 = Enable Brown-out power saving mode. Brown-out detection operates in power saving mode if enabled. Enable this bit will switch on internal 10kHz RC to be a timer for about 12.8ms interval of detection. The discrete detection will save much power but the hysteresis feature disappears.

CONFIG0

7	6	5	4	3	2	1	0
CBS	-	-	-	-	MOVCL	LOCK	-
r/w	-	-	-	-	r/w	r/w	-

unprogrammed value: 1111 1111b

Bit	Name	Description
7	CBS	**CONFIG boot select.** This bit defines from which block MCU boots after all resets except software reset. 1 = MCU will boot from APROM after all resets except software reset. 0 = MCU will boot from LDROM after all resets except software reset.

CHPCON – Chip Control (TA protected)

7	6	5	4	3	2	1	0
SWRST	ISPF	LDUEN	XRAMEN	-	-	BS[1]	ISPEN
w	r/w	r/w	r/w	-	-	r/w	r/w

Address: 9FH reset value: see Table 6–2. N78E059A/N78E055A SFR Descriptions and Reset Values

Bit	Name	Description
1	BS	**Boot select.** There are different meanings of writing to or reading from this bit. Writing: It defines from which block MCU boots after all resets. 0 = The next rebooting will be from APROM. 1 = The next rebooting will be from LDROM. Reading: It indicates from which block MCU booted after previous reset. 0 = The previous rebooting is from APROM. 1 = The previous rebooting is from LDROM.

[1] Note that this bit is initialized by being loaded from the inverted value of CBS bit in CONFIG0.7 at all resets except software reset. It keeps unchanged after software reset.

Note that after the CPU is released from all reset state, the hardware will always check the BS bit instead of the CBS bit to determine from APROM or LDROM that the device reboots.

22.7 Reset State

The reset state does not affect the on-chip RAM. The data in the RAM will be preserved during the reset. Note that the RAM contents may be lost if the V_{DD} falls below approximately 1.2V. This is the minimum voltage level required for RAM data retention. Therefore, after the power-on reset the RAM contents will be indeterminate. During a power fail condition. If the power falls below the data retention minimum voltage, the RAM contents will also lose.

After a reset, most of SFRs go to their initial values except bits which are affected by different reset events. See the notes of Table 6–2. N78E059A/N78E055A SFR Descriptions and Reset Values. The Program Counter

is forced to 0000H and held as long as the reset condition is applied. Note that the Stack Pointer is also reset to 07H, therefore the stack contents may be effectively lost during the reset event even though the RAM contents are not altered.

After a reset, interrupts and Timers are disabled. The I/O port SFRs have FFH written into them which puts the port pins in a high state.

CONFIG3

7	6	5	4	3	2	1	0
CWDTEN	EN6T	ROG	CKF	INTOSCFS	-	FOSC	-
r/w	r/w	r/w	r/w	r/w	-	r/w	-

unprogrammed value: 1111 1111b

Bit	Name	Description
7	CWDTEN	**CONFIG Watchdog Timer enable.** 1 = Disable Watchdog Timer after all resets. 0 = Enable Watchdog Timer after all resets.
6	EN6T	**Enable 6T mode.** This bit switches MCU between 12T and 6T mode. See Figure 20–1. Clock System Block Diagram for definitions in details. 1 = MCU runs at 12T mode. Each machine-cycle is equal to 12 clocks of system oscillator. The operating mode is the same as a standard 8051 MCU. (F_{CPU} and F_{PERIPH} is a half of F_{OSC}.) 0 = MCU runs at 6T mode. Each machine-cycle is equal to 6 clocks of system oscillator. This mode doubles the whole chip operation compared with the standard 8051. (F_{CPU} and F_{PERIPH} is equal to F_{OSC}.)
5	ROG	**Reducing oscillator gain.** 1 = Use normal gain for crystal oscillating. The frequency can be up to 40MHz. 0 = Use reduced gain for crystal oscillating. The frequency should be lower than 24MHz. In reduced gain mode, it will also help to decrease EMI.
4	CKF	**Clock filter enable.** 1 = Enable clock filter. It increases noise immunity and EMC capacity. 0 = Disable clock filter. ***Note that the clock filter should be always disabled if the crystal frequency is above 24MHz.***
3	INTOSCFS	**Internal RC oscillator frequency select.** 1 = Select 22.1184MHz as the system clock if internal RC oscillator mode is used. It bypasses the divided-by-2 path of internal oscillator to select 22.1184MHz output as the system clock source. 0 = Select 11.0592MHz as the system clock if internal RC oscillator mode is used. The internal RC divided-by-2 path is selected. The internal oscillator is equivalent to 11.0592MHz output used as the system clock.
2	-	**Reserved.**
1	FOSC	**Oscillator selection bit.** This bit selects the source of the system clock. 1 = Crystal, resonator, or external clock input. 0 = Internal RC oscillator.
0	-	**Reserved.**

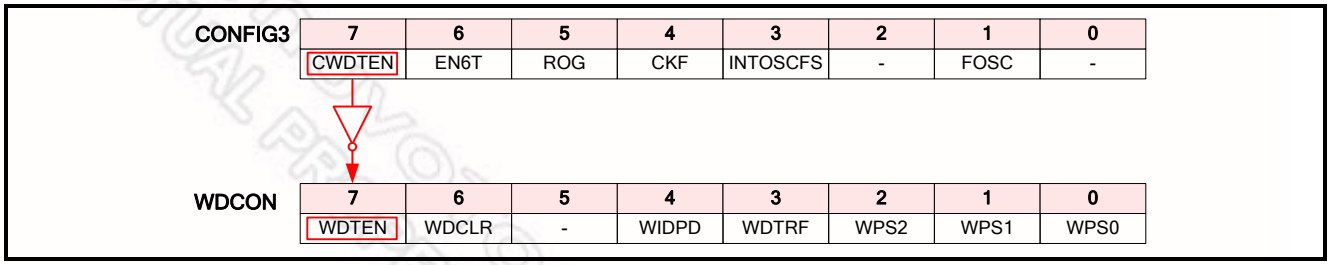

Figure 24–3. CONFIG3 Reset Reloading

Table 25–1. Instruction Set for N78E059A/N78E055A

Instruction		OPCODE	Bytes	Clock Cycles in 12T Mode	Clock Cycles in 6T Mode
INC	A	04	1	12	6
INC	Rn	08~0F	1	12	6
INC	@Ri	06, 07	1	12	6
INC	direct	05	2	12	6
INC	DPTR	A3	1	24	12
DEC	A	14	1	12	6
DEC	Rn	18~1F	1	12	6
DEC	@Ri	16, 17	1	12	6
DEC	direct	15	2	12	6
MUL	AB	A4	1	48	24
DIV	AB	84	1	48	24
DA	A	D4	1	12	6
ANL	A, Rn	58~5F	1	12	6
ANL	A, @Ri	56, 57	1	12	6
ANL	A, direct	55	2	12	6
ANL	A, #data	54	2	12	6
ANL	direct, A	52	2	12	6
ANL	direct, #data	53	3	24	12
ORL	A, Rn	48~4F	1	12	6
ORL	A, @Ri	46, 47	1	12	6
ORL	A, direct	45	2	12	6
ORL	A, #data	44	2	12	6
ORL	direct, A	42	2	12	6
ORL	direct, #data	43	3	24	12
XRL	A, Rn	68~6F	1	12	6
XRL	A, @Ri	66, 67	1	12	6
XRL	A, direct	65	2	12	6
XRL	A, #data	64	2	12	6
XRL	direct, A	62	2	12	6
XRL	direct, #data	63	3	24	12
CLR	A	E4	1	12	6
CPL	A	F4	1	12	6
RL	A	23	1	12	6
RLC	A	33	1	12	6
RR	A	03	1	12	6
RRC	A	13	1	12	6
SWAP	A	C4	1	12	6
MOV	A, Rn	E8~EF	1	12	6
MOV	A, @Ri	E6, E7	1	12	6
MOV	A, direct	E5	2	12	6

Figures below shows supply and Idle mode current under 12T/6T with internal program memory mode.

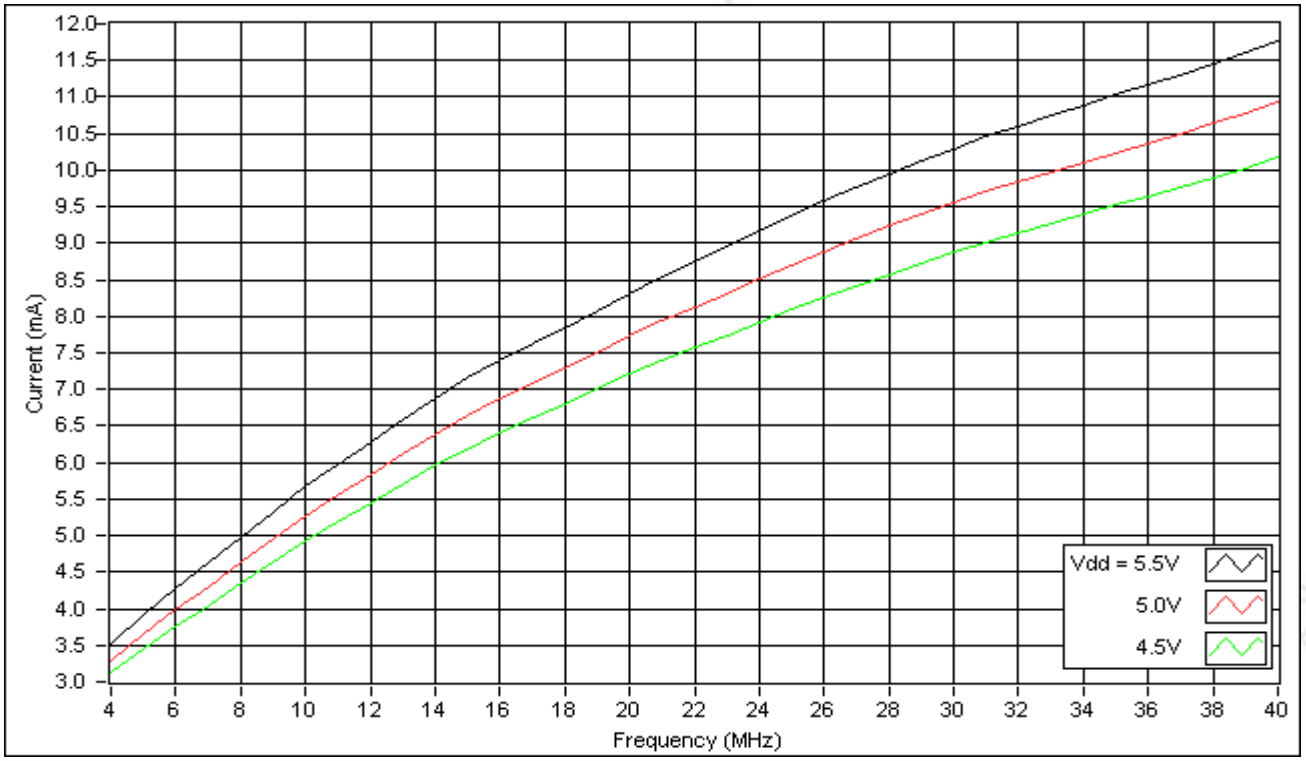

Figure 26–1. Supply Current Under 12T Mode, External Clock (1)

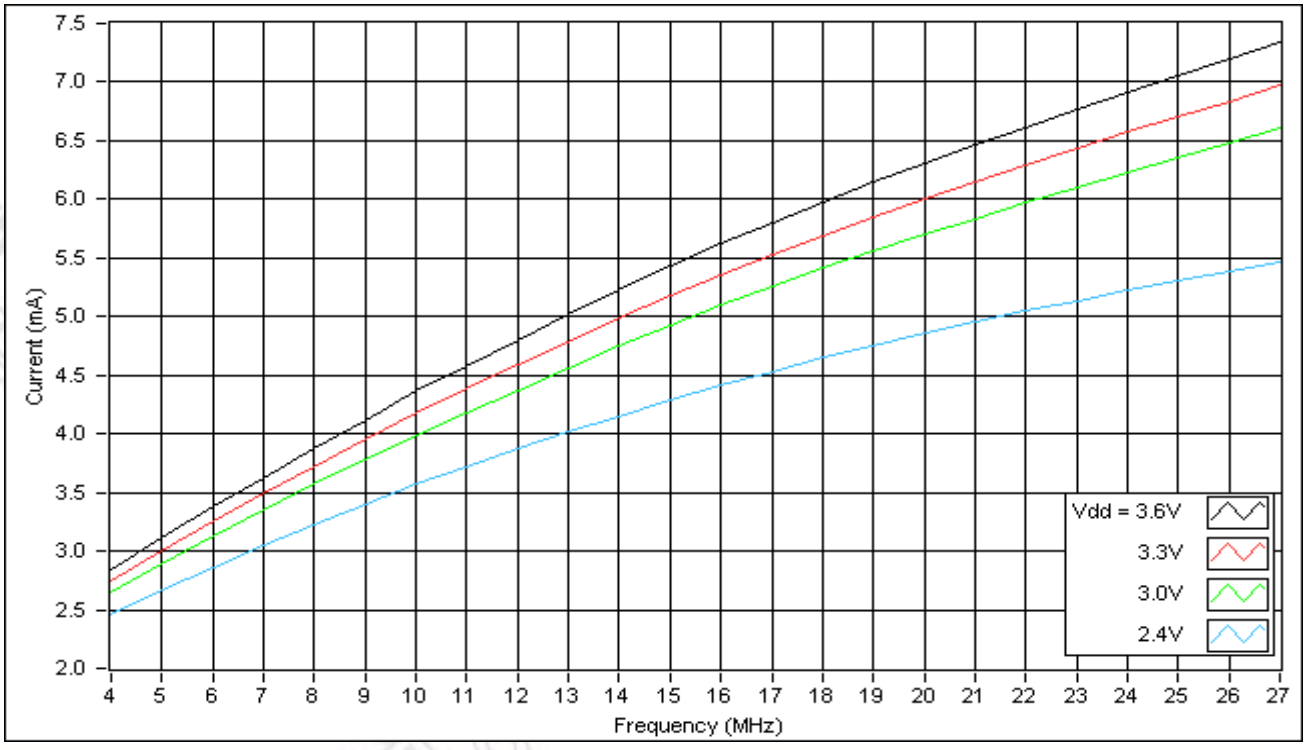

Figure 26–2. Supply Current Under 12T Mode, External Clock (2)

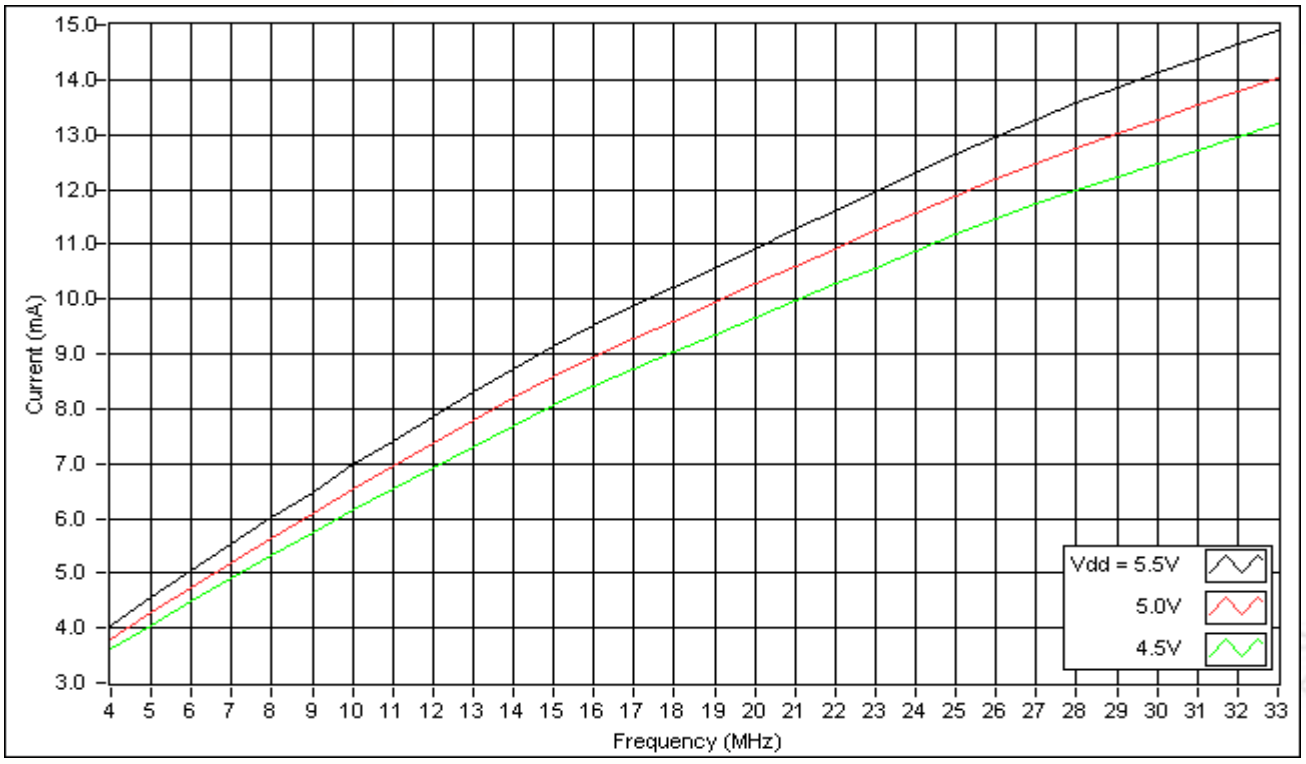

Figure 26–3. Supply Current Under 6T Mode, External Clock (1)

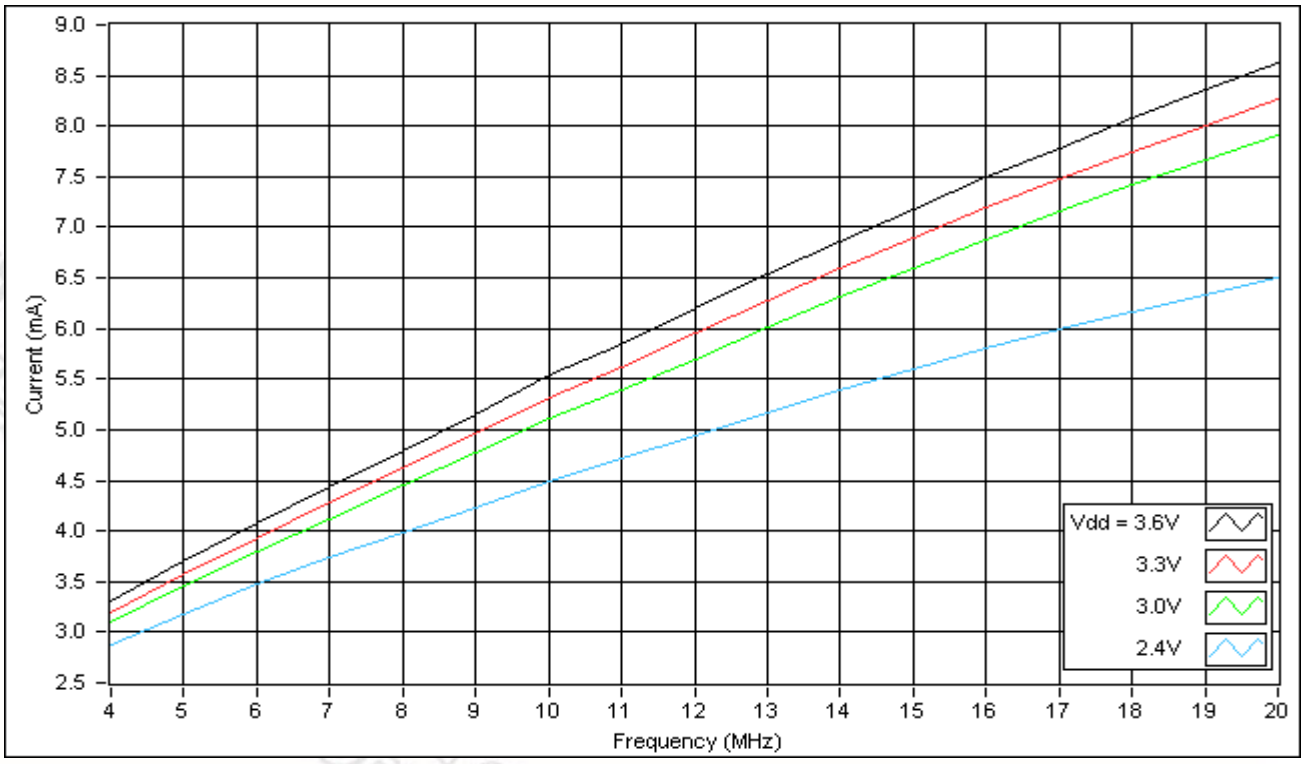

Figure 26–4. Supply Current Under 6T Mode, External Clock (2)

26.3 AC Electrical Characteristics

Table 26–2. AC Characteristics

Symbol	Parameter	12T mode		6T mode		Unit
		Min.	Max.	Min.	Max.	
External Clock						
1/ t_{CLCL}	External clock input frequency	0	40	0	33	MHz
	Crystal/resonator frequency	4	40	4	33	
t_{CHCX}	High time	12		15		ns
t_{CLCX}	Low time	12		15		ns
t_{CLCH}	Rise time		8		5	ns
t_{CHCL}	Fall time		8		5	ns
Program Memory						
t_{LHLL}	ALE pulse width	2 t_{CLCL} -15		t_{CLCL} -15		ns
t_{AVLL}	Address valid to ALE low	t_{CLCL} -15		0.5 t_{CLCL} -15		ns
t_{LLAX}	Address hold after ALE low	t_{CLCL} -15		0.5 t_{CLCL} -15		ns
t_{LLIV}	ALE low to valid instruction in		4 t_{CLCL} -45		2 t_{CLCL} -45	ns
t_{LLPL}	ALE low to $\overline{PSEN}$ low	t_{CLCL} -15		0.5 t_{CLCL} -15		ns
t_{PLPH}	$\overline{PSEN}$ pulse width	3 t_{CLCL} -15		1.5 t_{CLCL} -15		ns
t_{PLIV}	$\overline{PSEN}$ low to valid instruction in		3 t_{CLCL} -50		1.5 t_{CLCL} -50	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input instruction float after $\overline{PSEN}$		t_{CLCL} -15		0.5 t_{CLCL} -15	ns
t_{AVIV}	Address to valid instruction in		5 t_{CLCL} -60		2.5 t_{CLCL} -60	ns
t_{PLAZ}	$\overline{PSEN}$ low to address float		10		10	ns
Data Memory						
t_{RLRH}	$\overline{RD}$ pulse width	6 t_{CLCL} -30		3 t_{CLCL} -30		ns
t_{WLWH}	$\overline{WR}$ pulse width	6 t_{CLCL} -30		3 t_{CLCL} -30		ns
t_{RLDV}	$\overline{RD}$ low to valid data in		5 t_{CLCL} -50		2.5 t_{CLCL} -50	ns
t_{RHDX}	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	Data float after $\overline{RD}$		2 t_{CLCL} -12		t_{CLCL} -12	ns
t_{LLDV}	ALE low to valid data in		8 t_{CLCL} -50		4 t_{CLCL} -50	ns
t_{AVDV}	Address to valid data in		9 t_{CLCL} -75		4.5 t_{CLCL} -75	ns
t_{LLWL}	ALE low to $\overline{RD}$ or $\overline{WR}$ low	3 t_{CLCL} -15	3 t_{CLCL} +15	1.5 t_{CLCL} -15	1.5 t_{CLCL} +15	ns