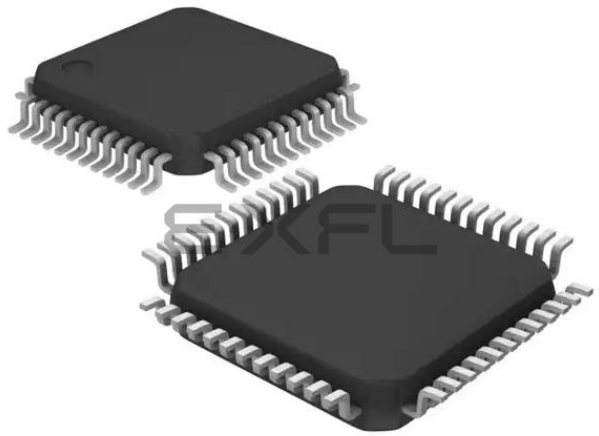
Nuvoton Technology Corporation - N78E059ALG Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n78e059alg

3. BLOCK DIAGRAM

Figure 3–1 shows the functional block diagram of N78E059A/N78E055A. It gives the outline of the device. The user can find all the device's peripheral functions in the diagram.

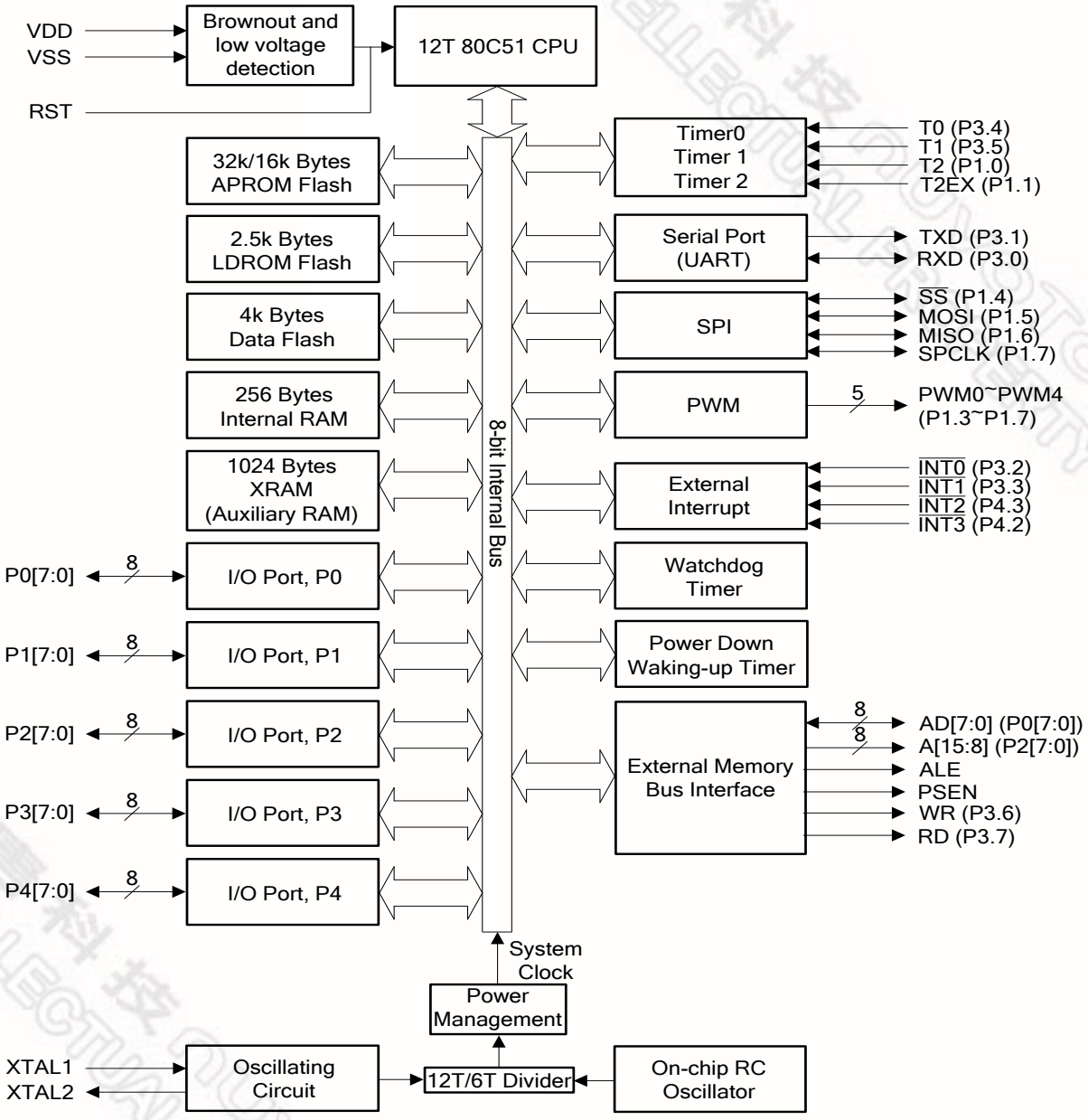

Figure 3–1. N78E059A/N78E055A Function Block Diagram

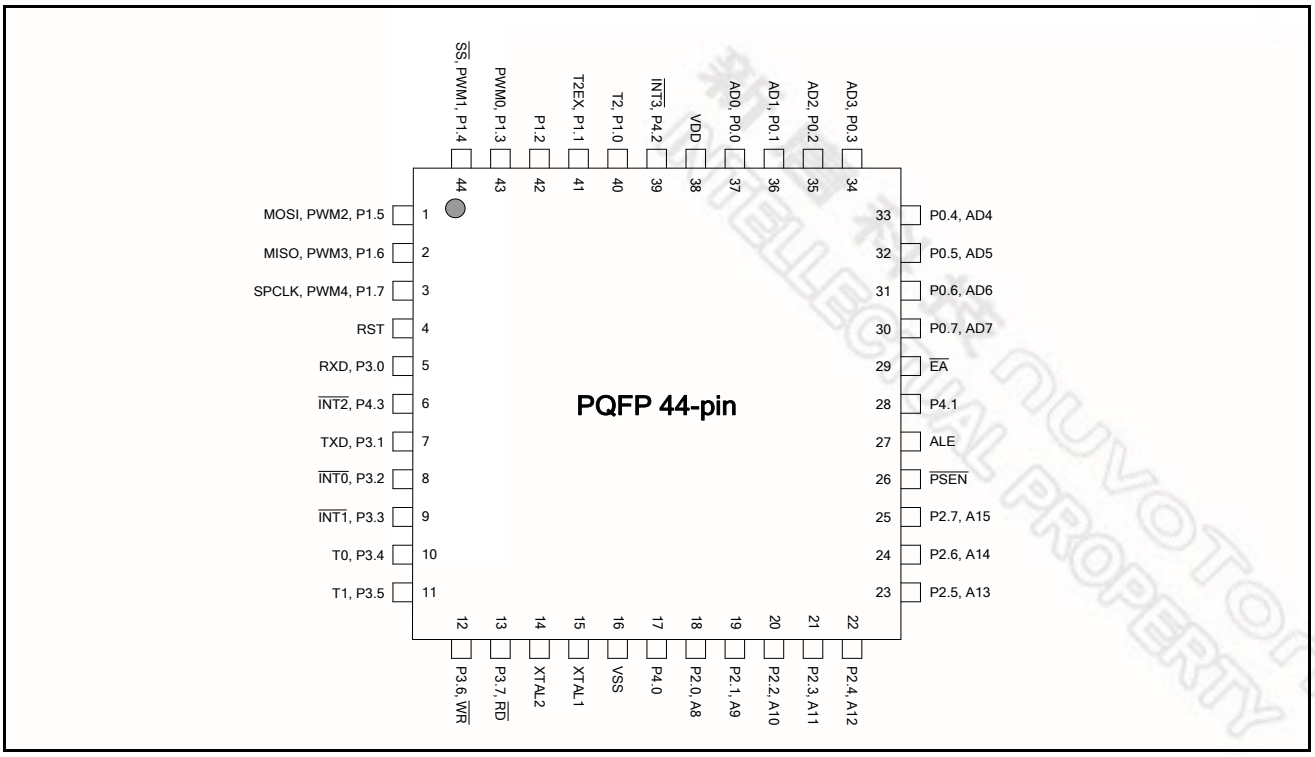

Figure 4–3. Pin Assignment of PQFP 44-Pin

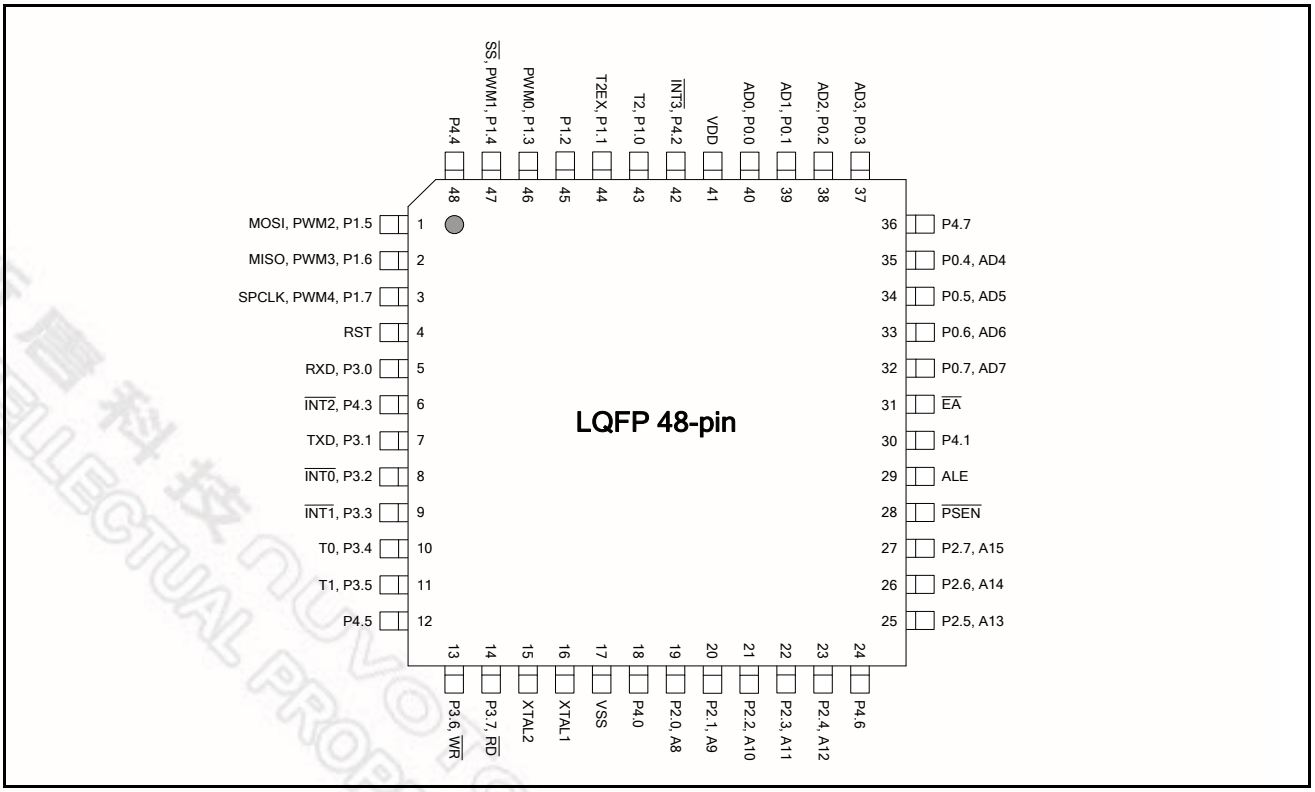

Figure 4–4. Pin Assignment of LQFP 48-Pin

Table 4–1. Pin Description

Pin number				Symbol	Alternate Function		Type[1]	Description
DIP	PLCC	PQFP	LQFP		1	2		
								an external capacitor to V_{DD}.
39	43	37	40	P0.0		AD0	D, I/O	**PORT0:** Port 0 is an 8-bit open-drain port by default. Via setting P0UP (P0OR.0), P0 will switch as weakly pulled up internally. P0 has an alternative function as AD[7:0] while external memory accessing. During the external memory access, P0 will output high will be internal strong pulled-up rather than weak pull-up in order to drive out high byte address for external devices.
38	42	36	39	P0.1		AD1	D, I/O	
37	41	35	38	P0.2		AD2	D, I/O	
36	40	34	37	P0.3		AD3	D, I/O	
35	39	33	35	P0.4		AD4	D, I/O	
34	38	32	34	P0.5		AD5	D, I/O	
33	37	31	33	P0.6		AD6	D, I/O	
32	36	30	32	P0.7		AD7	D, I/O	
1	2	40	43	P1.0	T2		I/O	**PORT1:** Port 1 is an 8-bit quasi bi-directional I/O port. Its multifunction pins are for T2, T2EX, PWM0~PWM4, $\overline{SS}$, MOSI, MISO, and SPCLK.
2	3	41	44	P1.1	T2EX		I/O	
3	4	42	45	P1.2			I/O	
4	5	43	46	P1.3	PWM0		I/O	
5	6	44	47	P1.4	PWM1	$\overline{SS}$	I/O	
6	7	1	1	P1.5	PWM2	MOSI	I/O	
7	8	2	2	P1.6	PWM3	MISO	I/O	
8	9	3	3	P1.7	PWM4	SPCLK	I/O	
21	24	18	19	P2.0		A8	I/O	**PORT2:** Port 2 is an 8-bit quasi bi-directional I/O port. It has an alternative function as A[15:8] while external memory accessing. During the external memory access, P2 will output high will be internal strong pulled-up rather than weak pull-up in order to drive out high byte address for external devices.
22	25	19	20	P2.1		A9	I/O	
23	26	20	21	P2.2		A10	I/O	
24	27	21	22	P2.3		A11	I/O	
25	28	22	23	P2.4		A12	I/O	
26	29	23	25	P2.5		A13	I/O	
27	30	24	26	P2.6		A14	I/O	
28	31	25	27	P2.7		A15	I/O	

Bit	Name	Description
2	OV	**Overflow flag.** OV is used for a signed character operands. For a ADD or ADDC instruction, OV will be set if there is a carry out of bit 6 but not out of bit 7, or a carry out of bit 7 but not bit 6. Otherwise, OV is cleared. OV indicates a negative number produced as the sum of two positive operands or a positive sum from two negative operands. For a SUBB, OV is set if a borrow is needed into bit6 but not into bit 7, or into bit7 but not bit 6. Otherwise, OV is cleared. OV indicates a negative number produced when a negative value is subtracted from a positive value, or a positive result when a positive number is subtracted from a negative number. For a MUL, if the product is greater than 255 (00FFH), OV will be set. Otherwise, it is cleared. For a DIV, it is normally 0. However, if B had originally contained 00H, the values returned in A and B will be undefined. Meanwhile, the OV will be set.
1	F1	**User flag 1.** The general purpose flag that can be set or cleared by the user via software.
0	P	**Parity flag.** Set to 1 to indicate an odd number of ones in the accumulator. Cleared for an even number of ones. It performs even parity check.

Table 7–1. Instructions that affect flag settings

Instruction	CY	OV	AC	Instruction	CY	OV	AC
ADD	X[1]	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	0	X		ANL C, /bit	X		
DIV	0	X		ORL C, bit	X		
DA A	X			ORL C, /bit	X		
RRC A	X			MOV C, bit	X		
RLC A	X			CJNE	X		
SETB C	1						

[1] X indicates the modification depends on the result of the instruction.

P3 – Port 3 (bit-addressable)

7	6	5	4	3	2	1	0
P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: B0H reset value: 1111 1111b

Bit	Name	Description
7:0	P3[7:0]	**Port 3.** Port 3 is an 8-bit quasi bi-directional I/O port.

P4 – Port 4 (bit-addressable)

7	6	5	4	3	2	1	0
P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: D8H reset value: 1111 1111b

Bit	Name	Description
7:0	P4[7:0]	**Port 4.** Port 4 is an 8-bit quasi bi-directional I/O port. It also possesses bit-addressable feature as P0~P3. Note that a full 8-bit P4 is just on LQPF-48 package. PLCC-44 and PQFP-44 just have low nibble 4 bits of P4. DIP-40 does not have this additional P4.

TH0 – Timer 0 High Byte

7	6	5	4	3	2	1	0
TH0[7:0]							
r/w							

Address: 8CH reset value: 0000 0000b

Bit	Name	Description
7:0	TH0[7:0]	**Timer 0 high byte.** The TH0 register is the high byte of the 16-bit Timer 0.

TL1 – Timer 1 Low Byte

7	6	5	4	3	2	1	0
TL1[7:0]							
r/w							

Address: 8BH reset value: 0000 0000b

Bit	Name	Description
7:0	TL1[7:0]	**Timer 1 low byte.** The TL1 register is the low byte of the 16-bit Timer 1.

TH1 – Timer 1 High Byte

7	6	5	4	3	2	1	0
TH1[7:0]							
r/w							

Address: 8DH reset value: 0000 0000b

Bit	Name	Description
7:0	TH1[7:0]	**Timer 1 high byte.** The TH1 register is the high byte of the 16-bit Timer 1.

10.1.1 Mode 0 (13-bit Timer)

In Mode 0, the Timer/Counter is a 13-bit counter. The 13-bit counter consists of THx and the five lower bits of TLx. The upper three bits of TLx are ignored. The Timer/Counter is enabled when TRx is set and either GATE is 0 or $\overline{INTx}$ is 1. Gate = 1 allows the Timer to calculate the pulse width on external input pin $\overline{INTx}$. When the 13-bit value moves from 1FFFH to 0000H, the Timer overflow flag TFx is set and an interrupt occurs if enabled. Note that the peripheral clock is $F_{OSC}/2$ in 12T mode and is F_{OSC} in 6T mode. See Section 20. "CLOCK SYSTEM" on page 102.

Table 10–1. Timer 2 Operating Modes

Timer 2 Mode	RCLK (T2CON.5) or TCLK (T2CON.4)	CP/$\overline{RL2}$ (T2CON.0)	T2OE (T2MOD.1)
16-bit capture[1]	0	1	X
16-bit auto-reload	0	0	0
Baud rate generator	1	X	0
Clock-out[2]	X	0	1

[1] The capture is valid while EXEN2 (T2CON.3) is a 1. Or Timer/Counter 2 behaves just like a 16-bit timer/counter.

[2] C/$\overline{T2}$ (T2CON.1) must be 0.

10.2.1 Capture Mode

The capture mode is enabled by setting the CP/$\overline{RL2}$ bit in the T2CON register to 1. In the capture mode, Timer/Counter 2 serves as a 16 bit up counter. When the counter rolls over from FFFFH to 0000H, the TF2 bit is set, which will generate an Timer 2 interrupt request. If the EXEN2 bit is set, then a negative transition of T2EX pin (alternative function of P1.1) will cause the value in the TL2 and TH2 register to be captured by the RCAP2L and RCAP2H registers. The TH2 and TL2 keeps on counting while this capture event occurs. This capture action also causes the EXF2 (T2CON.6) bit set, which will also generate an Timer 2 interrupt. If Timer 2 interrupt enabled, both TF2 and EXF2 flags will generate interrupt vectoring to the same location. The user should check which one triggers the Timer 2 interrupt in the interrupt service routine.

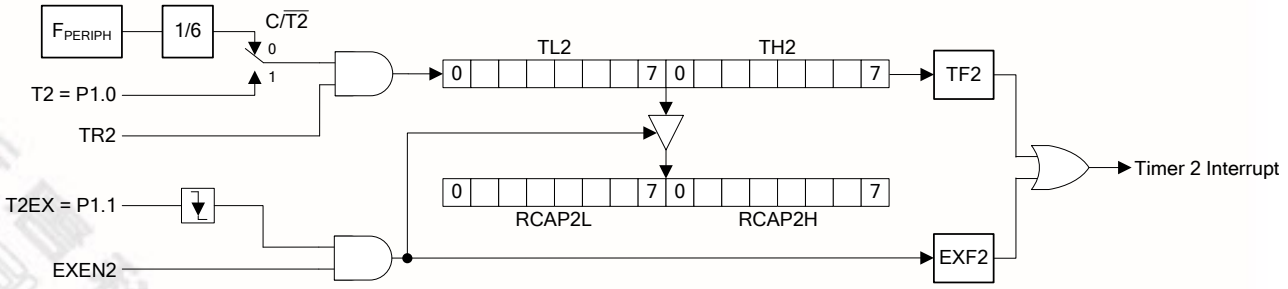

Figure 10–5. Timer/Counter 2 in Capture Mode

10.2.2 Auto-reload Mode

The auto-reload mode is enabled by clearing the CP/$\overline{RL2}$ bit in the T2CON register. In this mode, Timer/Counter 2 is a 16 bit up counter. When the counter rolls over from FFFFH, TF2 (T2CON.7) is set as 1 and a reload is generated that causes the contents of the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers respectively. If the EXEN2 bit is set, then a negative transition on T2EX pin will also cause a reload. This action also sets the EXF2 bit in T2CON.

CONFIG3

7	6	5	4	3	2	1	0
CWDTEN	EN6T	ROG	CKF	INTOSCFS	-	FOSC	-
r/w	r/w	r/w	r/w	r/w	-	r/w	-

unprogrammed value: 1111 1111b

Bit	Name	Description
7	CWDTEN	**CONFIG Watchdog Timer enable.** 1 = Disable Watchdog Timer after all resets. 0 = Enable Watchdog Timer after all resets.

WDCON – Watchdog Timer Control (TA protected)

7	6	5	4	3	2	1	0
WDTEN[1]	WDCLR	-	WIDPD[2]	WDTRF[3]	WPS2[2]	WPS1[2]	WPS0[2]
r/w	w	-	r/w	r/w	r/w	r/w	r/w

Address: AAH reset value: see Table 6–2. N78E059A/N78E055A SFR Descriptions and Reset Values

Bit	Name	Description
7	WDTEN	**Watchdog Timer enable.** 0 = Disable Watchdog Timer. 1 = Enable Watchdog Timer. The WDT counter starts running.
6	WDCLR	**Watchdog Timer clear.** Setting this bit will reset the Watchdog Timer count to 00H. It puts the counter in a known state and prohibit the system from reset. Note that this bit is written-only and has no need to be cleared via software.
5	-	**Reserved.**
4	WIDPD	**Watchdog Timer running in Idle and Power Down mode.** This bit decides whether Watchdog Timer runs in Idle or Power Down mode. 0 = WDT counter is halted while CPU is in Idle or Power Down mode. 1 = WDT keeps running while CPU is in Idle or Power Down mode.
3	WDTRF	**Watchdog Timer reset flag.** When the CPU is reset by Watchdog Timer time-out event, this bit will be set via hardware. This flag is recommended to be cleared via software.
2	WPS2	**Watchdog Timer clock pre-scalar select.** These bits determine the scale of the clock divider for WDT counter. The scale is from 1/1 through 1/256. See Table 11–1.
1	WPS1	
0	WPS0	

[1] WDTEN is initialized by the inversed value of CWDTEN (CONFIG3.7) after all resets.
[2] WIDPD and WPS[2:0] are cleared after power-on reset, and keep unchanged after any other resets.
[3] WDTRF will be cleared after power-on reset, be set after Watchdog Timer reset, and remains unchanged after any other resets.

The Watchdog time-out interval is determined by the formula $\frac{1}{F_{LOSC} \times clock\,divider\,scalar} \times 64$. Where F_{ILRC} is the frequency of internal 10kHz RC. The following table shows an example of the Watchdog time-out interval under different F_{WCK} and pre-scalars.

TH1 reload value	Oscillator Frequency (MHz)				
	11.0592	14.7456	18.432	22.1184	36.864
Baud Rate					
9600	FDh	FCh	FBh	FAh	F6h
4800	FAh	F8h	F6h	F4h	ECh
2400	F4h	F0h	ECh	E8h	D8h
1200	E8h	E0h	D8h	D0h	B0h
300	A0h	80h	60h	40h	

Table 13–4. Timer 2 Generated Commonly Used Baud Rates

RCAP2H, RCAP2L reload value	Oscillator Frequency (MHz)				
	11.0592	14.7456	18.432	22.1184	36.864
Baud Rate					
115200	FFh, FDh	FFh, FCh	FFh, FBh	FFh, FAh	FFh, F6h
57600	FFh, FAh	FFh, F8h	FFh, F6h	FFh, F4h	FFh, ECh
38400	FFh, F7h	FFh, F4h	FFh, F1h	FFh, EEh	FFh, E2h
19200	FFh, EEh	FFh, E8h	FFh, E2h	FFh, DCh	FFh, C4h
9600	FFh, DCh	FFh, D0h	FFh, C4h	FFh, B8h	FFh, 88h
4800	FFh, B8h	FFh, A0h	FFh, 88h	FFh, 70h	FFh, 10h
2400	FFh, 70h	FFh, 40h	FFh, 10h	FEh, E0h	FEh, 20h
1200	FEh, E0h	FEh, 80h	FEh, 20h	FDh, C0h	FCh, 40h
300	FBh, 80h	FAh, 00h	F8h, 80h	F7h, 00h	F1h, 00h

13.6 Multiprocessor Communication

N78E059A/N78E055A multiprocessor communication feature of UART lets a Master device send a multiple frame serial message to a Slave device in a multi-slave configuration. It does this without interrupting other slave devices that may be on the same serial line. This feature can be used only in UART mode 2 or 3 mode. After 9 data bits are received. The 9th bit value is written to RB8 (SCON.2). The user can enable this function by setting SM2 (SCON.5) as a logic 1 so that when the stop bit is received, the serial interrupt will be generated only if RB8 is 1. When the SM2 bit is 1, serial data frames that are received with the 9th bit as 0 do not generate an interrupt. In this case, the 9th bit simply separates the address from the serial data.

When the Master device wants to transmit a block of data to one of several slaves on a serial line, it first sends out an address byte to identify the target slave. Note that in this case, an address byte differs from a data byte: In an address byte, the 9th bit is 1 and in a data byte, it is 0. The address byte interrupts all slaves so that each slave can examine the received byte and see if it is being addressed. The addressed slave then clears its SM2

Concerning the Slave mode, the $\overline{SS}$ signal needs to be taken care. As shown in Figure 14–4. SPI Clock Formats, when CPHA = 0, the first SPCLK edge is the sampling strobe of MSB (for an example of LSBFE = 0, MSB first). Therefore, the Slave must shift its MSB data before the first SPCLK edge. The falling edge of $\overline{SS}$ is used for preparing the MSB on MISO line. The $\overline{SS}$ pin therefore must toggle high and then low between each successive serial byte. Furthermore, if the slave writes data to the SPI data register (SPDR) while $\overline{SS}$ is low, a write collision error occurs.

When CPHA = 1, the sampling edge thus locates on the second edge of SPCLK clock. The Slave uses the first SPCLK clock to shift MSB out rather than the $\overline{SS}$ falling edge. Therefore, the $\overline{SS}$ line can remain low between successive transfers. This format may be preferred in systems having single fixed Master and single fixed Slave. The $\overline{SS}$ line of the unique Slave device can be tied to V_{SS} as long as only CPHA = 1 clock mode is used.

Note: The SPI should be configured before it is enabled (SPIEN = 1), or a change of LSBFE, MSTR, CPOL, CPHA and SPR[1:0] will abort a transmission in progress and force the SPI system into idle state. Prior to any configuration bit changed, SPIEN must be disabled first.

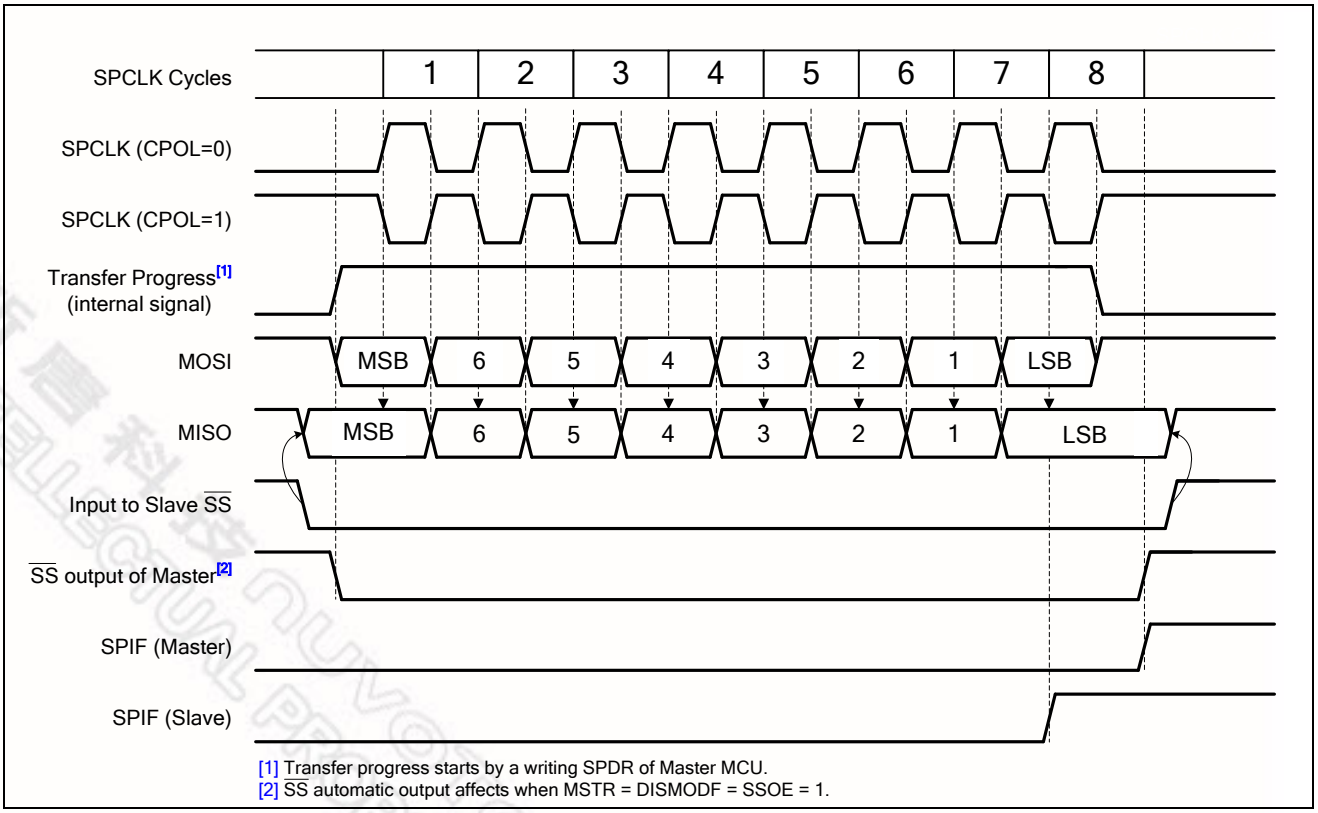

Figure 14–5. SPI Clock and Data Format with CPHA = 0

Bit	Name	Description
5	PT2	**Timer 2 interrupt priority low bit.**
4	PS	**Serial port (UART) interrupt priority low bit.**
3	PT1	**Timer 1 interrupt priority low bit.**
2	PX1	**External interrupt 1 priority low bit.**
1	PT0	**Timer 0 interrupt priority low bit.**
0	PX0	**External interrupt 0 priority low bit.**

[1] IP is used in combination with the IPH to determine the priority of each interrupt source. See Table 17–2. Interrupt Priority Level Setting for correct interrupt priority configuration.

IPH – Interrupt Priority High

7	6	5	4	3	2	1	0
PX3H[2]	PX2H[2]	PT2H[3]	PSH[3]	PT1H[3]	PX1H[3]	PT0H[3]	PX0H[3]
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: BAH reset value: 0000 0000b

Bit	Name	Description
7	PX3H	**External interrupt 3 priority high bit.**
6	PX2H	**External interrupt 3 priority high bit.**
5	PT2H	**Timer 2 interrupt priority high bit.**
4	PSH	**Serial port (UART) interrupt priority high bit.**
3	PT1H	**Timer 1 interrupt priority high bit.**
2	PX1H	**External interrupt 1 priority high bit.**
1	PT0H	**Timer 0 interrupt priority high bit.**
0	PX0H	**External interrupt 0 priority high bit.**

[2] PX2H and PX3H are used in combination with the PX2 (XICON.3) and PX3 (XICON.7) respectively to determine the priority of external interrupt 2 and 3. See Table 17–2. Interrupt Priority Level Setting for correct interrupt priority configuration.

[3] These bits is used in combination with the IP respectively to determine the priority of each interrupt source. See Table 17–2. Interrupt Priority Level Setting for correct interrupt priority configuration.

EIP – Extensive Interrupt Priority[4]

7	6	5	4	3	2	1	0
-	-	-	-	-	PBOD	PPDT	PSPI
-	-	-	-	-	r/w	r/w	r/w

Address: BCH reset value: 0000 0000b

Bit	Name	Description
7:3	-	**Reserved.**
2	PBOD	**Brown-out detection interrupt priority low bit.**
1	PPDT	**Power Down waking-up timer interrupt priority low bit.**
0	PSPI	**SPI interrupt priority low bit.**

XICON – External Interrupt Control (bit-addressable)

7	6	5	4	3	2	1	0
PX3[1]	EX3	IE3	IT3	PX2[1]	EX2	IE2	IT2
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: C0H reset value: 0000 0000b

Bit	Name	Description
7	PX3	**External interrupt 3 priority low bit.**
6	EX3	**Enable external interrupt 3.** 0 = Disable external interrupt 3. 1 = Enable interrupt generated by $\overline{INT3}$ pin (P4.2).
5	IE3	**External interrupt 3 edge flag.** This flag is set via hardware when an edge/level of type defined by IT3 is detected. If IT3 = 1, this bit will remain set until cleared via software or at the beginning of the External Interrupt 3 service routine. If IT3 = 0, this flag is the inverse of the $\overline{INT3}$ input signal's logic level.
4	IT3	**External interrupt 3 type select.** This bit selects whether the $\overline{INT3}$ pin will detect falling edge or low level triggered interrupts. 0 = $\overline{INT3}$ is low level triggered. 1 = $\overline{INT3}$ is falling edge triggered.
3	PX2	**External interrupt 2 priority low bit.**
2	EX2	**Enable external interrupt 2.** 0 = Disable external interrupt 2. 1 = Enable interrupt generated by $\overline{INT2}$ pin (P4.3).
1	IE2	**External interrupt 2 edge flag.** This flag is set via hardware when an edge/level of type defined by IT2 is detected. If IT2 = 1, this bit will remain set until cleared via software or at the beginning of the External Interrupt 2 service routine. If IT2 = 0, this flag is the inverse of the $\overline{INT2}$ input signal's logic level.
0	IT2	**External interrupt 2 type select.** This bit selects whether the $\overline{INT2}$ pin will detect falling edge or low level triggered interrupts. 0 = $\overline{INT2}$ is low level triggered. 1 = $\overline{INT2}$ is falling edge triggered.

[1] PX2 and PX3 are used in combination with the PX2H (IPH.6) and PX3H (IPH.7) respectively to determine the priority of external interrupt 2 and 3. See Table 17–2. Interrupt Priority Level Setting for correct interrupt priority configuration.

The External Interrupts $\overline{INT0}$ and $\overline{INT1}$ can be either edge or level triggered depending on bits IT0 (TCON.0) and IT1 (TCON.2). The bits IE0 (TCON.1) and IE1 (TCON.3) are the flags which are checked to generate the interrupt. In the edge triggered mode, the $\overline{INT0}$ or $\overline{INT1}$ inputs are sampled in every machine-cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IE0 or IE1 will be set. Since the external interrupts are sampled every machine-cycle, they have to be held high or low for at least one complete machine-cycle. The IE0 and IE1 are automatically cleared when the interrupt service routine is called. If the level triggered mode is selected, then the requesting source has to

Most of interrupt flags must be cleared by writing it as a logic 0 via software. Without clearing the flag, the ISR of corresponding interrupt source will execute again and again non-stopped.

17.1 Priority Level Structure

There are four priority levels for the interrupts, highest, high, low, and lowest. The interrupt sources can be individually set to one of four priority levels by setting their own priority bits. Table 17–2 lists four priority setting. Naturally, a low priority interrupt can itself be interrupted by a high priority interrupt, but not by another same level interrupt or lower level. A highest priority can't be interrupted by any other interrupt source. In addition, there exists a pre-defined hierarchy among the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown on Table 17–3. It also summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, natural priority and the permission to wake up the CPU from Power Down mode. For details of waking CPU up from Power Down mode, please see Section 19.2 "Power Down Mode" on page 100.

Table 17–2. Interrupt Priority Level Setting

Interrupt Priority Control Bits		Interrupt Priority Level
IPH / EIPH	IP / EIP / XICON[7,3]	
0	0	Level 0 (lowest)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest)

Table 17–3. Characteristics of Each Interrupt Source

Source	Vector Address	Flag	Enable Bit	Natural Priority	Priority Control Bits	Power Down Waking up
External interrupt 0	0003H	IE0[1]	EX0	1	PX0, PX0H	Yes
Timer 0 overflow	000BH	TF0[2]	ET0	2	PT0, PT0H	No
External interrupt 1	0013H	IE1[1]	EX1	3	PX1, PX1H	Yes
Timer 1 overflow	001BH	TF1[2]	ET1	4	PT1, PT1H	No
Serial port (UART)	0023H	RI + TI	ES	5	PS, PSH	No
Timer 2 overflow / capture / reload	002BH	TF2[2] + EXF2	ET2	6	PT2, PT2H	No
External interrupt 2	0033H	IE2[1]	EX2	7	PX2, PX2H	Yes
External interrupt 3	003BH	IE3[1]	EX3	8	PX3, PX3H	Yes

```
        CALL    Trigger_ISP
        MOV     B,R0
        MOV     A,ISPFD
        CJNE    A,B,Program_CONFIG_Verify_Error
        RET
Program_CONFIG_Verify_Error:
        CALL    Disable_ISP
        mov     P0,#00h
        SJMP    $
;*********************************************************************
;               APROM code
;*********************************************************************
AP_code :
        DB      75h, 90h, 55h               ;OPCODEs of "mov    P1,#55h"
        DB      75h,0A0h,0Aah               ;OPCODEs of "mov    P2,#0aah"
        DB      80h,0Feh                    ;OPCODEs of "sjmp   $"

        END
```

WDCON – Watchdog Timer Control (TA protected)

7	6	5	4	3	2	1	0
WDTEN	WDCLR	-	WIDPD	WDTRF	WPS2	WPS1	WPS0
r/w	w	-	r/w	r/w	r/w	r/w	r/w

Address: AAH reset value: see Table 6–2. N78E059A/N78E055A SFR Descriptions and Reset Values

Bit	Name	Description
3	WDTRF	**Watchdog Timer reset flag.** When the CPU is reset by Watchdog Timer time-out event, this bit will be set via hardware. This flag is recommended to be cleared via software.

22.1 Power-on Reset

N78E059A/N78E055A incorporate an internal voltage reference. During a power-on process of rising power supply voltage V_{DD}, this voltage reference will hold the CPU in power-on reset mode when V_{DD} is lower than the voltage reference threshold. This design makes CPU not access program flash while the V_{DD} is not adequate performing the flash reading. If a undetermined operating code is read from the program flash and executed, this will put CPU and even the whole system in to a erroneous state. After a while, V_{DD} rises above the reference threshold where the system can work, the selected oscillator will start and then program code will be executed from 0000H. At the same time, a power-on flag POF (PCON.4) will be set 1 to indicate a cold reset, a power-on reset complete. Note that the contents of internal RAM will be undetermined after a power-on. The user is recommended to give initial values for the RAM block.

The POF is recommended to be cleared to 0 via software in order to check if a cold reset or warm reset performed after the next reset occurs. If a cold reset caused by power off and on, POF will be set 1 again. If the reset is a warm reset caused by other reset sources, POF will remain 0. The user may take a different course to check other reset flags and deal with the warm reset event.

22.2 Brown-out Reset

Brown-out detection circuit is for monitoring the V_{DD} level during execution. When V_{DD} drops to the selected Brown-out trigger level (V_{BOD}), the Brown-out detection logic will reset the CPU if BORST (PMC.4) setting 1. After a Brown-out reset, BORF (RSR.2) will set 1 via hardware. It will not be altered by any reset other than a power-on reset. Software can clear this bit.

22.3 RST Pin Reset

The hardware reset input is RST pin which is the input with a Schmitt trigger. A hardware reset is accomplished by holding the RST pin high for at least two machine-cycles to ensure detection of a valid hardware reset sig-

CHPCON – Chip Control (TA protected)

7	6	5	4	3	2	1	0
SWRST	ISPF	LDUEN	XRAMEN	-	-	BS	ISPEN
w	r/w	r/w	r/w	-	-	r/w	r/w

Address: 9FH reset value: see Table 6–2. N78E059A/N78E055A SFR Descriptions and Reset Values

Bit	Name	Description
7	SWRST	**Software reset.** To set this bit as a logic 1 will cause a software reset. It will automatically be cleared via hardware after reset in finished.

The software demo code are listed below.

```
MOV TA,#0Aah              ;TA protection.
MOV TA,#55h               ;
ANL CHPCON,#0FDh          ;BS = 0, reset to APROM.
MOV TA,#0Aah
MOV TA,#55h
ORL CHPCON,#80h           ;Software reset
```

22.6 Boot Select

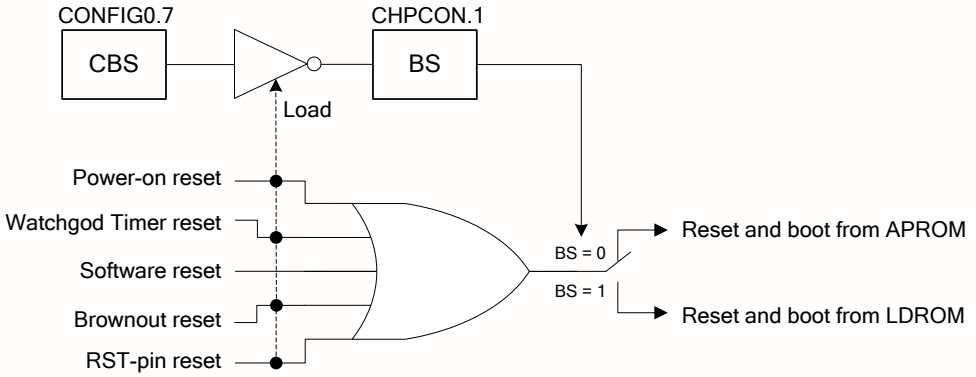

Figure 22–1. Boot Selecting Diagram

N78E059A/N78E055A provides users a flexible boot selection for variant application. The SFR bit BS in CHPCON.1 determines CPU booting from APROM or LDROM after any source of reset. If reset occurs and BS is 0, CPU will reboot from APPROM. Else, the CPU will reboot from LDROM.

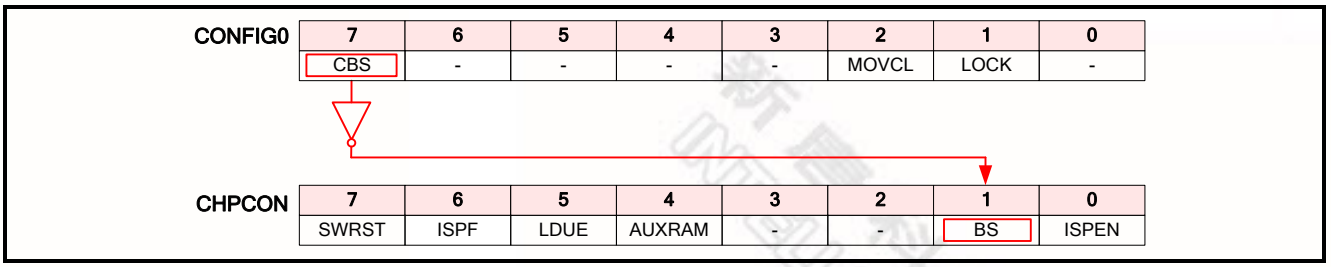

Figure 24–1. CONFIG0 Reset Reloading Except Software Reset

CONFIG2

7	6	5	4	3	2	1	0
CBODEN	CBOV1	CBOV0	CBORST	-	-	-	-
r/w	r/w	r/w	r/w	-	-	-	-

unprogrammed value: 1111 1111b

Bit	Name	Description
7	CBODEN	**CONFIG Brown-out detect enable.** 1 = Enable Brown-out detection. 0 = Disable Brown-out detection.
6	CBOV1	**CONFIG Brown-out voltage select.** These two bits select one of four Brown-out voltage level. CBOV1 CBOV0 Brown-out Voltage 1 1 2.2V 1 0 2.7V 0 1 3.8V 0 0 4.5V
5	CBOV0	
4	CBORST	**CONFIG Brown-out reset enable.** This bit decides if a Brown-out reset is caused after a Brown-out event. 1 = Enable Brown-out reset when V_{DD} drops below V_{BOD}. 0 = Disable Brown-out reset when V_{DD} drops below V_{BOD}.
3:0	-	**Reserved.**

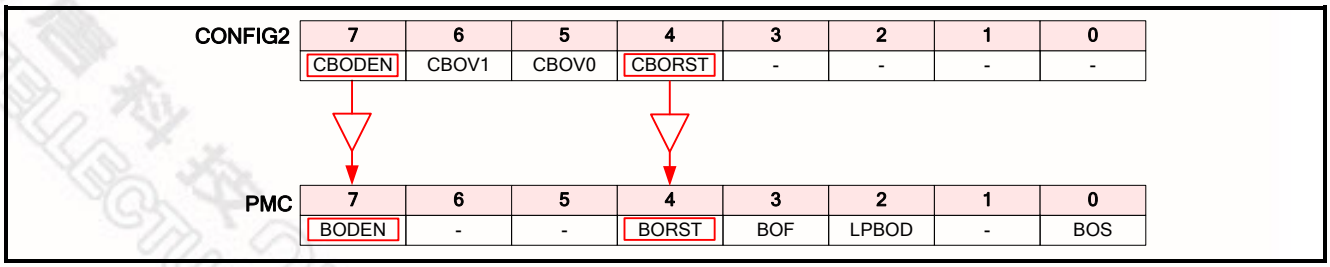

Figure 24–2. CONFIG2 Reset Reloading

CONFIG3

7	6	5	4	3	2	1	0
CWDTEN	EN6T	ROG	CKF	INTOSCFS	-	FOSC	-
r/w	r/w	r/w	r/w	r/w	-	r/w	-

unprogrammed value: 1111 1111b

Bit	Name	Description
7	CWDTEN	**CONFIG Watchdog Timer enable.** 1 = Disable Watchdog Timer after all resets. 0 = Enable Watchdog Timer after all resets.
6	EN6T	**Enable 6T mode.** This bit switches MCU between 12T and 6T mode. See Figure 20–1. Clock System Block Diagram for definitions in details. 1 = MCU runs at 12T mode. Each machine-cycle is equal to 12 clocks of system oscillator. The operating mode is the same as a standard 8051 MCU. (F_{CPU} and F_{PERIPH} is a half of F_{OSC}.) 0 = MCU runs at 6T mode. Each machine-cycle is equal to 6 clocks of system oscillator. This mode doubles the whole chip operation compared with the standard 8051. (F_{CPU} and F_{PERIPH} is equal to F_{OSC}.)
5	ROG	**Reducing oscillator gain.** 1 = Use normal gain for crystal oscillating. The frequency can be up to 40MHz. 0 = Use reduced gain for crystal oscillating. The frequency should be lower than 24MHz. In reduced gain mode, it will also help to decrease EMI.
4	CKF	**Clock filter enable.** 1 = Enable clock filter. It increases noise immunity and EMC capacity. 0 = Disable clock filter. ***Note that the clock filter should be always disabled if the crystal frequency is above 24MHz.***
3	INTOSCFS	**Internal RC oscillator frequency select.** 1 = Select 22.1184MHz as the system clock if internal RC oscillator mode is used. It bypasses the divided-by-2 path of internal oscillator to select 22.1184MHz output as the system clock source. 0 = Select 11.0592MHz as the system clock if internal RC oscillator mode is used. The internal RC divided-by-2 path is selected. The internal oscillator is equivalent to 11.0592MHz output used as the system clock.
2	-	**Reserved.**
1	FOSC	**Oscillator selection bit.** This bit selects the source of the system clock. 1 = Crystal, resonator, or external clock input. 0 = Internal RC oscillator.
0	-	**Reserved.**

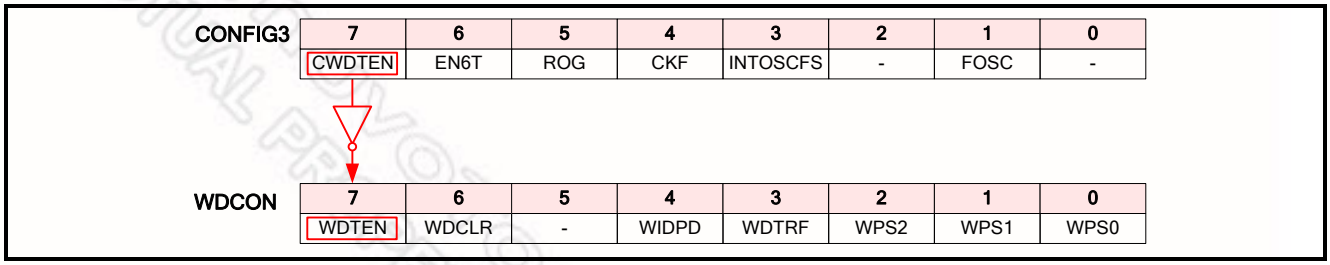

Figure 24–3. CONFIG3 Reset Reloading

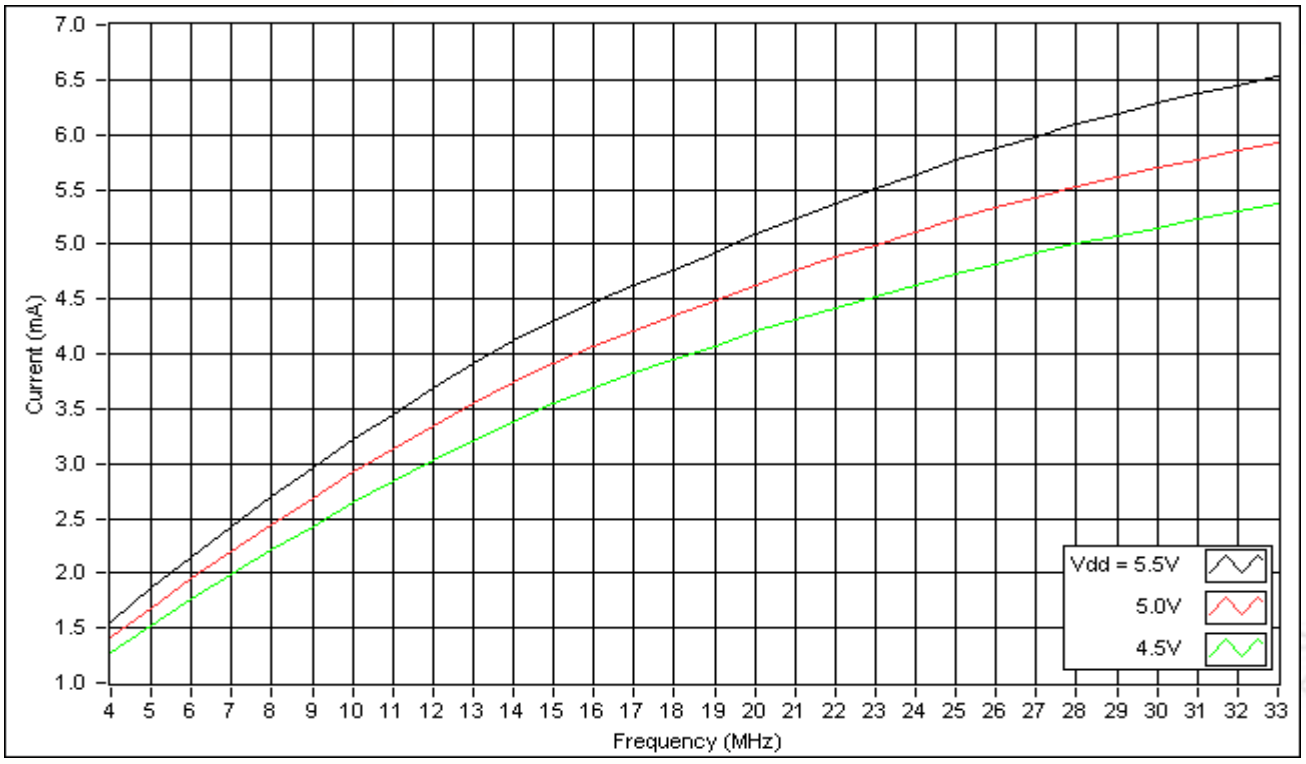

Figure 26–7. Idle Mode Current Under 6T Mode, External Clock (1)

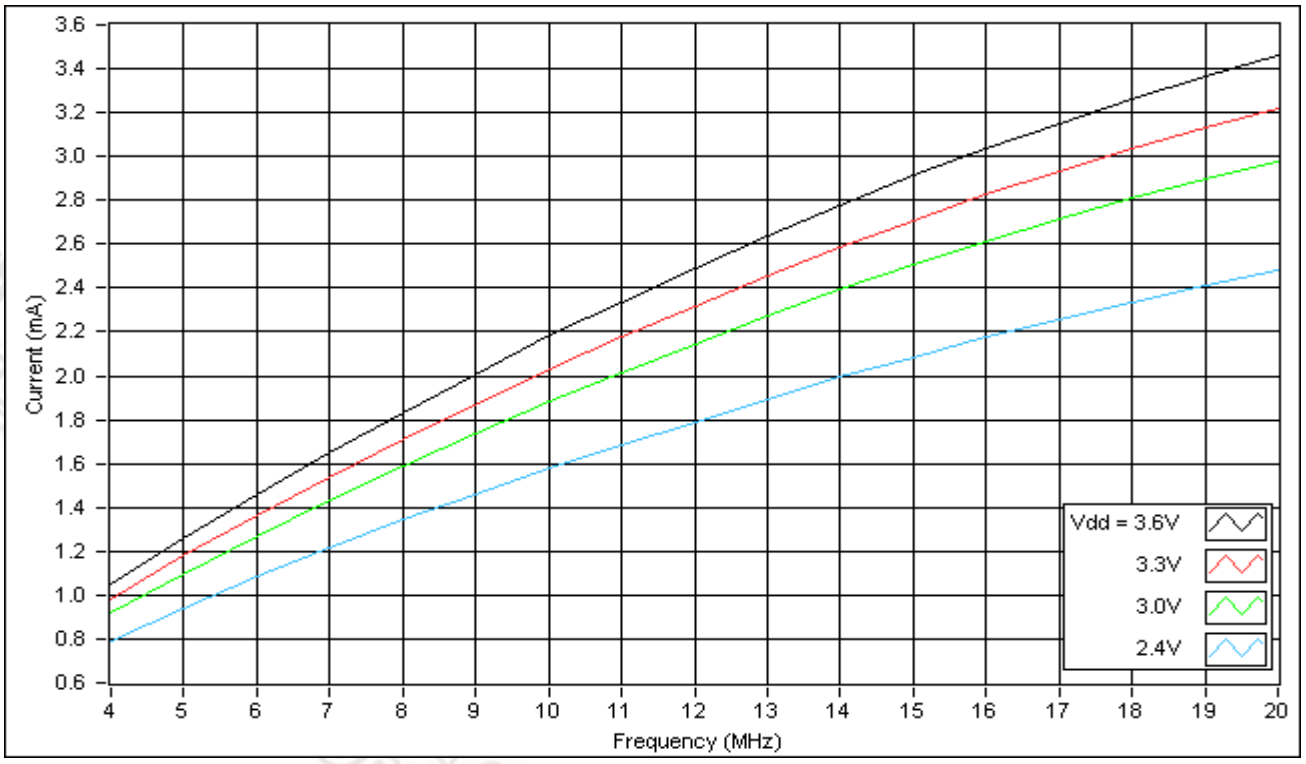

Figure 26–8. Idle Mode Current Under 6T Mode, External Clock (2)

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