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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega88a-mu

Table of Contents

Introduction.....	1
Feature.....	1
1. Description.....	4
2. Configuration Summary.....	5
3. Ordering Information	6
3.1. ATmega48A.....	6
3.2. ATmega88A	7
3.3. ATmega168A	8
4. Block Diagram.....	9
5. Pin Configurations.....	10
5.1. Pin-out.....	10
5.2. Pin Descriptions.....	14
6. I/O Multiplexing.....	16
7. Resources.....	18
8. Data Retention.....	19
9. About Code Examples.....	20
10. Capacitive Touch Sensing.....	21
10.1. QTouch Library.....	21
11. Packaging Information.....	22
11.1. 32-pin 32A.....	22
11.2. 32-pin 32M1-A.....	23
11.3. 32-pin 32CC1.....	24
11.4. 28-pin 28M1.....	25
11.5. 28-pin 28P3.....	26

1. Description

The Atmel AVR® core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in a single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega48A/88A/168A provides the following features: 4K/8K/16Kbytes of In-System Programmable Flash with Read-While-Write capabilities, 256/512/512bytes EEPROM, 512/1K/1Kbytes SRAM, 23 general purpose I/O lines, 32 general purpose working registers, Real Time Counter (RTC), three flexible Timer/Counters with compare modes and PWM, 1 serial programmable USARTs, 1 byte-oriented 2-wire Serial Interface (I2C), a 6-channel 10-bit ADC (8 channels in TQFP and QFN/MLF packages), a programmable Watchdog Timer with internal Oscillator, an SPI serial port, and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In Extended Standby mode, both the main oscillator and the asynchronous timer continue to run.

Atmel offers the QTouch® library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS™) technology for unambiguous detection of key events. The easy-to-use QTouch Suite toolchain allows you to explore, develop and debug your own touch applications.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega48A/88A/168A is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega48A/88A/168A is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

2. Configuration Summary

Features	ATmega48A/88A/168A
Pin Count	28/32
Flash (Bytes)	4K/8K/16K
SRAM (Bytes)	512/1K/1K
EEPROM (Bytes)	256/512/512
Interrupt Vector Size (instruction word/vector)	1/1/2
General Purpose I/O Lines	23
SPI	2
TWI (I ² C)	1
USART	1
ADC	10-bit 15kSPS
ADC Channels	8
8-bit Timer/Counters	2
16-bit Timer/Counters	1

ATmega88A and ATmega168A support a real Read-While-Write Self-Programming mechanism. There is a separate Boot Loader Section, and the SPM instruction can only execute from there. In ATmega48A, there is no Read-While-Write support and no separate Boot Loader Section. The SPM instruction can execute from the entire Flash.

3. Ordering Information

3.1. ATmega48A

Speed [MHz] ⁽³⁾	Power Supply [V]	Ordering Code ⁽²⁾	Package ⁽¹⁾	Operational Range
20	1.8 - 5.5	ATmega48A-AU ATmega48A-AUR ⁽⁴⁾ ATmega48A-CCU ATmega48A-CCUR ⁽⁴⁾ ATmega48A-MMH ⁽⁵⁾ ATmega48A-MMHR ⁽⁴⁾⁽⁵⁾ ATmega48A-MU ATmega48A-MUR ⁽⁴⁾ ATmega48A-PU	32A 32A 32CC1 32CC1 28M1 28M1 32M1-A 32M1-A 28P3	Industrial (-40°C to 85°C)

Note:

1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. Please refer to *Speed Grades* for Speed vs. V_{CC}
4. Tape & Reel.
5. NiPdAu Lead Finish.

Package Type	
28M1	28-pad, 4 x 4 x 1.0 body, Lead Pitch 0.45mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
28P3	28-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
32M1-A	32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
32A	32-lead, Thin (1.0mm) Plastic Quad Flat Package (TQFP)
32CC1	32-ball, 4 x 4 x 0.6mm package, ball pitch 0.5mm, Ultra Thin, Fine-Pitch Ball Grill Array (UFBGA)

3.3. ATmega168A

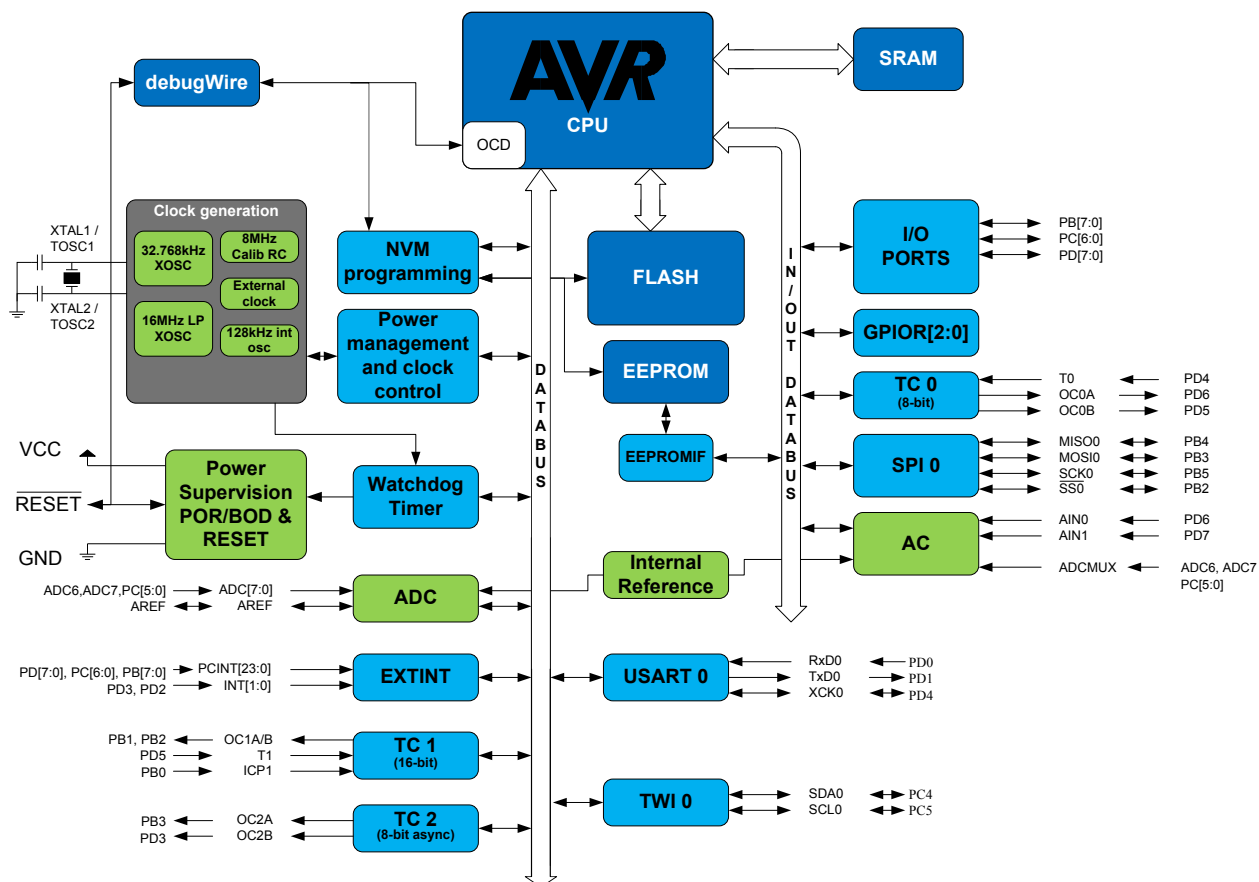
Speed [MHz] ⁽³⁾	Power Supply [V]	Ordering Code ⁽²⁾	Package ⁽¹⁾	Operational Range
20	1.8 - 5.5	ATmega168A-AU ATmega168A-AUR ⁽⁵⁾ ATmega168A-CCU ATmega168A-CCUR ⁽⁵⁾ ATmega168A-MMH ⁽⁴⁾ ATmega168A-MMHR ⁽⁴⁾⁽⁵⁾ ATmega168A-MU ATmega168A-MUR ⁽⁵⁾ ATmega168A-PU	32A 32A 32CC1 32CC1 28M1 28M1 32M1-A 32M1-A 28P3	Industrial (-40°C to 85°C)

Note:

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4. Tape & Reel.
5. NiPdAu Lead Finish.

Package Type	
28M1	28-pad, 4 x 4 x 1.0 body, Lead Pitch 0.45mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
28P3	28-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
32M1-A	32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
32A	32-lead, Thin (1.0mm) Plastic Quad Flat Package (TQFP)
32CC1	32-ball, 4 x 4 x 0.6mm package, ball pitch 0.5mm, Ultra Thin, Fine-Pitch Ball Grill Array (UFBGA)

Figure 4-1. Block Diagram



5. Pin Configurations

5.1. Pin-out

Figure 5-1. 28-pin PDIP

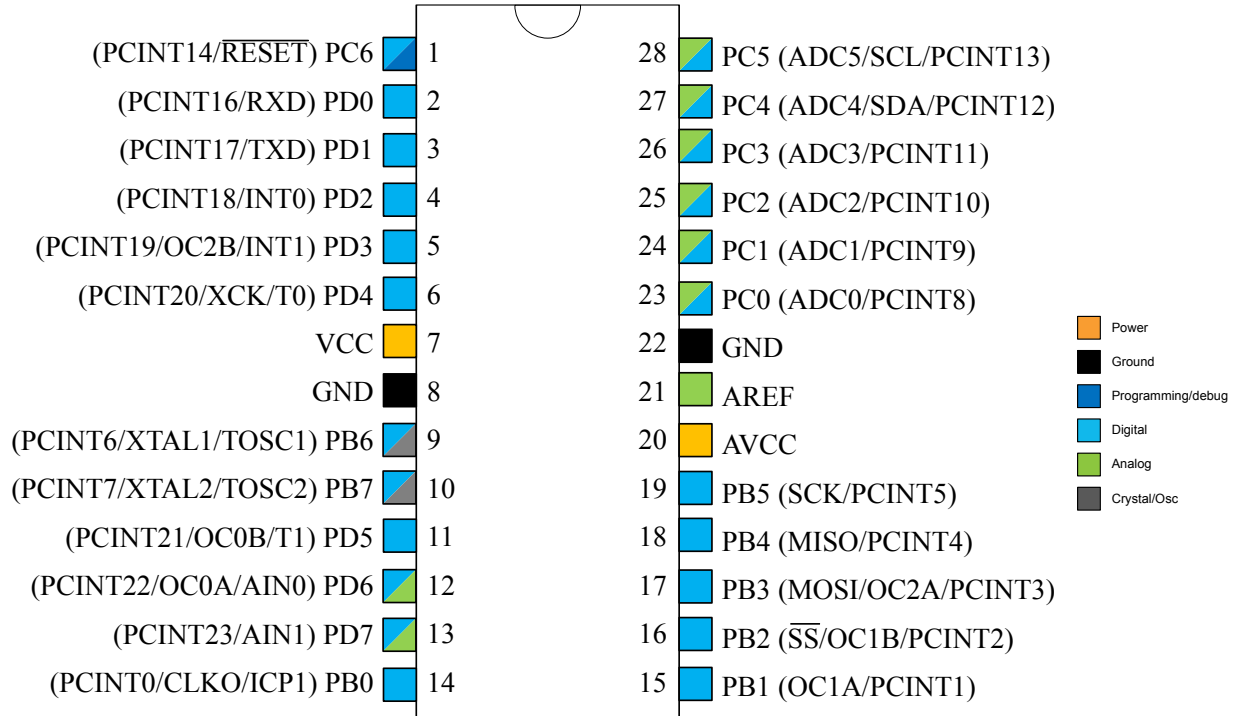


Figure 5-2. 28-pin MLF Top View

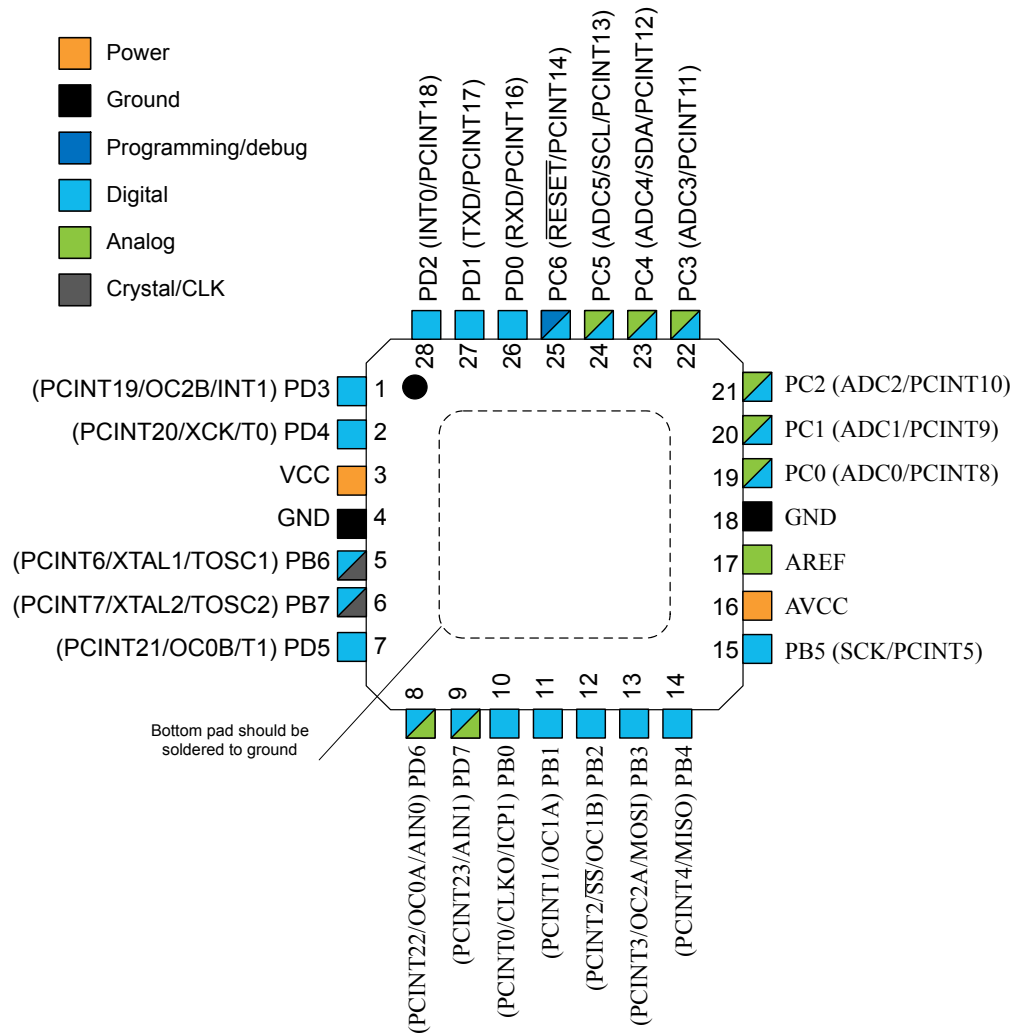
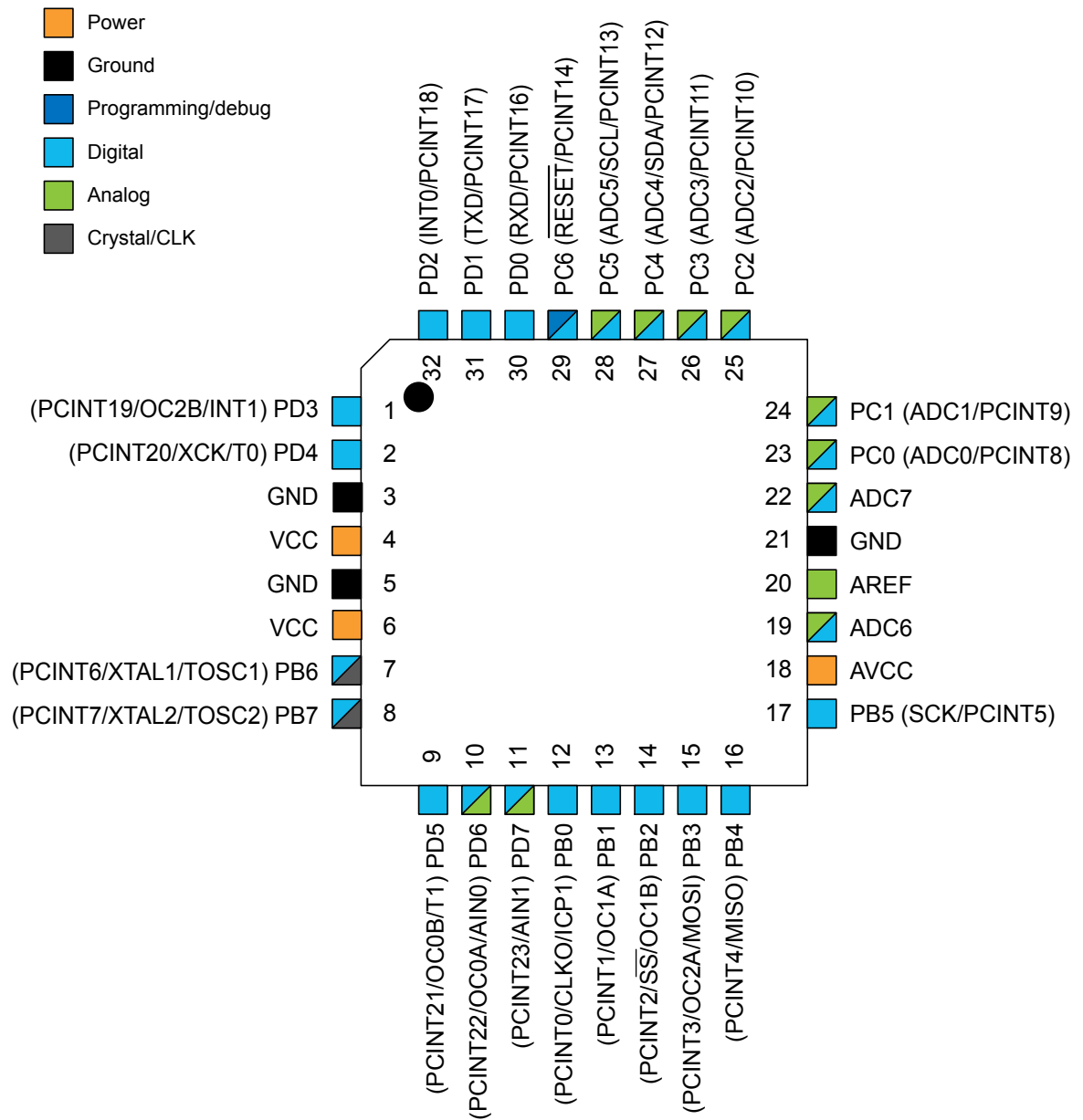


Figure 5-3. 32-pin TQFP Top View



Legend:

- Power (Orange)
- Ground (Black)
- Programming/debug (Blue)
- Digital (Light Blue)
- Analog (Green)
- Crystal/CLK (Grey)

Pin Functions:

Pin	Function(s)	Type
1	(PCINT19/OC2B/INT1) PD3	Digital
2	(PCINT20/XCK/T0) PD4	Digital
3	GND	Ground
4	VCC	Power
5	GND	Ground
6	VCC	Power
7	(PCINT6/XTAL1/TOSC1) PB6	Crystal/CLK
8	(PCINT7/XTAL2/TOSC2) PB7	Crystal/CLK
9	(PCINT21/OC0B/T1) PD5	Digital
10	(PCINT22/OC0A/AIN0) PD6	Analog
11	(PCINT23/AIN1) PD7	Analog
12	(PCINT0/CLKO/ICP1) PB0	Digital
13	(PCINT1/OC1A) PB1	Digital
14	(PCINT2/SS/OC1B) PB2	Digital
15	(PCINT3/OC2A/MOSI) PB3	Digital
16	(PCINT4/MISO) PB4	Digital
17	PB5 (SCK/PCINT5)	Digital
18	AVCC	Power
19	ADC6	Analog
20	AREF	Analog
21	GND	Ground
22	ADC7	Analog
23	PC0 (ADC0/PCINT8)	Analog
24	PC1 (ADC1/PCINT9)	Analog
25	PC2 (ADC2/PCINT10)	Analog
26	PC3 (ADC3/PCINT11)	Analog
27	PC4 (ADC4/SDA/PCINT12)	Analog
28	PC5 (ADC5/SCL/PCINT13)	Analog
29	PC6 (RESET/PCINT14)	Digital
30	PD0 (RXD/PCINT16)	Digital
31	PD1 (TXD/PCINT17)	Digital
32	PD2 (INT0/PCINT18)	Digital

Bottom pad should be soldered to ground

	1	2	3	4	5	6
A	PD2	PD1	PC6	PC4	PC2	PC1
B	PD3	PD4	PD0	PC5	PC3	PC0
C	GND	GND	-	-	ADC7	GND
D	VCC	VCC	-	-	AREF	ADC6
E	PB6	PD6	PB0	PB2	AVCC	PB5
F	PB7	PD5	PD7	PB1	PB3	PB4

5.2. Pin Descriptions

5.2.1. VCC

Digital supply voltage.

5.2.2. GND

Ground.

5.2.3. Port B (PB[7:0]) XTAL1/XTAL2/TOSC1/TOSC2

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Depending on the clock selection fuse settings, PB6 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PB7 can be used as output from the inverting Oscillator amplifier.

If the Internal Calibrated RC Oscillator is used as chip clock source, PB[7:6] is used as TOSC[2:1] input for the Asynchronous Timer/Counter2 if the AS2 bit in ASSR is set.

5.2.4. Port C (PC[5:0])

Port C is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The PC[5:0] output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

5.2.5. PC6/RESET

If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical characteristics of PC6 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a Reset.

The various special features of Port C are elaborated in the *Alternate Functions of Port C* section.

5.2.6. Port D (PD[7:0])

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

5.2.7. AV_{CC}

AV_{CC} is the supply voltage pin for the A/D Converter, PC[3:0], and PE[3:2]. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter. Note that PC[6:4] use digital supply voltage, V_{CC}.

5.2.8. AREF

AREF is the analog reference pin for the A/D Converter.

5.2.9. **ADC[7:6] (TQFP and VFQFN Package Only)**

In the TQFP and VFQFN package, ADC[7:6] serve as analog inputs to the A/D converter. These pins are powered from the analog supply and serve as 10-bit ADC channels.

6. I/O Multiplexing

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions.

The following table describes the peripheral signals multiplexed to the PORT I/O pins.

Table 6-1. PORT Function Multiplexing

(32-pin 32UFBGA) Pin#	(32-pin MLF/ TQFP) Pin#	(28-pin MLF) Pin#	(28-pin PIPD) Pin#	PAD	EXTINT	PCINT	ADC/A C	OSC	T/C #0	T/C #1	USART 0	I2C 0	SPI 0
B1	1	1	5	PD[3]	INT1	PCINT19			OC2B				
B2	2	2	6	PD[4]		PCINT20			T0		XCK0		
D1	4	3	7	VCC									
C1	3	4	8	GND									
D2	6	-	-	VCC									
C2	5	-	-	GND									
E1	7	5	9	PB[6]		PCINT6		XTAL1/ TOSC1					
F1	8	6	10	PB[7]		PCINT7		XTAL2/ TOSC2					
F2	9	7	11	PD[5]		PCINT21			OC0B	T1			
E2	10	8	12	PD[6]		PCINT22	AIN0		OC0A				
F3	11	9	13	PD[7]		PCINT23	AIN1						
E3	12	10	14	PB[0]		PCINT0		CLKO	ICP1				
F4	13	11	15	PB[1]		PCINT1			OC1A				
E4	14	12	16	PB[2]		PCINT2			OC1B				SS0
F5	15	13	17	PB[3]		PCINT3			OC2A				MOSI0
F6	16	14	18	PB[4]		PCINT4							MISO0
E6	17	15	19	PB[5]		PCINT5							SCK0
E5	18	16	20	AVCC									
D6	19	-	-	ADC6			ADC6						
D5	20	17	21	AREF									
C6	21	18	22	GND									
C5	22	-	-	ADC7			ADC7						
B6	23	19	13	PC[0]		PCINT8	ADC0						
A6	24	20	24	PC[1]		PCINT9	ADC1						
A2	25	21	25	PC[2]		PCINT10	ADC2						
B5	26	22	26	PC[3]		PCINT11	ADC3						
A4	27	23	27	PC[4]		PCINT12	ADC4					SDA0	
B4	28	24	28	PC[5]		PCINT13	ADC5					SCL0	

7. Resources

A comprehensive set of development tools, application notes, and datasheets are available for download on <http://www.atmel.com/avr>.

8. Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C.

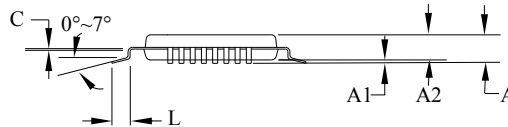
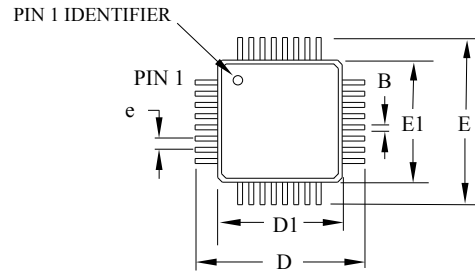
9. About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Confirm with the C compiler documentation for more details.

For I/O Registers located in extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically “LDS” and “STS” combined with “SBR”, “SBRC”, “SBR”, and “CBR”.

11. Packaging Information

11.1. 32-pin 32A



COMMON DIMENSIONS
(Unit of measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	
A1	0.05	—	0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	—	0.45	
C	0.09	—	0.20	
L	0.45	—	0.75	
e	0.80 TYP			

Notes:

1. This package conforms to JEDEC reference MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

2010-10-20

Atmel

TITLE

32A, 32-lead, 7 x 7mm body size, 1.0mm body thickness,
0.8mm lead pitch, thin profile plastic quad flat package (TQFP)

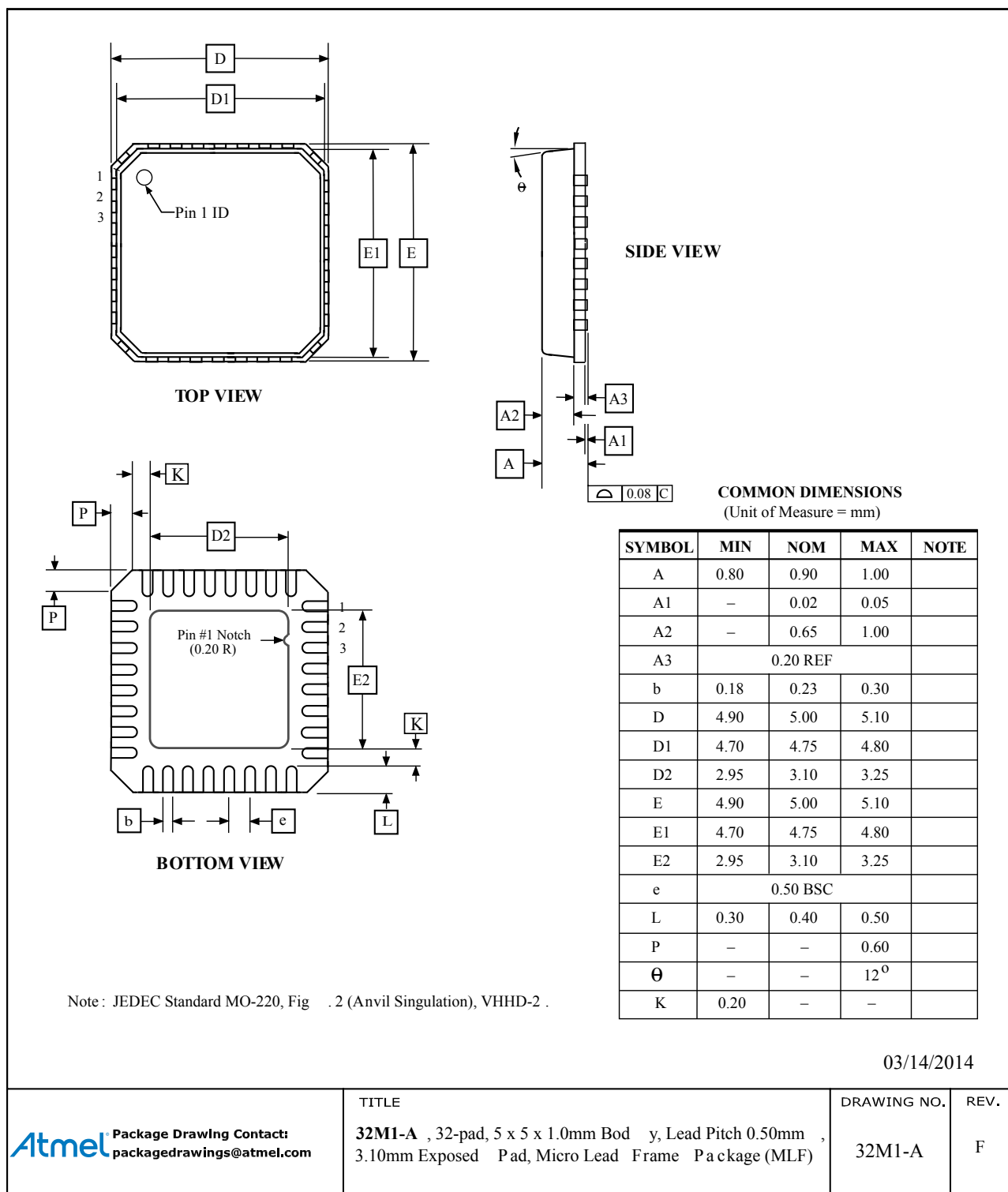
DRAWING NO.

32A

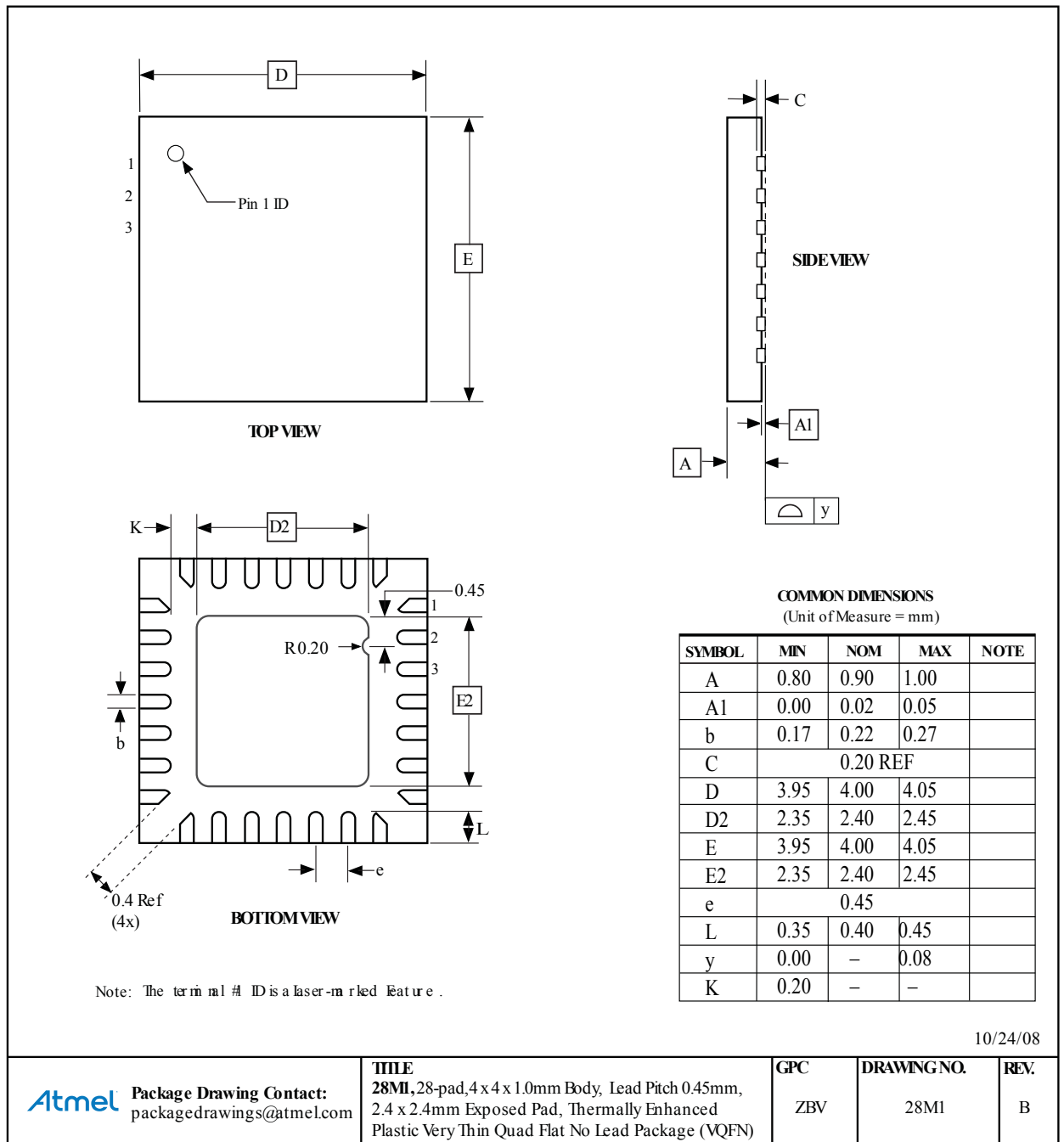
REV.

C

11.2. 32-pin 32M1-A



11.4. 28-pin 28M1



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