E·XFL

NXP USA Inc. - S9KEAZ128ACLH Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | CANbus, I²C, LINbus, SPI, UART/USART |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 58 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/s9keaz128aclh |

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- Timers
  - One 6-channel FlexTimer/PWM (FTM)
  - Two 2-channel FlexTimer/PWM (FTM)
  - One 2-channel periodic interrupt timer (PIT)
  - One pulse width timer (PWT)
  - One real-time clock (RTC)
- Communication interfaces
  - Two SPI modules (SPI)
  - Up to three UART modules (UART)
  - Two I2C modules (I2C)
  - One MSCAN module (MSCAN)
- Package options
  - 80-pin LQFP
  - 64-pin LQFP

# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **freescale.com** and perform a part number search for the following device numbers: KEAZ128.

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q B KEA A C FFF M T PP N

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • S = Automotive qualified<br>• P = Prequalification |
| B | Memory type | • 9 = Flash |
| KEA | Kinetis Auto family | • KEA |
| A | Key attribute | • Z = M0+ core<br>• F = M4 W/ DSP & FPU<br>• C= M4 W/ AP + FPU |
| C | CAN availability | • N = CAN not available<br>• (Blank) = CAN available |

*Table continues on the next page...*

| Field | Description | Values |
|---|---|---|
| FFF | Program flash memory size | • 128 = 128 KB |
| M | Maskset revision | • A = 1st Fab version<br>• B = Revision after 1st version |
| T | Temperature range (°C) | • C = –40 to 85<br>• V= –40 to 105<br>• M = –40 to 125 |
| PP | Package identifier | • LH = 64 LQFP (10 mm x 10 mm)<br>• LK = 80 LQFP (14 mm x 14 mm) |
| N | Packaging type | • R = Tape and reel<br>• (Blank) = Trays |

## 2.4 Example

This is an example part number:

S9KEAZ128AMLK

# 3 Ratings

## 3.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | –55 | 150 | °C | 1 |
| $T_{SDR}$ | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 3.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## Table 2. DC characteristics (continued)

| Symbol | Descriptions | | | Min | Typical[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $\|I_{INTOT}\|$ | Total leakage combined for all port pins | Pins in high impedance input mode | $V_{IN} = V_{DD}$ or $V_{SS}$ | — | — | 2 | µA |
| $R_{PU}$ | Pullup resistors | All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3) | — | 30.0 | — | 50.0 | kΩ |
| $R_{PU}$[3] | Pullup resistors | PTA2 and PTA3 pins | — | 30.0 | — | 60.0 | kΩ |
| $I_{IC}$ | DC injection current[4, 5, 6] | Single pin limit | $V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$ | -2 | — | 2 | mA |
| | | Total MCU limit, includes sum of all stressed pins | | -5 | — | 25 | |
| $C_{In}$ | Input capacitance, all pins | | — | — | — | 7 | pF |
| $V_{RAM}$ | RAM retention voltage | | — | 2.0 | — | — | V |

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 support high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to $V_{SS}$ and $V_{DD}$. PTA2 and PTA3 are true open drain I/O pins that are internally clamped to $V_{SS}$.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger value.
6. Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is higher than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Ensure that external $V_{DD}$ load will shunt current higher than maximum injection current when the MCU is not consuming power, such as when no system clock is present, or clock rate is very low (which would reduce overall power consumption).

## Table 3. LVD and POR specification

| Symbol | Description | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{POR}$ | POR re-arm voltage[1] | | 1.5 | 1.75 | 2.0 | V |
| $V_{LVDH}$ | Falling low-voltage detect threshold—high range (LVDV = 1)[2] | | 4.2 | 4.3 | 4.4 | V |
| $V_{LVW1H}$ | Falling low-voltage warning threshold— high range | Level 1 falling (LVWV = 00) | 4.3 | 4.4 | 4.5 | V |
| $V_{LVW2H}$ | | Level 2 falling (LVWV = 01) | 4.5 | 4.5 | 4.6 | V |
| $V_{LVW3H}$ | | Level 3 falling (LVWV = 10) | 4.6 | 4.6 | 4.7 | V |
| $V_{LVW4H}$ | | Level 4 falling (LVWV = 11) | 4.7 | 4.7 | 4.8 | V |
| $V_{HYSH}$ | High range low-voltage detect/ warning hysteresis | | — | 100 | — | mV |

*Table continues on the next page...*

## Table 3. LVD and POR specification (continued)

| Symbol | Description | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{LVDL}$ | Falling low-voltage detect threshold—low range (LVDV = 0) | | 2.56 | 2.61 | 2.66 | V |
| $V_{LVW1L}$ | Falling low-voltage warning threshold—low range | Level 1 falling (LVWV = 00) | 2.62 | 2.7 | 2.78 | V |
| $V_{LVW2L}$ | | Level 2 falling (LVWV = 01) | 2.72 | 2.8 | 2.88 | V |
| $V_{LVW3L}$ | | Level 3 falling (LVWV = 10) | 2.82 | 2.9 | 2.98 | V |
| $V_{LVW4L}$ | | Level 4 falling (LVWV = 11) | 2.92 | 3.0 | 3.08 | V |
| $V_{HYSDL}$ | Low range low-voltage detect hysteresis | | — | 40 | — | mV |
| $V_{HYSWL}$ | Low range low-voltage warning hysteresis | | — | 80 | — | mV |
| $V_{BG}$ | Buffered bandgap output [3] | | 1.14 | 1.16 | 1.18 | V |

1. Maximum is highest voltage that POR is guaranteed.
2. Rising thresholds are falling threshold + hysteresis.
3. voltage Factory trimmed at $V_{DD}$ = 5.0 V, Temp = 125 °C

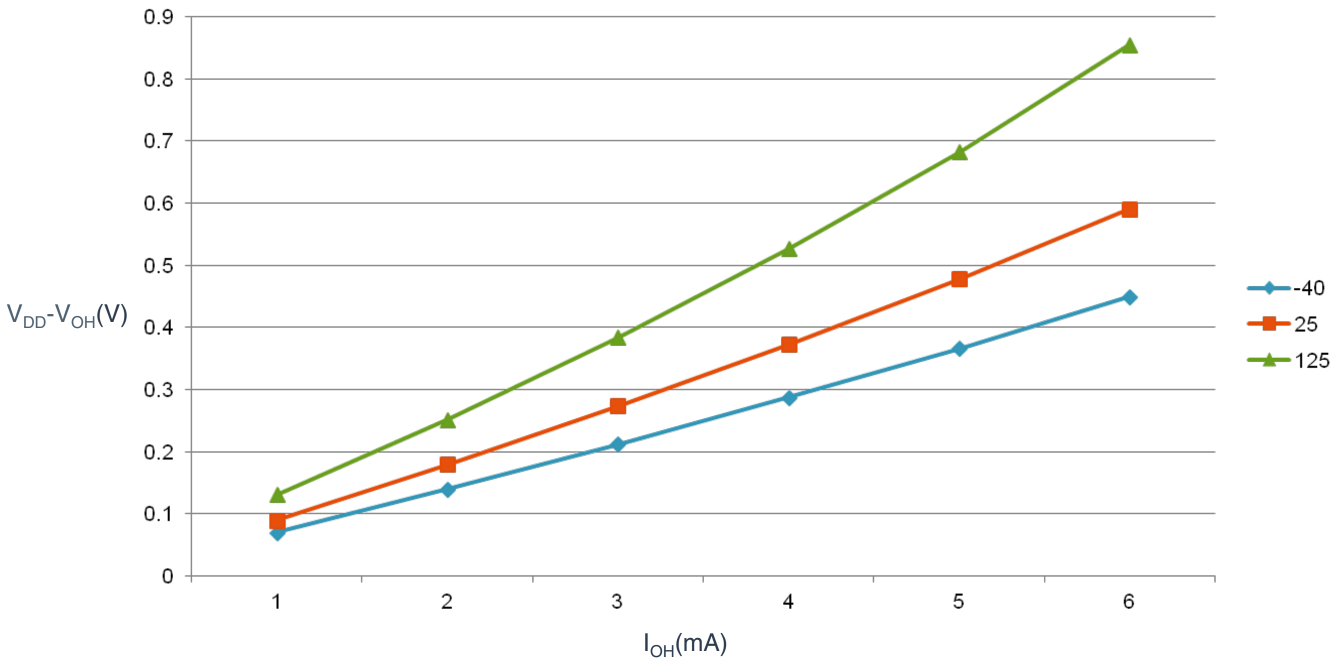


**Figure 1. Typical $V_{DD}$-$V_{OH}$ Vs. $I_{OH}$ (standard drive strength) ($V_{DD}$ = 5 V)**

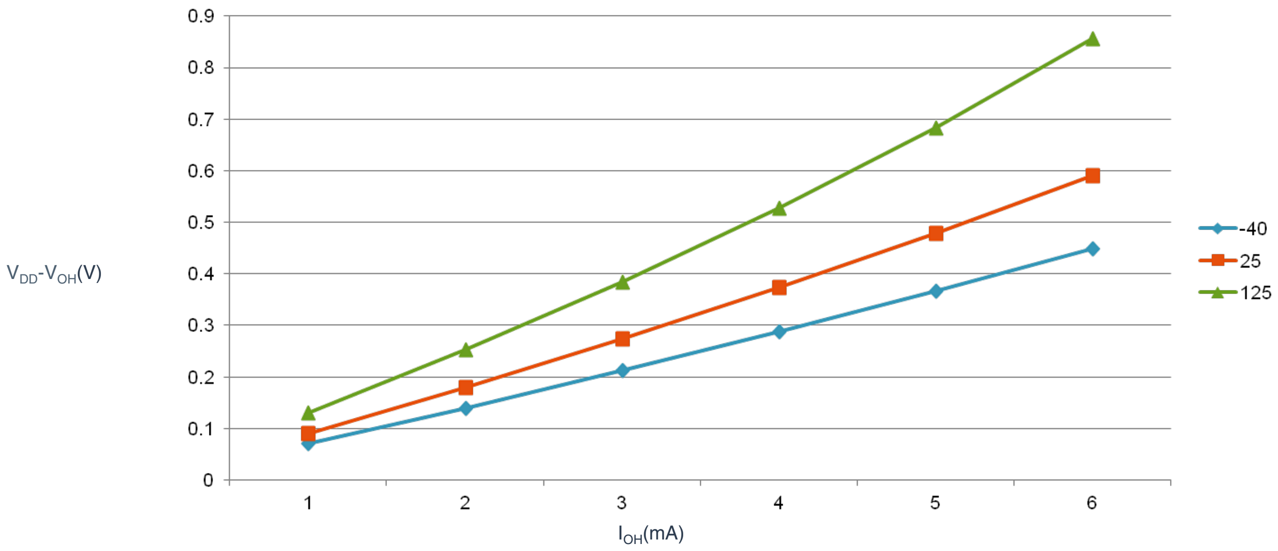


**Figure 2. Typical $V_{DD}$-$V_{OH}$ Vs. $I_{OH}$ (standard drive strength) ($V_{DD}$ = 3 V)**

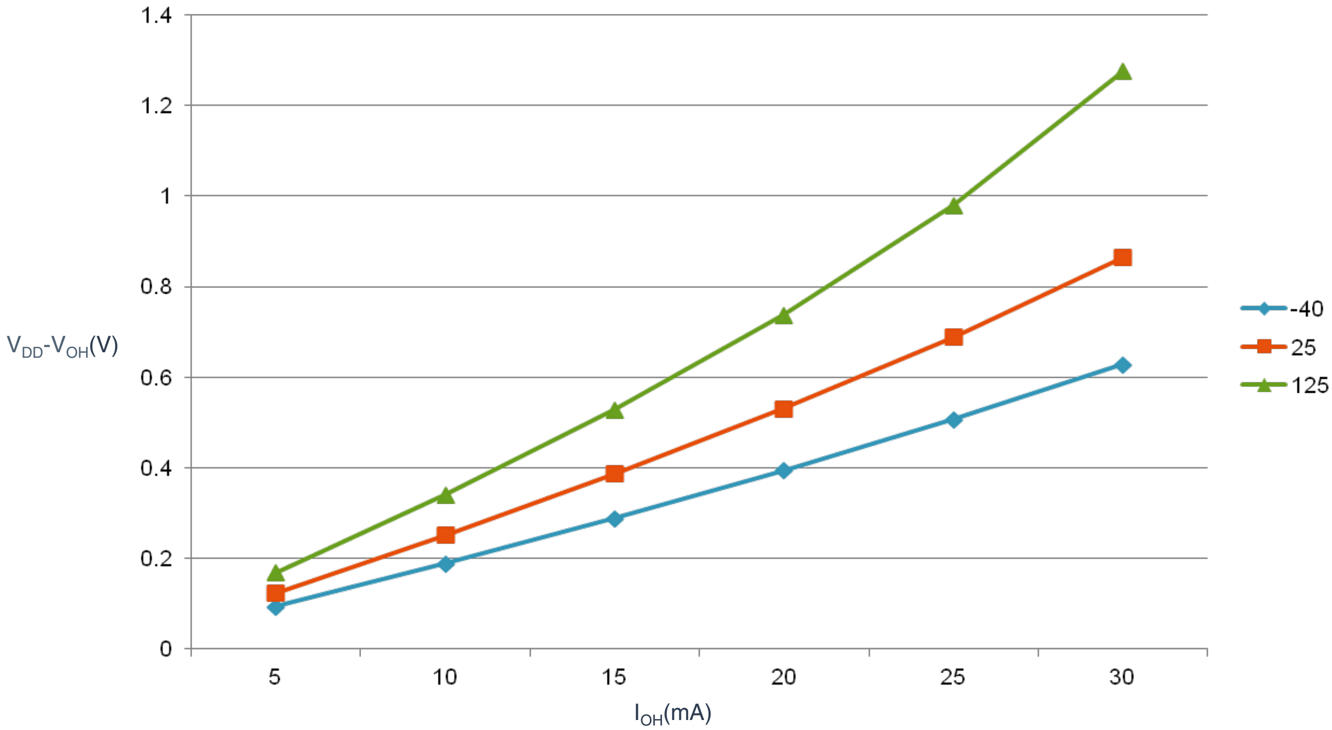


**Figure 3. Typical $V_{DD}$-$V_{OH}$ Vs. $I_{OH}$ (high drive strength) ($V_{DD}$ = 5 V)**

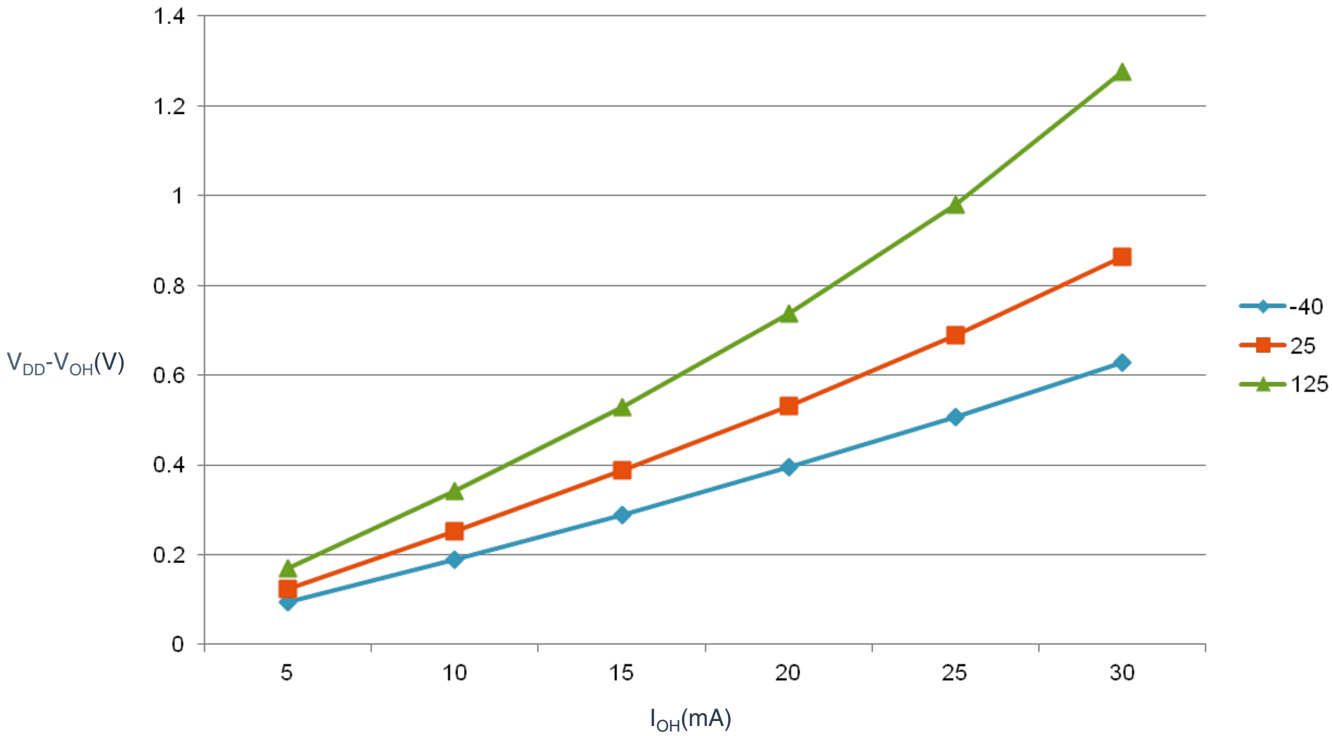


**Figure 4. Typical $V_{DD}$-$V_{OH}$ Vs. $I_{OH}$ (high drive strength) ($V_{DD}$ = 3 V)**

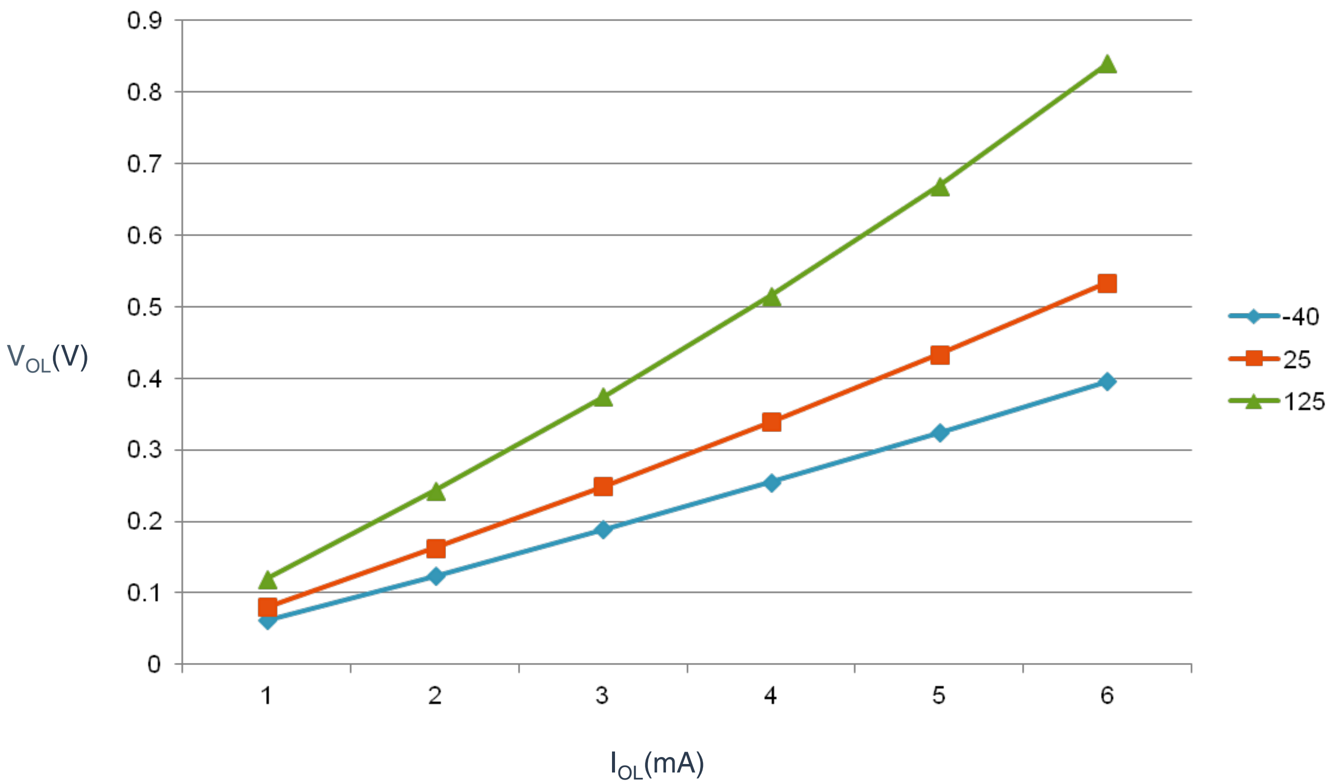


**Figure 5. Typical $V_{OL}$ Vs. $I_{OL}$ (standard drive strength) ($V_{DD}$ = 5 V)**

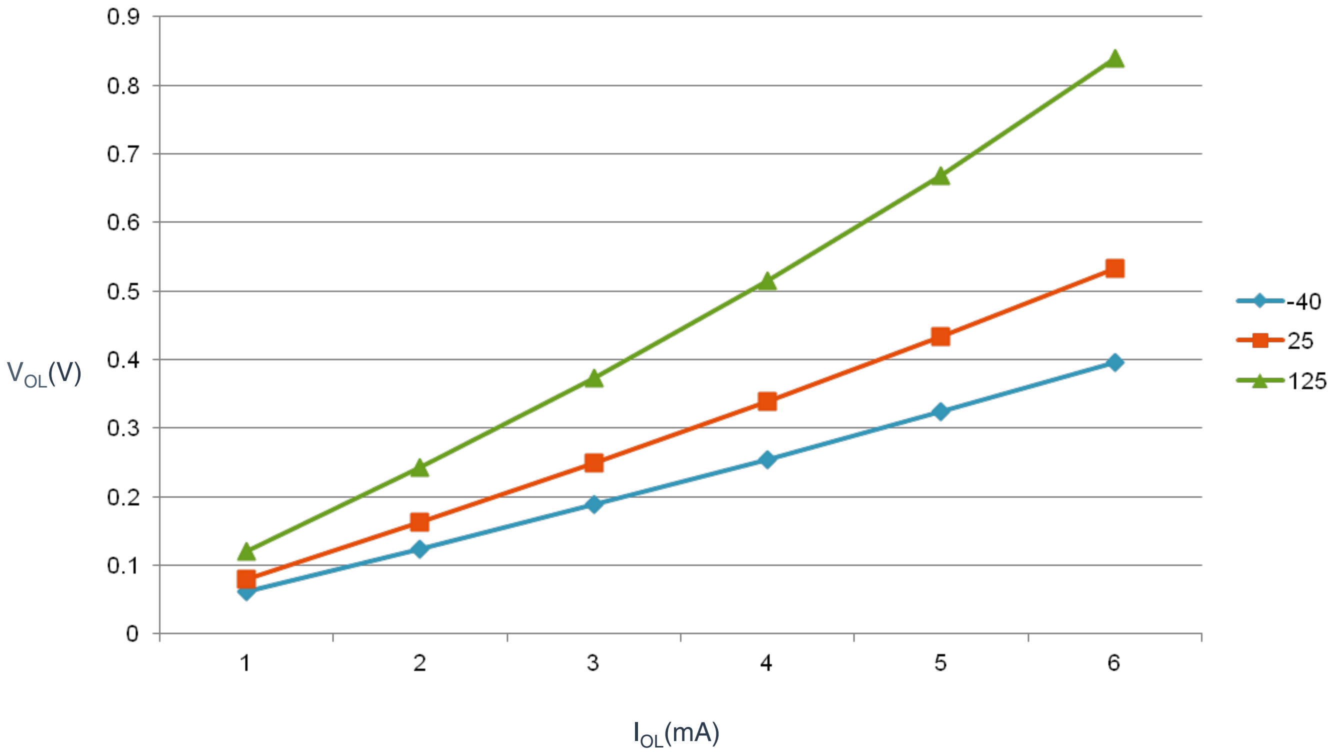


**Figure 6. Typical $V_{OL}$ Vs. $I_{OL}$ (standard drive strength) ($V_{DD}$ = 3 V)**

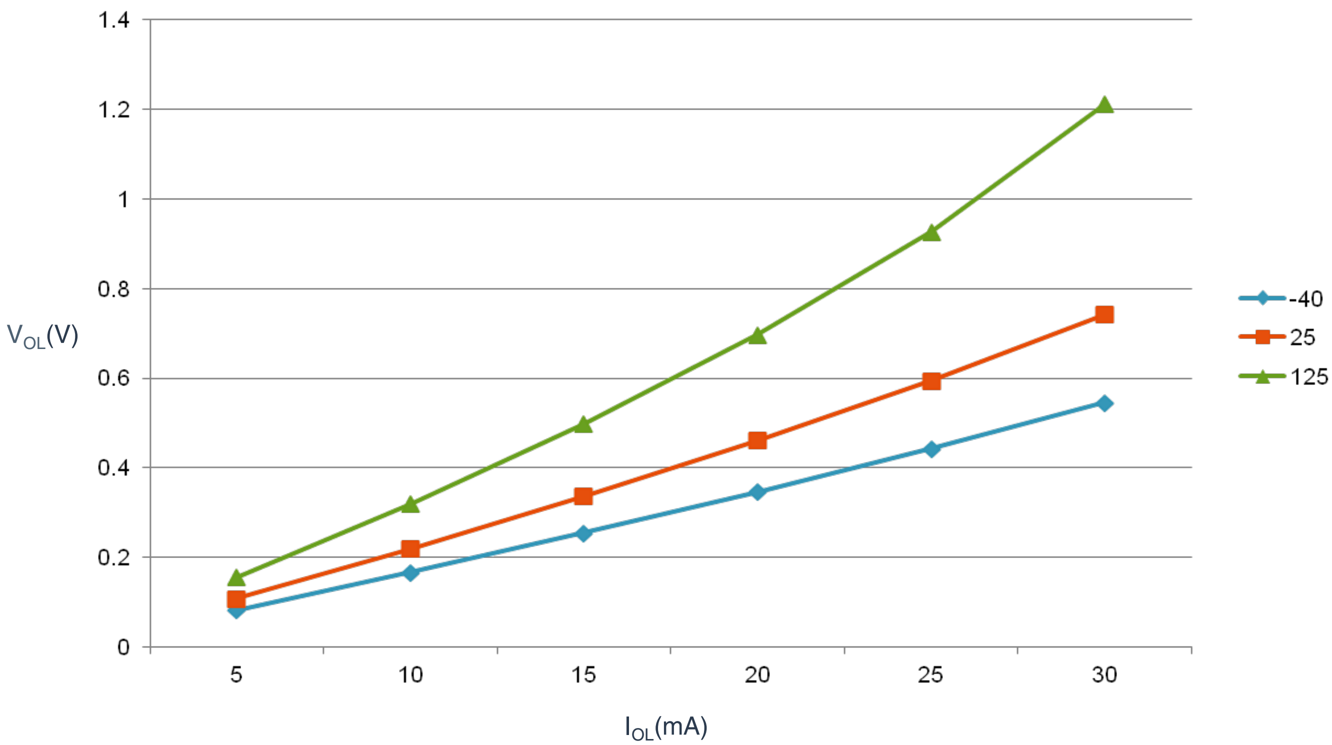


**Figure 7. Typical $V_{OL}$ Vs. $I_{OL}$ (high drive strength) ($V_{DD}$ = 5 V)**

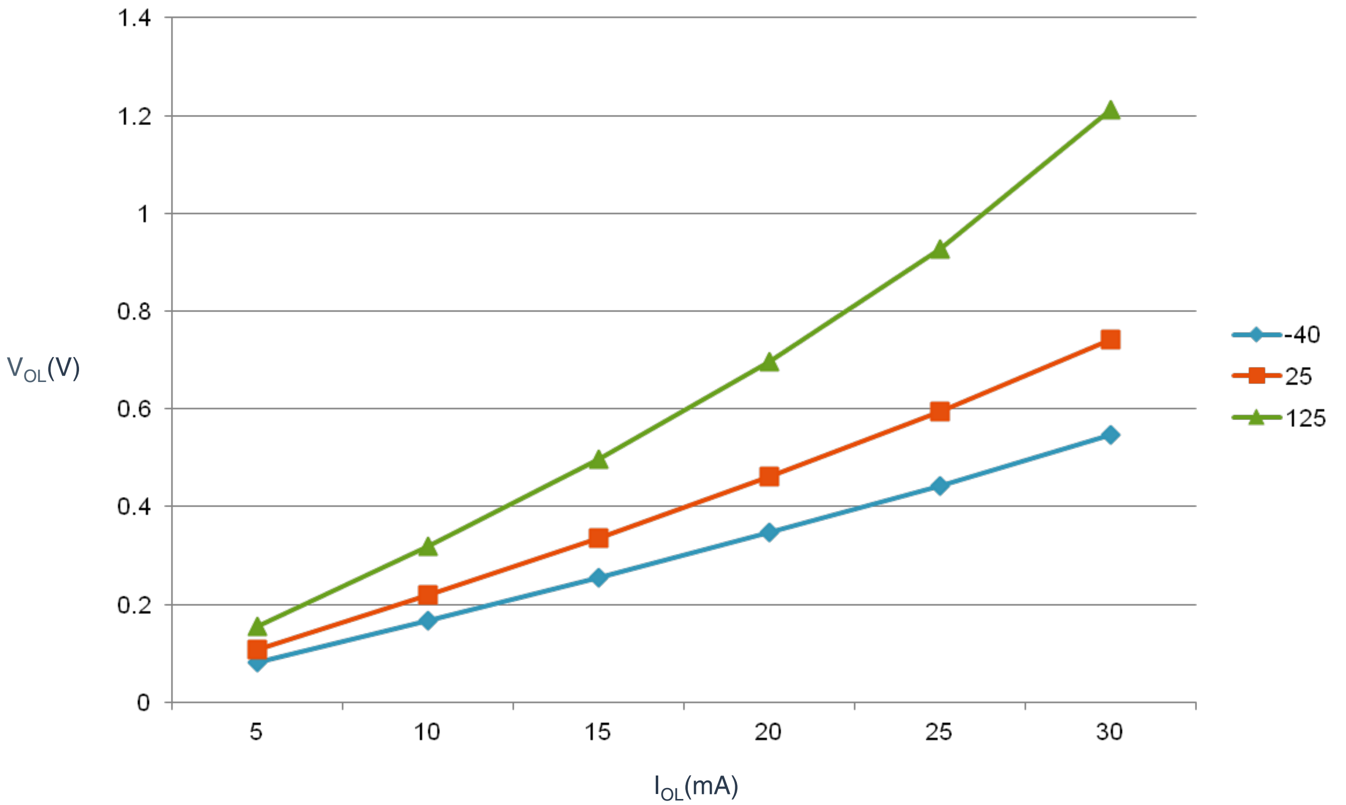


Figure 8. Typical $V_{OL}$ Vs. $I_{OL}$ (high drive strength) ($V_{DD}$ = 3 V)

### 4.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

| Parameter | Symbol | Core/Bus Freq | $V_{DD}$ (V) | Typical[1] | Max | Unit | Temp |
|---|---|---|---|---|---|---|---|
| Run supply current FEI mode, all modules clocks enabled; run from flash | $RI_{DD}$ | 48/24 MHz | 5 | 11.1 | — | mA | -40 to 125 °C |
| | | 24/24 MHz | | 8 | — | | |
| | | 12/12 MHz | | 5 | — | | |
| | | 1/1 MHz | | 2.4 | — | | |
| | | 48/24 MHz | 3 | 11 | — | | |
| | | 24/24 MHz | | 7.9 | — | | |
| | | 12/12 MHz | | 4.9 | — | | |
| | | 1/1 MHz | | 2.3 | — | | |
| Run supply current FEI mode, all modules clocks disabled and gated; run from flash | $RI_{DD}$ | 48/24 MHz | 5 | 7.8 | — | mA | -40 to 125 °C |
| | | 24/24 MHz | | 5.5 | — | | |
| | | 12/12 MHz | | 3.8 | — | | |
| | | 1/1 MHz | | 2.3 | — | | |

*Table continues on the next page...*

**Table 4. Supply current characteristics (continued)**

| Parameter | Symbol | Core/Bus Freq | $V_{DD}$ (V) | Typical[1] | Max | Unit | Temp |
|---|---|---|---|---|---|---|---|
| LVD adder to Stop[4] | — | — | 5 | 130 | — | μA | -40 to 125 °C |
| | | | 3 | 125 | — | | |

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. The high current is observed at high temperature.
3. RTC adder cause <1 μA $I_{DD}$ increase typically, RTC clock source is 1 kHz LPO clock.
4. LVD is periodically woken up from Stop by 5% duty cycle. The period is equal to or less than 2 ms.

### 4.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following Freescale applications notes, available on **freescale.com** for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

## 4.2 Switching specifications

### 4.2.1 Control timing

**Table 5. Control timing**

| Num | Rating | Symbol | Min | Typical[1] | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | System and core clock | $f_{Sys}$ | DC | — | 48 | MHz |
| 2 | Bus frequency ($t_{cyc}$ = 1/$f_{Bus}$) | $f_{Bus}$ | DC | — | 24 | MHz |
| 3 | Internal low power oscillator frequency | $f_{LPO}$ | 0.67 | 1.0 | 1.25 | KHz |
| 4 | External reset pulse width[2] | $t_{extrst}$ | 1.5 × $t_{cyc}$ | — | — | ns |

*Table continues on the next page...*

**Table 6. FTM input timing (continued)**

| Function | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| External clock period | $t_{TCLK}$ | 4 | — | $t_{cyc}$ |
| External clock high time | $t_{clkh}$ | 1.5 | — | $t_{cyc}$ |
| External clock low time | $t_{clkl}$ | 1.5 | — | $t_{cyc}$ |
| Input capture pulse width | $t_{ICPW}$ | 1.5 | — | $t_{cyc}$ |

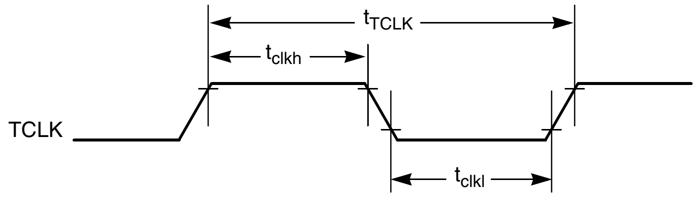


**Figure 11. Timer external clock**

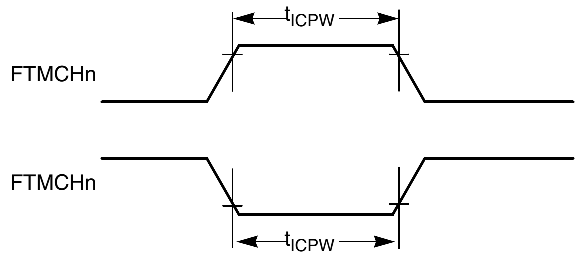


**Figure 12. Timer input capture pulse**

## 4.3 Thermal specifications

### 4.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and $V_{SS}$ or $V_{DD}$ and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and $V_{SS}$ or $V_{DD}$ will be very small.

## Table 7. Thermal attributes

| Board type | Symbol | Description | 64 LQFP | 80 LQFP | Unit | Notes |
|---|---|---|---|---|---|---|
| Single-layer (1S) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 71 | 57 | °C/W | 1, 2 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 53 | 44 | °C/W | 1, 3 |
| Single-layer (1S) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 59 | 47 | °C/W | 1, 3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 46 | 38 | °C/W | 1, 3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 35 | 28 | °C/W | 4 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 20 | 15 | °C/W | 5 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 5 | 3 | °C/W | 6 |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

The average chip-junction temperature ($T_J$) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

$T_A$ = Ambient temperature, °C

$\theta_{JA}$ = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between $P_D$ and $T_J$ (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C)$$

Solving the equations above for K gives:

$$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2$$

where K is a constant pertaining to the particular part. K can be determined by measuring $P_D$ (at equilibrium) for an known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving the above equations iteratively for any value of $T_A$.

# 5 Peripheral operating requirements and behaviors

## 5.1 Core modules

### 5.1.1 SWD electricals

**Table 8. SWD full voltage range electricals**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 2.7 | 5.5 | V |
| J1 | SWD_CLK frequency of operation<br>• Serial wire debug | 0 | 24 | MHz |
| J2 | SWD_CLK cycle period | 1/J1 | — | ns |
| J3 | SWD_CLK clock pulse width<br>• Serial wire debug | 20 | — | ns |
| J4 | SWD_CLK rise and fall times | — | 3 | ns |
| J9 | SWD_DIO input data setup time to SWD_CLK rise | 10 | — | ns |
| J10 | SWD_DIO input data hold time after SWD_CLK rise | 3 | — | ns |
| J11 | SWD_CLK high to SWD_DIO data valid | — | 35 | ns |
| J12 | SWD_CLK high to SWD_DIO high-Z | 5 | — | ns |

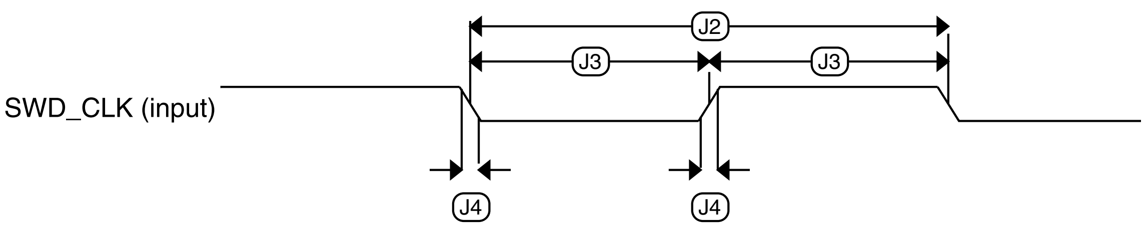


**Figure 13. Serial wire clock input timing**

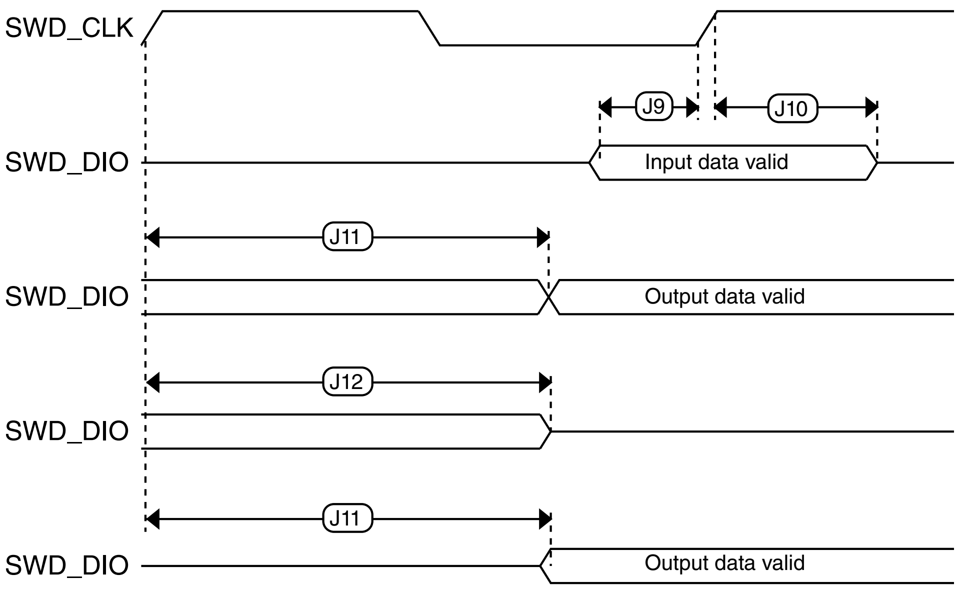


**Figure 14. Serial wire data timing**

## 5.2 External oscillator (OSC) and ICS characteristics

**Table 9. OSC and ICS specifications (temperature range = -40 to 125 °C ambient)**

| Num | Characteristic | | Symbol | Min | Typical[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | Crystal or resonator frequency | Low range (RANGE = 0) | $f_{lo}$ | 31.25 | 32.768 | 39.0625 | kHz |
| | | High range (RANGE = 1) | $f_{hi}$ | 4 | — | 24 | MHz |
| 2 | Load capacitors | | C1, C2 | See Note[2] | | | |
| 3 | Feedback resistor | Low Frequency, Low-Power Mode[3] | $R_F$ | — | — | — | MΩ |
| | | Low Frequency, High-Gain Mode | | — | 10 | — | MΩ |
| | | High Frequency, Low-Power Mode | | — | 1 | — | MΩ |
| | | High Frequency, High-Gain Mode | | — | 1 | — | MΩ |
| 4 | Series resistor - Low Frequency | Low-Power Mode [3] | $R_S$ | — | 0 | — | kΩ |
| | | High-Gain Mode | | — | 200 | — | kΩ |
| 5 | Series resistor - High Frequency | Low-Power Mode[3] | $R_S$ | — | 0 | — | kΩ |
| | Series resistor - High Frequency, High-Gain Mode | 4 MHz | | — | 0 | — | kΩ |
| | | 8 MHz | | — | 0 | — | kΩ |

*Table continues on the next page...*

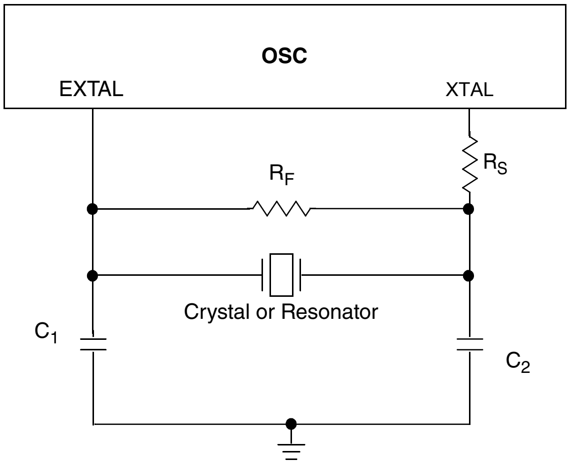


**Figure 15. Typical crystal or resonator circuit**

## 5.3 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash memories.

**Table 10. Flash characteristics**

| Characteristic | Symbol | Min[1] | Typical[2] | Max[3] | Unit[4] |
|---|---|---|---|---|---|
| Supply voltage for program/erase –40 °C to 125 °C | $V_{prog/erase}$ | 2.7 | — | 5.5 | V |
| Supply voltage for read operation | $V_{Read}$ | 2.7 | — | 5.5 | V |
| NVM Bus frequency | $f_{NVMBUS}$ | 1 | — | 24 | MHz |
| NVM Operating frequency | $f_{NVMOP}$ | 0.8 | 1 | 1.05 | MHz |
| Erase Verify All Blocks | $t_{VFYALL}$ | — | — | 2605 | $t_{cyc}$ |
| Erase Verify Flash Block | $t_{RD1BLK}$ | — | — | 2579 | $t_{cyc}$ |
| Erase Verify Flash Section | $t_{RD1SEC}$ | — | — | 485 | $t_{cyc}$ |
| Read Once | $t_{RDONCE}$ | — | — | 464 | $t_{cyc}$ |
| Program Flash (2 word) | $t_{PGM2}$ | 0.12 | 0.13 | 0.31 | ms |
| Program Flash (4 word) | $t_{PGM4}$ | 0.21 | 0.21 | 0.49 | ms |
| Program Once | $t_{PGMONCE}$ | 0.20 | 0.21 | 0.21 | ms |
| Erase All Blocks | $t_{ERSALL}$ | 95.42 | 100.18 | 100.30 | ms |
| Erase Flash Block | $t_{ERSBLK}$ | 95.42 | 100.18 | 100.30 | ms |
| Erase Flash Sector | $t_{ERSPG}$ | 19.10 | 20.05 | 20.09 | ms |
| Unsecure Flash | $t_{UNSECU}$ | 95.42 | 100.19 | 100.31 | ms |
| Verify Backdoor Access Key | $t_{VFYKEY}$ | — | — | 482 | $t_{cyc}$ |
| Set User Margin Level | $t_{MLOADU}$ | — | — | 415 | $t_{cyc}$ |
| FLASH Program/erase endurance $T_L$ to $T_H$ = -40 °C to 125 °C | $n_{FLPE}$ | 10 k | 100 k | — | Cycles |

*Table continues on the next page...*

**Table 10. Flash characteristics (continued)**

| Characteristic | Symbol | Min[1] | Typical[2] | Max[3] | Unit[4] |
|---|---|---|---|---|---|
| Data retention at an average junction temperature of $T_{Javg}$ = 85°C after up to 10,000 program/erase cycles | $t_{D\_ret}$ | 15 | 100 | — | years |

1. Minimum times are based on maximum $f_{NVMOP}$ and maximum $f_{NVMBUS}$
2. Typical times are based on typical $f_{NVMOP}$ and maximum $f_{NVMBUS}$
3. Maximum times are based on typical $f_{NVMOP}$ and typical $f_{NVMBUS}$ plus aging
4. $t_{cyc}$ = 1 / $f_{NVMBUS}$

Program and erase operations do not require any special power sources other than the normal $V_{DD}$ supply. For more detailed information about program/erase operations, see the Flash Memory Module section in the reference manual.

## 5.4 Analog

### 5.4.1 ADC characteristics

**Table 11. 5 V 12-bit ADC operating conditions**

| Characteristic | Conditions | Symbol | Min | Typ[1] | Max | Unit | Comment |
|---|---|---|---|---|---|---|---|
| Reference potential | • Low<br>• High | $V_{REFL}$<br>$V_{REFH}$ | $V_{SSA}$<br>$V_{DDA}/2$ | —<br>— | $V_{DDA}/2$<br>$V_{DDA}$ | V | — |
| Supply voltage | Absolute | $V_{DDA}$ | 2.7 | — | 5.5 | V | — |
| | Delta to $V_{DD}$ ($V_{DD}$-$V_{DDA}$) | $\Delta V_{DDA}$ | -100 | 0 | +100 | mV | — |
| Input voltage | | $V_{ADIN}$ | $V_{REFL}$ | — | $V_{REFH}$ | V | — |
| Input capacitance | | $C_{ADIN}$ | — | 4.5 | 5.5 | pF | — |
| Input resistance | | $R_{ADIN}$ | — | 3 | 5 | kΩ | — |
| Analog source resistance | 12-bit mode<br>• $f_{ADCK}$ > 4 MHz<br>• $f_{ADCK}$ < 4 MHz | $R_{AS}$ | —<br>— | —<br>— | 2<br>5 | kΩ | External to MCU |
| | 10-bit mode<br>• $f_{ADCK}$ > 4 MHz<br>• $f_{ADCK}$ < 4 MHz | | —<br>— | —<br>— | 5<br>10 | | |
| | 8-bit mode<br>(all valid $f_{ADCK}$) | | — | — | 10 | | |
| ADC conversion clock frequency | High speed (ADLPC=0) | $f_{ADCK}$ | 0.4 | — | 8.0 | MHz | — |
| | Low power (ADLPC=1) | | 0.4 | — | 4.0 | | |

## Table 12. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Characteristic | Conditions | Symbol | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| ADC asynchronous clock source | High speed (ADLPC = 0) | $f_{ADACK}$ | 2 | 3.3 | 5 | MHz |
| | Low power (ADLPC = 1) | | 1.25 | 2 | 3.3 | |
| Conversion time (including sample time) | Short sample (ADLSMP = 0) | $t_{ADC}$ | — | 20 | — | ADCK cycles |
| | Long sample (ADLSMP = 1) | | — | 40 | — | |
| Sample time | Short sample (ADLSMP = 0) | $t_{ADS}$ | — | 3.5 | — | ADCK cycles |
| | Long sample (ADLSMP = 1) | | — | 23.5 | — | |
| Total unadjusted Error[2] | 12-bit mode | $E_{TUE}$ | — | ±5.0 | — | LSB[3] |
| | 10-bit mode | | — | ±1.5 | — | |
| | 8-bit mode | | — | ±0.8 | — | |
| Differential Non-Liniarity | 12-bit mode | DNL | — | ±1.5 | — | LSB[3] |
| | 10-bit mode | | — | ±0.4 | — | |
| | 8-bit mode | | — | ±0.15 | — | |
| Integral Non-Linearity | 12-bit mode | INL | — | ±1.5 | — | LSB[3] |
| | 10-bit mode | | — | ±0.4 | — | |
| | 8-bit mode | | — | ±0.15 | — | |
| Zero-scale error[4] | 12-bit mode | $E_{ZS}$ | — | ±1.0 | — | LSB[3] |
| | 10-bit mode | | — | ±0.2 | — | |
| | 8-bit mode | | — | ±0.35 | — | |
| Full-scale error[5] | 12-bit mode | $E_{FS}$ | — | ±2.5 | — | LSB[3] |
| | 10-bit mode | | — | ±0.3 | — | |
| | 8-bit mode | | — | ±0.25 | — | |
| Quantization error | ≤12 bit modes | $E_Q$ | — | — | ±0.5 | LSB[3] |
| Input leakage error[6] | all modes | $E_{IL}$ | | $I_{In} \times R_{AS}$ | | mV |
| Temp sensor slope | -40 °C–25 °C | m | — | 3.266 | — | mV/°C |
| | 25 °C–125 °C | | — | 3.638 | — | |
| Temp sensor voltage | 25 °C | $V_{TEMP25}$ | — | 1.396 | — | V |

1. Typical values assume $V_{DDA}$ = 5.0 V, Temp = 25 °C, $f_{ADCK}$=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization
3. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
4. $V_{ADIN} = V_{SSA}$
5. $V_{ADIN} = V_{DDA}$
6. $I_{In}$ = leakage current (refer to DC characteristics)

### 5.4.2 Analog comparator (ACMP) electricals

**Table 13. Comparator electrical specifications**

| Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDA}$ | 2.7 | — | 5.5 | V |
| Supply current (Operation mode) | $I_{DDA}$ | — | 10 | 20 | μA |
| Analog input voltage | $V_{AIN}$ | $V_{SS}$ - 0.3 | — | $V_{DDA}$ | V |
| Analog input offset voltage | $V_{AIO}$ | — | — | 40 | mV |
| Analog comparator hysteresis (HYST=0) | $V_H$ | — | 15 | 20 | mV |
| Analog comparator hysteresis (HYST=1) | $V_H$ | — | 20 | 30 | mV |
| Supply current (Off mode) | $I_{DDAOFF}$ | — | 60 | — | nA |
| Propagation Delay | $t_D$ | — | 0.4 | 1 | μs |

## 5.5 Communication interfaces

### 5.5.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% $V_{DD}$ and 80% $V_{DD}$, unless noted, and 25 pF load on all SPI pins. All timing assumes slew rate control is disabled and high-drive strength is enabled for SPI output pins.

**Table 14. SPI master mode timing**

| Num. | Symbol | Description | Min. | Max. | Unit | Comment |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | $f_{Bus}/2048$ | $f_{Bus}/2$ | Hz | $f_{Bus}$ is the bus clock |
| 2 | $t_{SPSCK}$ | SPSCK period | 2 x $t_{Bus}$ | 2048 x $t_{Bus}$ | ns | $t_{Bus} = 1/f_{Bus}$ |
| 3 | $t_{Lead}$ | Enable lead time | 1/2 | — | $t_{SPSCK}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1/2 | — | $t_{SPSCK}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{Bus} – 30$ | 1024 x $t_{Bus}$ | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 8 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 8 | — | ns | — |
| 8 | $t_v$ | Data valid (after SPSCK edge) | — | 25 | ns | — |
| 9 | $t_{HO}$ | Data hold time (outputs) | 20 | — | ns | — |

*Table continues on the next page...*

## Table 15. SPI slave mode timing

| Num. | Symbol | Description | Min. | Max. | Unit | Comment |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | 0 | $f_{Bus}/4$ | Hz | $f_{Bus}$ is the bus clock as defined in Control timing. |
| 2 | $t_{SPSCK}$ | SPSCK period | 4 x $t_{Bus}$ | — | ns | $t_{Bus} = 1/f_{Bus}$ |
| 3 | $t_{Lead}$ | Enable lead time | 1 | — | $t_{Bus}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1 | — | $t_{Bus}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{Bus}$ - 30 | — | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 15 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 25 | — | ns | — |
| 8 | $t_a$ | Slave access time | — | $t_{Bus}$ | ns | Time to data active from high-impedance state |
| 9 | $t_{dis}$ | Slave MISO disable time | — | $t_{Bus}$ | ns | Hold time to high-impedance state |
| 10 | $t_v$ | Data valid (after SPSCK edge) | — | 25 | ns | — |
| 11 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 12 | $t_{RI}$ | Rise time input | — | $t_{Bus}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 13 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

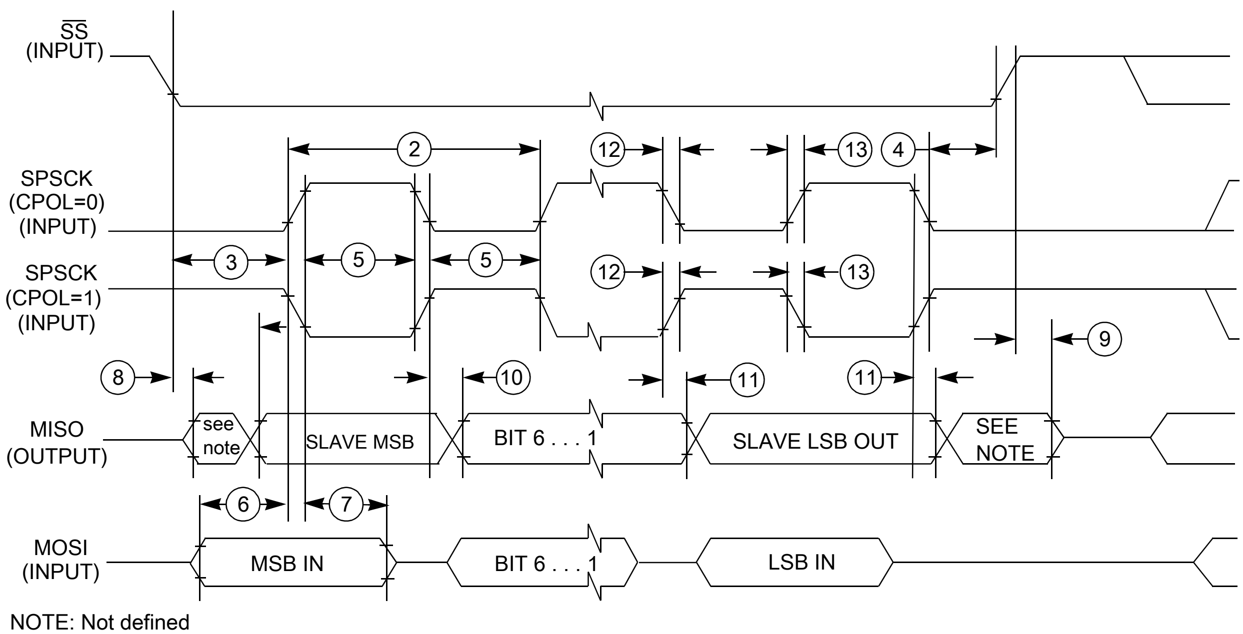


**Figure 19. SPI slave mode timing (CPHA = 0)**

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