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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	71
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9keaz64amlk

Table of Contents

Field	Description	Values
FFF	Program flash memory size	• 128 = 128 KB
M	Maskset revision	• A = 1st Fab version • B = Revision after 1st version
T	Temperature range (°C)	• C = –40 to 85 • V= –40 to 105 • M = –40 to 125
PP	Package identifier	• LH = 64 LQFP (10 mm x 10 mm) • LK = 80 LQFP (14 mm x 14 mm)
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

S9KEAZ128AMLK

3 Ratings

3.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

3.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4 General

4.1 Nonswitching electrical specifications

4.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 2. DC characteristics

Symbol	Descriptions			Min	Typical[1]	Max	Unit
—	Operating voltage		—	2.7	—	5.5	V
V_{OH}	Output high voltage	All I/O pins, except PTA2 and PTA3, standard-drive strength	5 V, I_{load} = –5 mA	V_{DD} – 0.8	—	—	V
			3 V, I_{load} = –2.5 mA	V_{DD} – 0.8	—	—	V
		High current drive pins, high-drive strength[2]	5 V, I_{load} = –20 mA	V_{DD} – 0.8	—	—	V
			3 V, I_{load} = –10 mA	V_{DD} – 0.8	—	—	V
I_{OHT}	Output high current	Max total I_{OH} for all ports	5 V	—	—	–100	mA
			3 V	—	—	–60	
V_{OL}	Output low voltage	All I/O pins, standard-drive strength	5 V, I_{load} = 5 mA	—	—	0.8	V
			3 V, I_{load} = 2.5 mA	—	—	0.8	V
		High current drive pins, high-drive strength[2]	5 V, I_{load} =20 mA	—	—	0.8	V
			3 V, I_{load} = 10 mA	—	—	0.8	V
I_{OLT}	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
			3 V	—	—	60	
V_{IH}	Input high voltage	All digital inputs	4.5≤V_{DD}<5.5 V	0.65 × V_{DD}	—	—	V
			2.7≤V_{DD}<4.5 V	0.70 × V_{DD}	—	—	
V_{IL}	Input low voltage	All digital inputs	4.5≤V_{DD}<5.5 V	—	—	0.35 × V_{DD}	V
			2.7≤V_{DD}<4.5 V	—	—	0.30 × V_{DD}	
V_{hys}	Input hysteresis	All digital inputs	—	0.06 × V_{DD}	—	—	mV
$\|I_{In}\|$	Input leakage current	Per pin (pins in high impedance input mode)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA

Table continues on the next page...

Table 2. DC characteristics (continued)

Symbol	Descriptions			Min	Typical[1]	Max	Unit
$\lvert I_{INTOT} \rvert$	Total leakage combined for all port pins	Pins in high impedance input mode	$V_{IN} = V_{DD}$ or V_{SS}	—	—	2	μA
R_{PU}	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	kΩ
R_{PU}[3]	Pullup resistors	PTA2 and PTA3 pins	—	30.0	—	60.0	kΩ
I_{IC}	DC injection current[4, 5, 6]	Single pin limit	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	-2	—	2	mA
		Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{In}	Input capacitance, all pins		—	—	—	7	pF
V_{RAM}	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 support high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}. PTA2 and PTA3 are true open drain I/O pins that are internally clamped to V_{SS}.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger value.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as when no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 3. LVD and POR specification

Symbol	Description		Min	Typ	Max	Unit
V_{POR}	POR re-arm voltage[1]		1.5	1.75	2.0	V
V_{LVDH}	Falling low-voltage detect threshold—high range (LVDV = 1)[2]		4.2	4.3	4.4	V
V_{LVW1H}	Falling low-voltage warning threshold— high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V_{LVW2H}		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V_{LVW3H}		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V_{LVW4H}		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V_{HYSH}	High range low-voltage detect/ warning hysteresis		—	100	—	mV

Table continues on the next page...

Table 3. LVD and POR specification (continued)

Symbol	Description		Min	Typ	Max	Unit
V_{LVDL}	Falling low-voltage detect threshold—low range (LVDV = 0)		2.56	2.61	2.66	V
V_{LVW1L}	Falling low-voltage warning threshold—low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V_{LVW2L}		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V_{LVW3L}		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V_{LVW4L}		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V_{HYSDL}	Low range low-voltage detect hysteresis		—	40	—	mV
V_{HYSWL}	Low range low-voltage warning hysteresis		—	80	—	mV
V_{BG}	Buffered bandgap output [3]		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. Rising thresholds are falling threshold + hysteresis.
3. voltage Factory trimmed at V_{DD} = 5.0 V, Temp = 125 °C

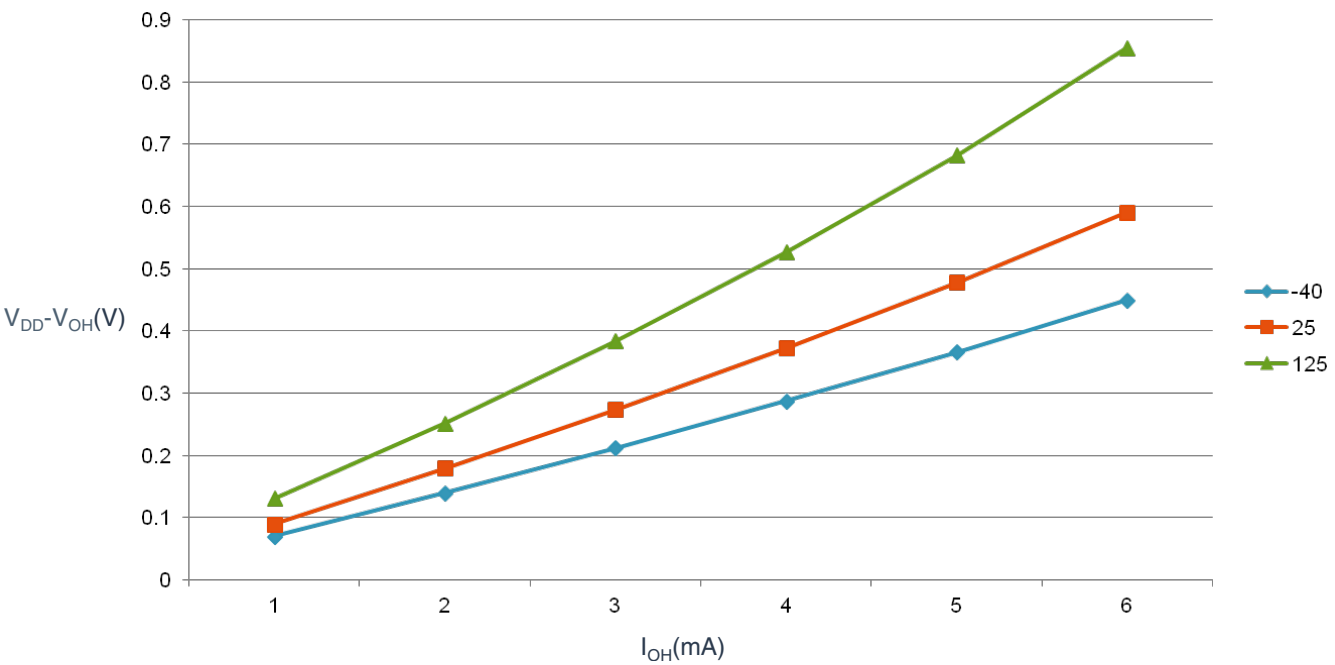

Figure 1. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 5 V)

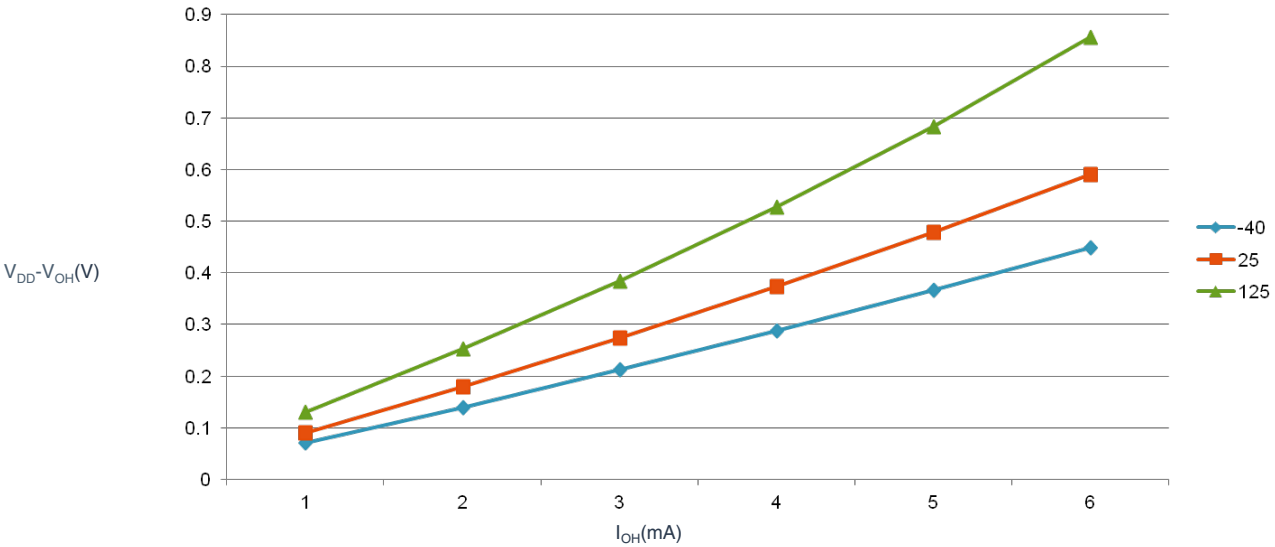

Figure 2. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 3 V)

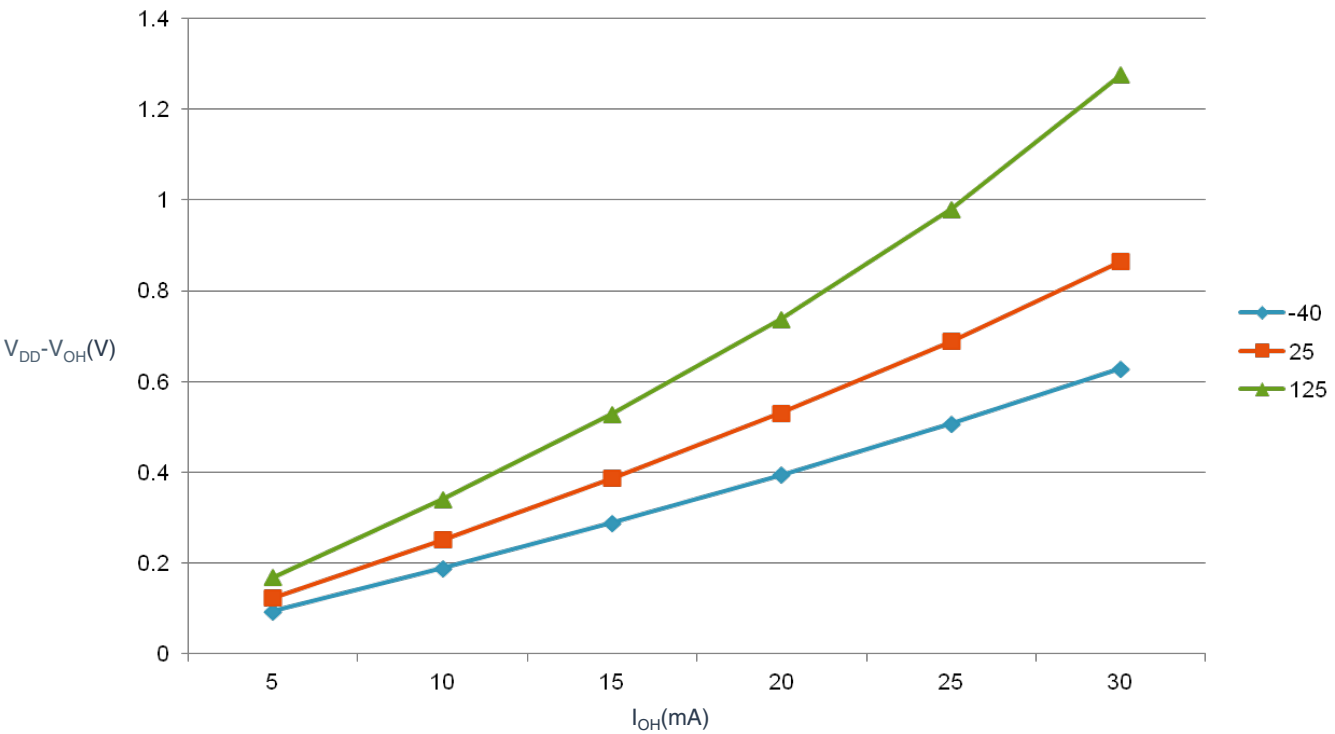

Figure 3. Typical V_{DD}-V_{OH} Vs. I_{OH} (high drive strength) (V_{DD} = 5 V)

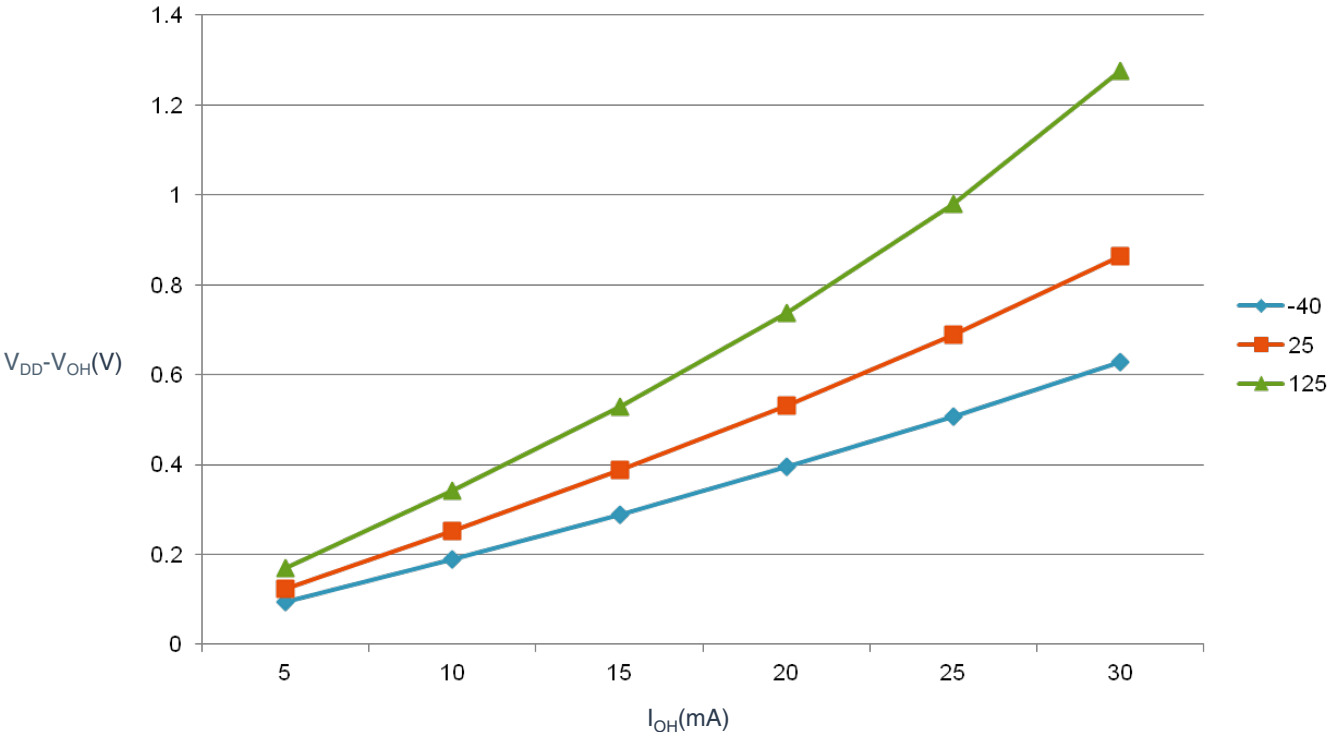

Figure 4. Typical V_{DD}-V_{OH} Vs. I_{OH} (high drive strength) (V_{DD} = 3 V)

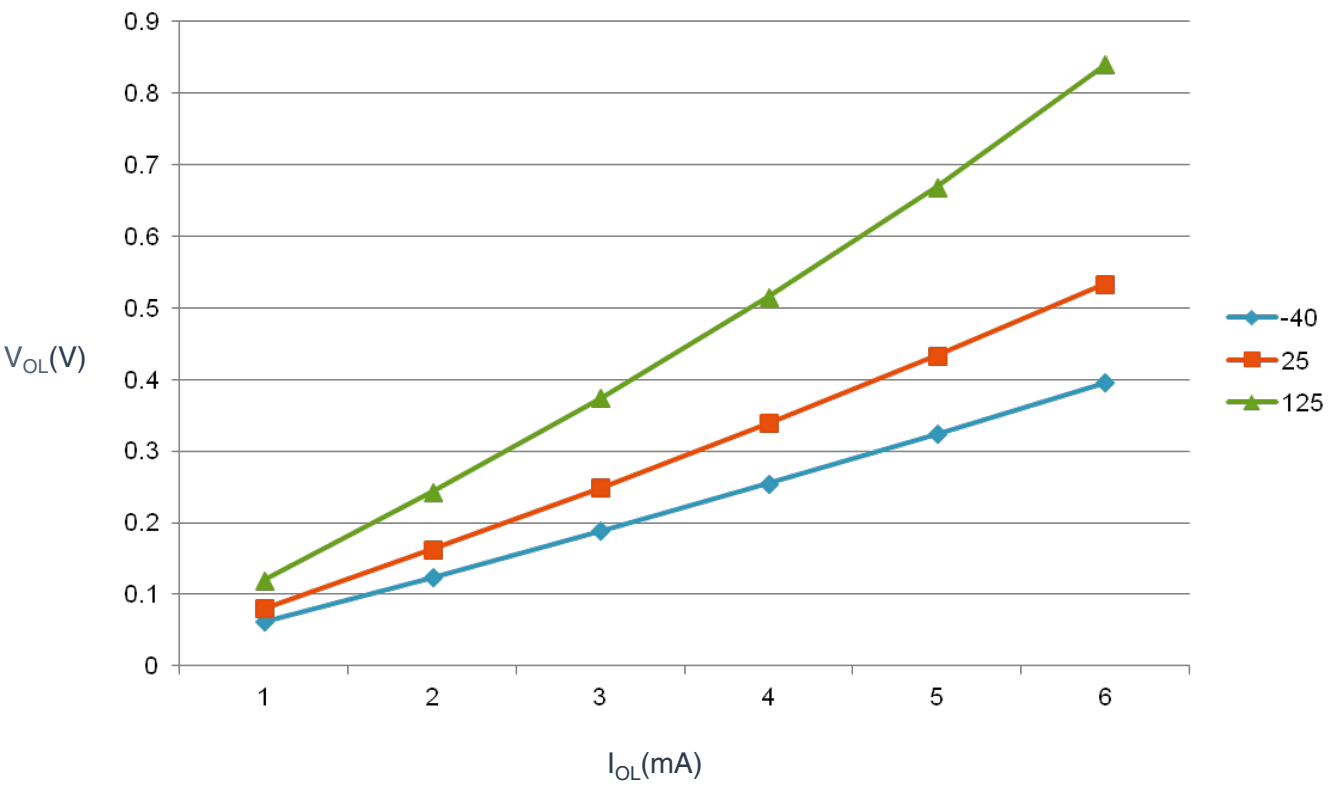

Figure 5. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 5 V)

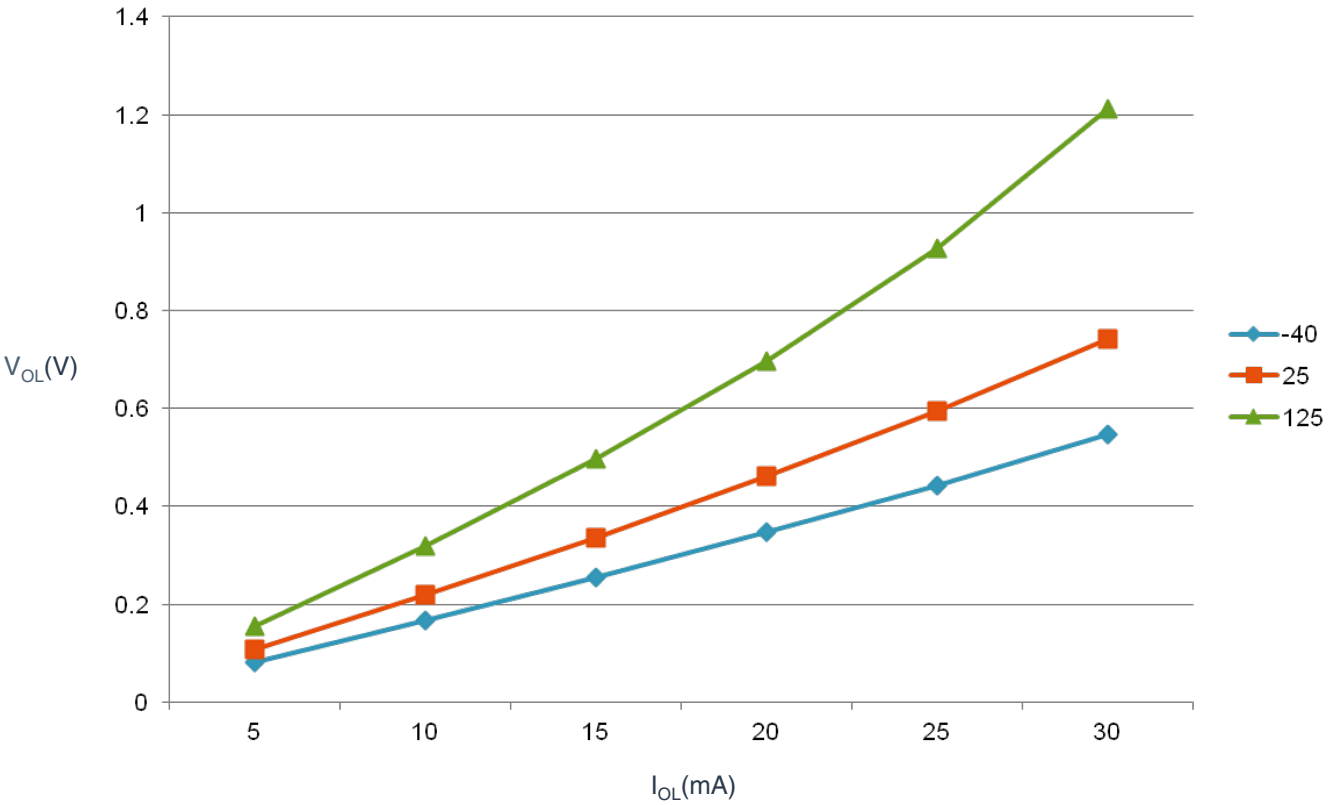

Figure 8. Typical V_{OL} Vs. I_{OL} (high drive strength) (V_{DD} = 3 V)

4.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
Run supply current FEI mode, all modules clocks enabled; run from flash	RI_{DD}	48/24 MHz	5	11.1	—	mA	-40 to 125 °C
		24/24 MHz		8	—		
		12/12 MHz		5	—		
		1/1 MHz		2.4	—		
		48/24 MHz	3	11	—		
		24/24 MHz		7.9	—		
		12/12 MHz		4.9	—		
		1/1 MHz		2.3	—		
Run supply current FEI mode, all modules clocks disabled and gated; run from flash	RI_{DD}	48/24 MHz	5	7.8	—	mA	-40 to 125 °C
		24/24 MHz		5.5	—		
		12/12 MHz		3.8	—		
		1/1 MHz		2.3	—		

Table continues on the next page...

Table 4. Supply current characteristics (continued)

Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
		48/24 MHz	3	7.7	—		
		24/24 MHz		5.4	—		
		12/12 MHz		3.7	—		
		1/1 MHz		2.2	—		
Run supply current FBE mode, all modules clocks enabled; run from RAM	RI_{DD}	48/24 MHz	5	14.7	—	mA	-40 to 125 °C
		24/24 MHz		9.8	14.9[2]		
		12/12 MHz		6	—		
		1/1 MHz		2.4	—		
		48/24 MHz	3	14.6	—		
		24/24 MHz		9.6	12.8[2]		
		12/12 MHz		5.9	—		
		1/1 MHz		2.3	—		
Run supply current FBE mode, all modules clocks disabled and gated; run from RAM	RI_{DD}	48/24 MHz	5	11.4	—	mA	-40 to 125 °C
		24/24 MHz		7.7	12.5[2]		
		12/12 MHz		4.7	—		
		1/1 MHz		2.3	—		
		48/24 MHz	3	11.3	—		
		24/24 MHz		7.6	9.5[2]		
		12/12 MHz		4.6	—		
		1/1 MHz		2.2	—		
Wait mode current FEI mode, all modules clocks enabled	WI_{DD}	48/24 MHz	5	8.4	—	mA	-40 to 125 °C
		24/24 MHz		6.5	7.2[2]		
		12/12 MHz		4.3	—		
		1/1 MHz		2.4	—		
		48/24 MHz	3	8.3	—		
		24/24 MHz		6.4	7.1[2]		
		12/12 MHz		4.2	—		
		1/1 MHz		2.3	—		
Stop mode supply current no clocks active (except 1 kHz LPO clock)[3]	SI_{DD}	—	5	2	170[2]	µA	-40 to 125 °C
		—	3	1.9	160[2]		-40 to 125 °C
ADC adder to Stop ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B	—	—	5	86	—	µA	-40 to 125 °C
			3	82	—		
ACMP adder to Stop	—	—	5	12	—	µA	-40 to 125 °C
			3	12	—		

Table continues on the next page...

Table 4. Supply current characteristics (continued)

Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
LVD adder to Stop[4]	—	—	5	130	—	µA	-40 to 125 °C
			3	125	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. The high current is observed at high temperature.
3. RTC adder cause <1 µA I_{DD} increase typically, RTC clock source is 1 kHz LPO clock.
4. LVD is periodically woken up from Stop by 5% duty cycle. The period is equal to or less than 2 ms.

4.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following Freescale applications notes, available on **freescale.com** for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

4.2 Switching specifications

4.2.1 Control timing

Table 5. Control timing

Num	Rating	Symbol	Min	Typical[1]	Max	Unit
1	System and core clock	f_{Sys}	DC	—	48	MHz
2	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	DC	—	24	MHz
3	Internal low power oscillator frequency	f_{LPO}	0.67	1.0	1.25	KHz
4	External reset pulse width[2]	t_{extrst}	1.5 × t_{cyc}	—	—	ns

Table continues on the next page...

Table 5. Control timing (continued)

Num	Rating		Symbol	Min	Typical[1]	Max	Unit
5	Reset low drive		t_{rstdrv}	34 × t_{cyc}	—	—	ns
6	IRQ pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
		Synchronous path[3]	t_{IHIL}	1.5 × t_{cyc}	—	—	ns
7	Keyboard interrupt pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
		Synchronous path	t_{IHIL}	1.5 × t_{cyc}	—	—	ns
8	Port rise and fall time - Normal drive strength (load = 50 pF)[4]	—	t_{Rise}	—	10.2	—	ns
			t_{Fall}	—	9.5	—	ns
	Port rise and fall time - high drive strength (load = 50 pF)[4]	—	t_{Rise}	—	5.4	—	ns
			t_{Fall}	—	4.6	—	ns

1. Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a $\overline{\text{RESET}}$ pin request.
3. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
4. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range -40 °C to 125 °C.

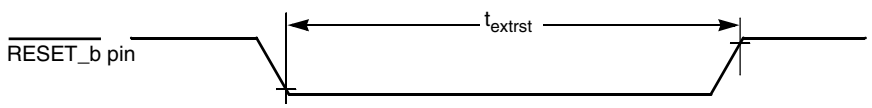

Figure 9. Reset timing

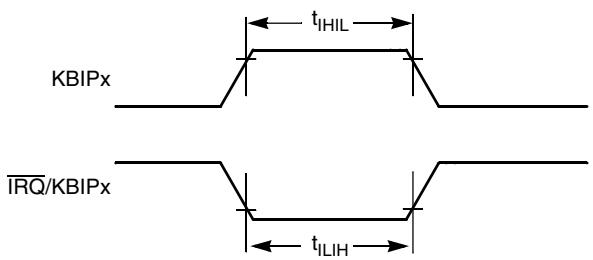

Figure 10. KBIPx timing

4.2.2 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 6. FTM input timing

Function	Symbol	Min	Max	Unit
Timer clock frequency	f_{Timer}	f_{Bus}	f_{Sys}	Hz
External clock frequency	f_{TCLK}	0	f_{Timer}/4	Hz

Table continues on the next page...

Table 6. FTM input timing (continued)

Function	Symbol	Min	Max	Unit
External clock period	t_{TCLK}	4	—	t_{cyc}
External clock high time	t_{clkh}	1.5	—	t_{cyc}
External clock low time	t_{clkl}	1.5	—	t_{cyc}
Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

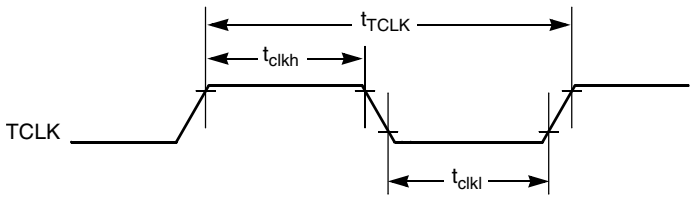

Figure 11. Timer external clock

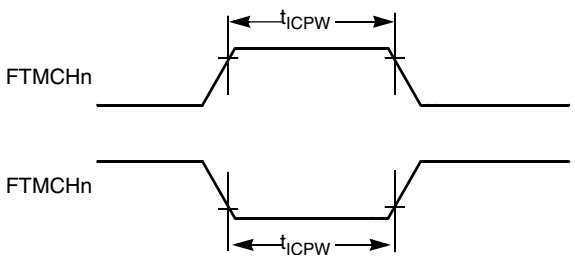

Figure 12. Timer input capture pulse

4.3 Thermal specifications

4.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for an known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

5 Peripheral operating requirements and behaviors

5.1 Core modules

5.1.1 SWD electricals

Table 8. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	24	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	3	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	35	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

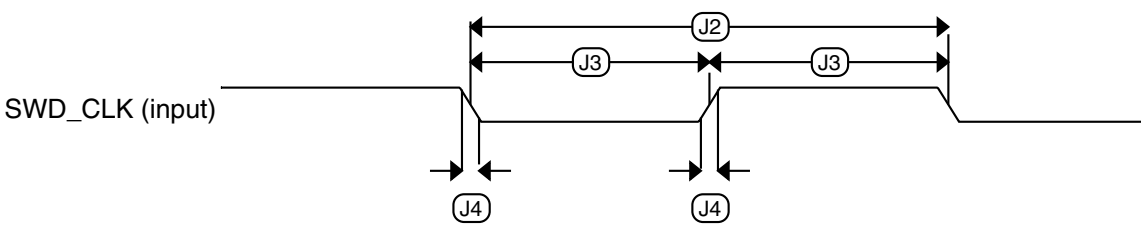

Figure 13. Serial wire clock input timing

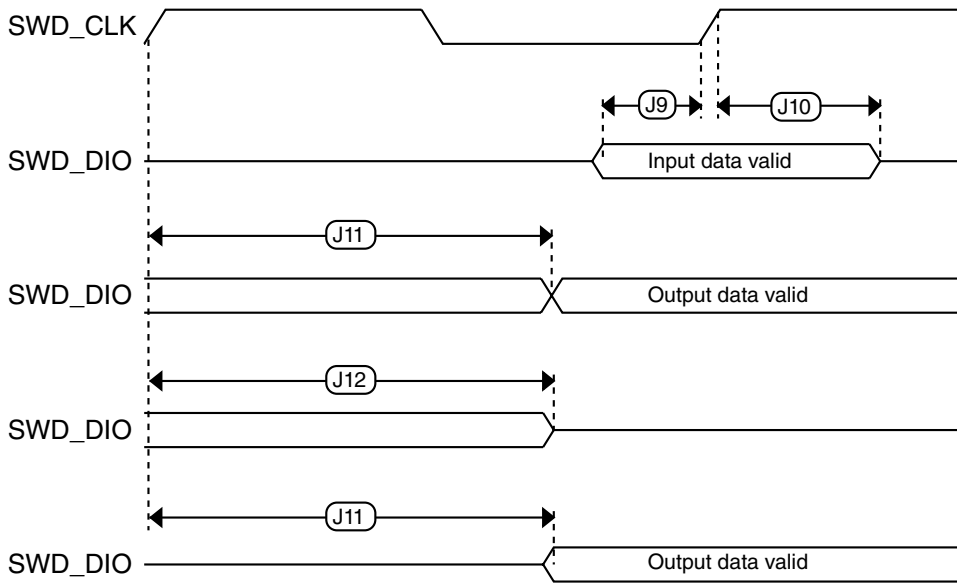

Figure 14. Serial wire data timing

5.2 External oscillator (OSC) and ICS characteristics

Table 9. OSC and ICS specifications (temperature range = -40 to 125 °C ambient)

Num	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	Crystal or resonator frequency	Low range (RANGE = 0)	f_{lo}	31.25	32.768	39.0625	kHz
		High range (RANGE = 1)	f_{hi}	4	—	24	MHz
2	Load capacitors		C1, C2	See Note[2]			
3	Feedback resistor	Low Frequency, Low-Power Mode[3]	R_F	—	—	—	MΩ
		Low Frequency, High-Gain Mode		—	10	—	MΩ
		High Frequency, Low-Power Mode		—	1	—	MΩ
		High Frequency, High-Gain Mode		—	1	—	MΩ
4	Series resistor - Low Frequency	Low-Power Mode [3]	R_S	—	0	—	kΩ
		High-Gain Mode		—	200	—	kΩ
5	Series resistor - High Frequency	Low-Power Mode[3]	R_S	—	0	—	kΩ
	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
		8 MHz		—	0	—	kΩ

Table continues on the next page...

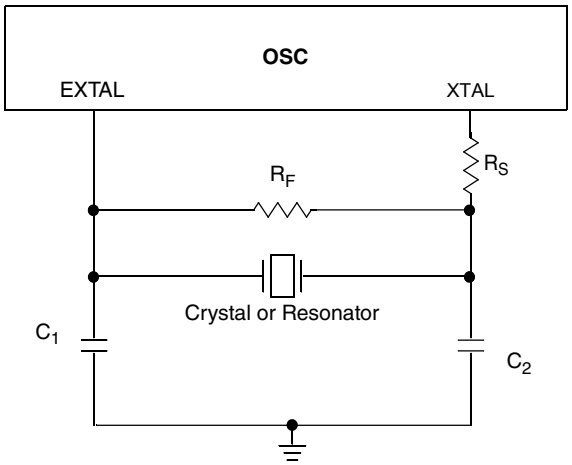

Figure 15. Typical crystal or resonator circuit

5.3 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash memories.

Table 10. Flash characteristics

Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
Supply voltage for program/erase –40 °C to 125 °C	$V_{prog/erase}$	2.7	—	5.5	V
Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
NVM Bus frequency	f_{NVMBUS}	1	—	24	MHz
NVM Operating frequency	f_{NVMOP}	0.8	1	1.05	MHz
Erase Verify All Blocks	t_{VFYALL}	—	—	2605	t_{cyc}
Erase Verify Flash Block	t_{RD1BLK}	—	—	2579	t_{cyc}
Erase Verify Flash Section	t_{RD1SEC}	—	—	485	t_{cyc}
Read Once	t_{RDONCE}	—	—	464	t_{cyc}
Program Flash (2 word)	t_{PGM2}	0.12	0.13	0.31	ms
Program Flash (4 word)	t_{PGM4}	0.21	0.21	0.49	ms
Program Once	$t_{PGMONCE}$	0.20	0.21	0.21	ms
Erase All Blocks	t_{ERSALL}	95.42	100.18	100.30	ms
Erase Flash Block	t_{ERSBLK}	95.42	100.18	100.30	ms
Erase Flash Sector	t_{ERSPG}	19.10	20.05	20.09	ms
Unsecure Flash	t_{UNSECU}	95.42	100.19	100.31	ms
Verify Backdoor Access Key	t_{VFYKEY}	—	—	482	t_{cyc}
Set User Margin Level	t_{MLOADU}	—	—	415	t_{cyc}
FLASH Program/erase endurance T_L to T_H = -40 °C to 125 °C	n_{FLPE}	10 k	100 k	—	Cycles

Table continues on the next page...

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

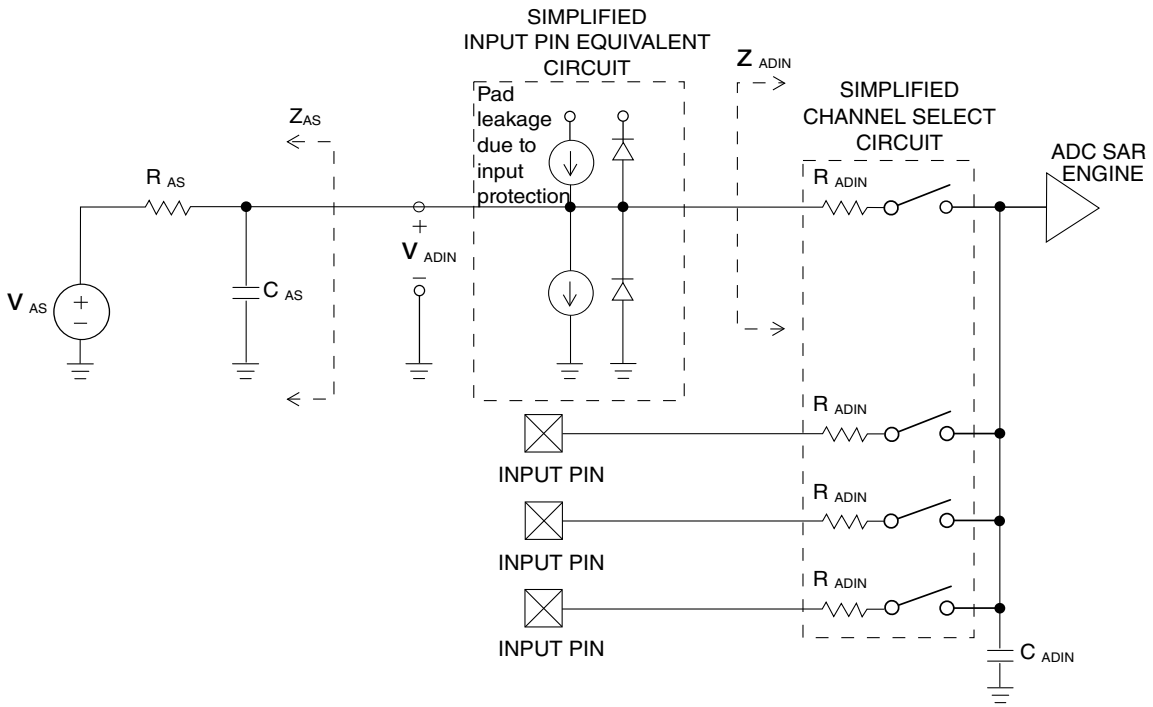

Figure 16. ADC input impedance equivalency diagram

Table 12. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDA}	—	133	—	µA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		I_{DDA}	—	218	—	µA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDA}	—	327	—	µA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDA}	—	582	990	µA
Supply current	Stop, reset, module off	I_{DDA}	—	0.011	1	µA

Table continues on the next page...

Table 12. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit
ADC asynchronous clock source	High speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)		1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)		—	40	—	
Sample time	Short sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)		—	23.5	—	
Total unadjusted Error[2]	12-bit mode	E_{TUE}	—	±5.0	—	LSB[3]
	10-bit mode		—	±1.5	—	
	8-bit mode		—	±0.8	—	
Differential Non-Liniarity	12-bit mode	DNL	—	±1.5	—	LSB[3]
	10-bit mode		—	±0.4	—	
	8-bit mode		—	±0.15	—	
Integral Non-Linearity	12-bit mode	INL	—	±1.5	—	LSB[3]
	10-bit mode		—	±0.4	—	
	8-bit mode		—	±0.15	—	
Zero-scale error[4]	12-bit mode	E_{ZS}	—	±1.0	—	LSB[3]
	10-bit mode		—	±0.2	—	
	8-bit mode		—	±0.35	—	
Full-scale error[5]	12-bit mode	E_{FS}	—	±2.5	—	LSB[3]
	10-bit mode		—	±0.3	—	
	8-bit mode		—	±0.25	—	
Quantization error	≤12 bit modes	E_Q	—	—	±0.5	LSB[3]
Input leakage error[6]	all modes	E_{IL}	I_{In} x R_{AS}			mV
Temp sensor slope	-40 °C–25 °C	m	—	3.266	—	mV/°C
	25 °C–125 °C		—	3.638	—	
Temp sensor voltage	25 °C	V_{TEMP25}	—	1.396	—	V

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization
3. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
4. $V_{ADIN} = V_{SSA}$
5. $V_{ADIN} = V_{DDA}$
6. I_{In} = leakage current (refer to DC characteristics)

5.4.2 Analog comparator (ACMP) electricals

Table 13. Comparator electrical specifications

Characteristic	Symbol	Min	Typical	Max	Unit
Supply voltage	V_{DDA}	2.7	—	5.5	V
Supply current (Operation mode)	I_{DDA}	—	10	20	μA
Analog input voltage	V_{AIN}	V_{SS} - 0.3	—	V_{DDA}	V
Analog input offset voltage	V_{AIO}	—	—	40	mV
Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
Propagation Delay	t_D	—	0.4	1	μs

5.5 Communication interfaces

5.5.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% V_{DD} and 80% V_{DD}, unless noted, and 25 pF load on all SPI pins. All timing assumes slew rate control is disabled and high-drive strength is enabled for SPI output pins.

Table 14. SPI master mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	$f_{Bus}/2048$	$f_{Bus}/2$	Hz	f_{Bus} is the bus clock
2	t_{SPSCK}	SPSCK period	2 x t_{Bus}	2048 x t_{Bus}	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{Bus} – 30	1024 x t_{Bus}	ns	—
6	t_{SU}	Data setup time (inputs)	8	—	ns	—
7	t_{HI}	Data hold time (inputs)	8	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	25	ns	—
9	t_{HO}	Data hold time (outputs)	20	—	ns	—

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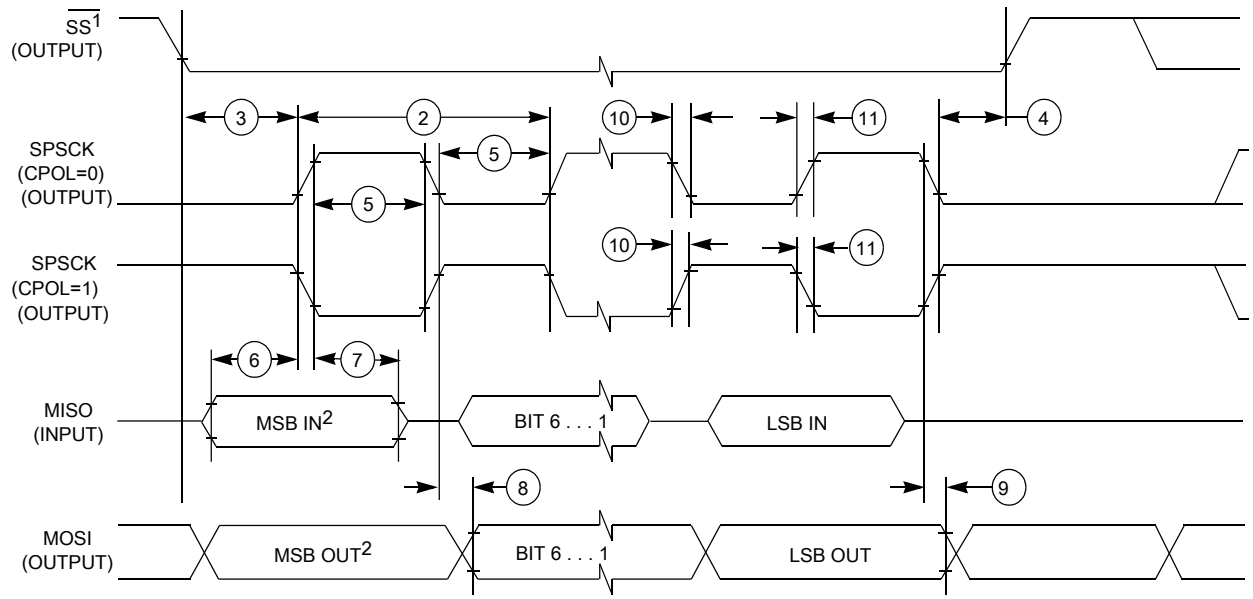
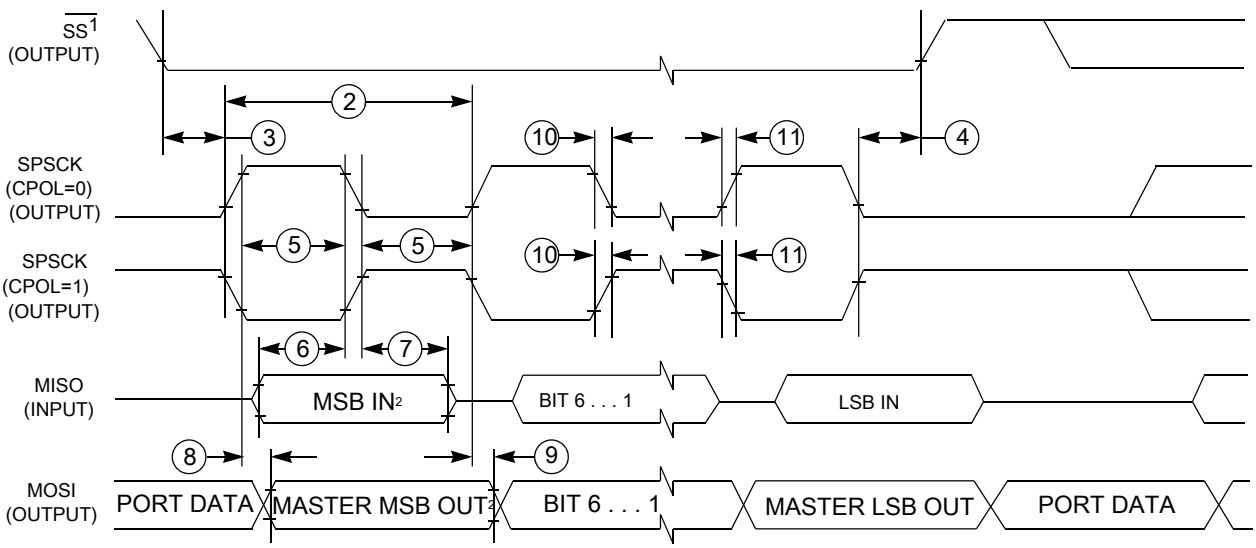
Table 14. SPI master mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
10	t_{RI}	Rise time input	—	t_{Bus} – 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. SPI master mode timing (CPHA=0)



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

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