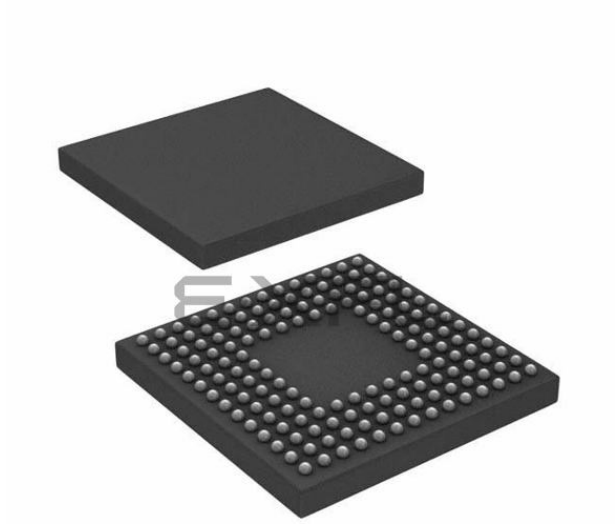

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	400MHz
Non-Volatile Memory	ROM (1kB)
On-Chip RAM	52kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LFBGA, CSPBGA
Supplier Device Package	160-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf531wbbcz406

GENERAL DESCRIPTION

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are members of the Blackfin® family of products, incorporating the Analog Devices, Inc./Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single instruction, multiple data (SIMD) multimedia capabilities into a single instruction set architecture.

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are completely code and pin-compatible, differing only with respect to their performance and on-chip memory. Specific performance and memory configurations are shown in Table 1.

Table 1. Processor Comparison

Features		ADSP-BF531	ADSP-BF532	ADSP-BF533
SPORTs		2	2	2
UART		1	1	1
SPI		1	1	1
GP Timers		3	3	3
Watchdog Timers		1	1	1
RTC		1	1	1
Parallel Peripheral Interface		1	1	1
GPIOs		16	16	16
Memory Configuration	L1 Instruction SRAM/Cache	16K bytes	16K bytes	16K bytes
	L1 Instruction SRAM	16K bytes	32K bytes	64K bytes
	L1 Data SRAM/Cache	16K bytes	32K bytes	32K bytes
	L1 Data SRAM			32K bytes
	L1 Scratchpad	4K bytes	4K bytes	4K bytes
	L3 Boot ROM	1K bytes	1K bytes	1K bytes
Maximum Speed Grade		400 MHz	400 MHz	600 MHz
Package Options: CSP_BGA Plastic BGA LQFP		 160-Ball 169-Ball 176-Lead	 160-Ball 169-Ball 176-Lead	 160-Ball 169-Ball 176-Lead

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

PORTABLE LOW POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. Blackfin processors are designed in a low power and low voltage design methodology and feature dynamic power management—the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. Varying the voltage and frequency can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This translates into longer battery life for portable appliances.

SYSTEM INTEGRATION

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are highly integrated system-on-a-chip solutions for the next generation of digital communication and consumer multimedia applications. By combining industry-standard interfaces with a high performance signal processing core, users can develop cost-effective solutions quickly without the need for costly external components. The system peripherals include a UART port, an SPI port, two serial ports (SPORTs), four general-purpose timers (three with PWM capability), a real-time clock, a watchdog timer, and a parallel peripheral interface.

PROCESSOR PERIPHERALS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors contain a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the functional block diagram in Figure 1 on Page 1). The general-purpose peripherals include functions such as UART, timers with PWM (pulse-width modulation) and pulse measurement capability, general-purpose I/O pins, a real-time clock, and a watchdog timer. This set of functions satisfies a wide variety of typical system support needs and is augmented by the system expansion capabilities of the part. In addition to these general-purpose peripherals, the processors contain high speed serial and parallel ports for interfacing to a variety of audio, video, and modem codec functions; an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources; and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

All of the peripherals, except for general-purpose I/O, real-time clock, and timers, are supported by a flexible DMA structure. There is also a separate memory DMA channel dedicated to data transfers between the processor's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses running at up to 133 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The processors include an on-chip voltage regulator in support of the processor's dynamic power management capability. The voltage regulator provides a range of core voltage levels from V_{DDEXT}. The voltage regulator can be bypassed at the user's discretion.

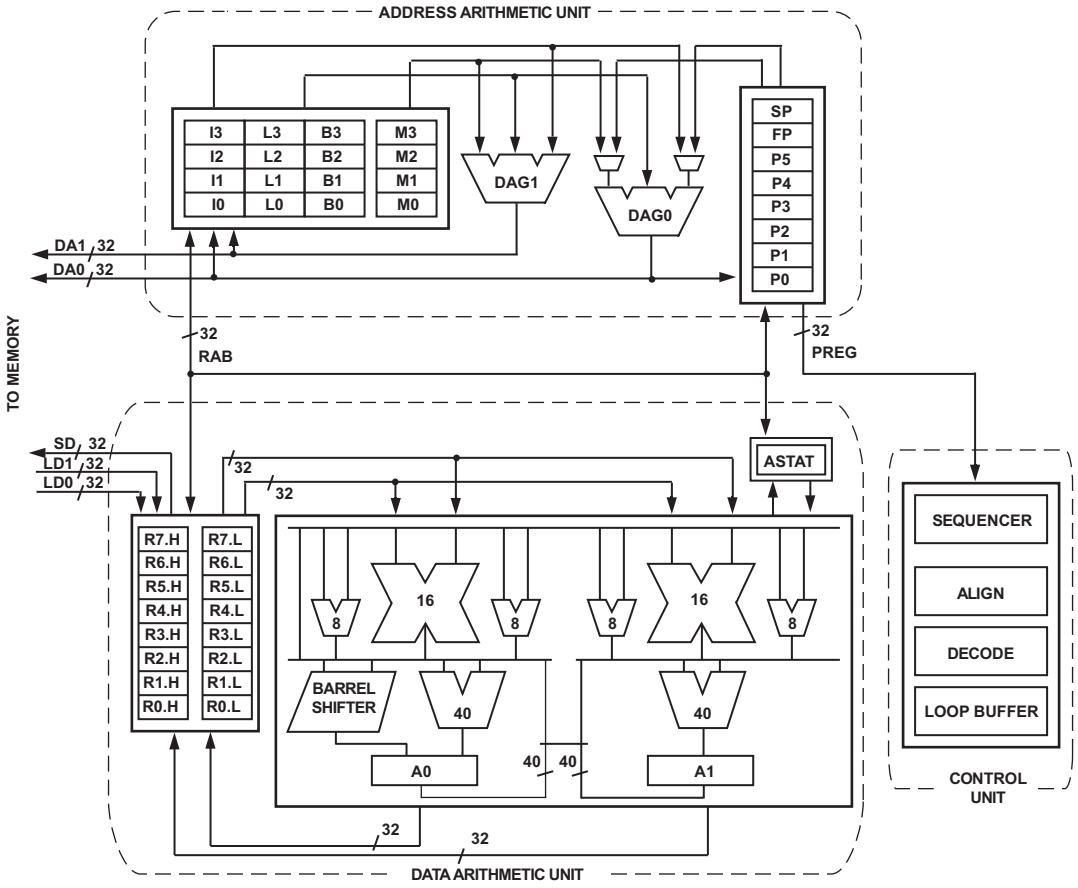


Figure 2. Blackfin Processor Core

The second on-chip memory block is the L1 data memory, consisting of one or two banks of up to 32K bytes. The memory banks are configurable, offering both cache and SRAM functionality. This memory block is accessed at full processor speed.

The third memory block is a 4K byte scratchpad SRAM, which runs at the same speed as the L1 memories, but is only accessible as data SRAM and cannot be configured as cache memory.

External (Off-Chip) Memory

External memory is accessed via the external bus interface unit (EBIU). This 16-bit interface provides a glueless connection to a bank of synchronous DRAM (SDRAM) as well as up to four banks of asynchronous memory devices including flash, EPROM, ROM, SRAM, and memory mapped I/O devices.

The PC133-compliant SDRAM controller can be programmed to interface to up to 128M bytes of SDRAM. The SDRAM controller allows one row to be open for each internal SDRAM bank, for up to four internal SDRAM banks, improving overall system performance.

The asynchronous memory controller can be programmed to control up to four banks of devices with very flexible timing parameters for a wide variety of devices. Each bank occupies a 1M byte segment regardless of the size of the devices used, so that these banks are only contiguous if each is fully populated with 1M byte of memory.

I/O Memory Space

Blackfin processors do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one containing the control MMRs for all core functions, and the other containing the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors contain a small boot kernel, which configures the appropriate peripheral for booting. If the processors are configured to boot from boot ROM memory space, the processor starts executing from the on-chip boot ROM. For more information, see Booting Modes on Page 14.

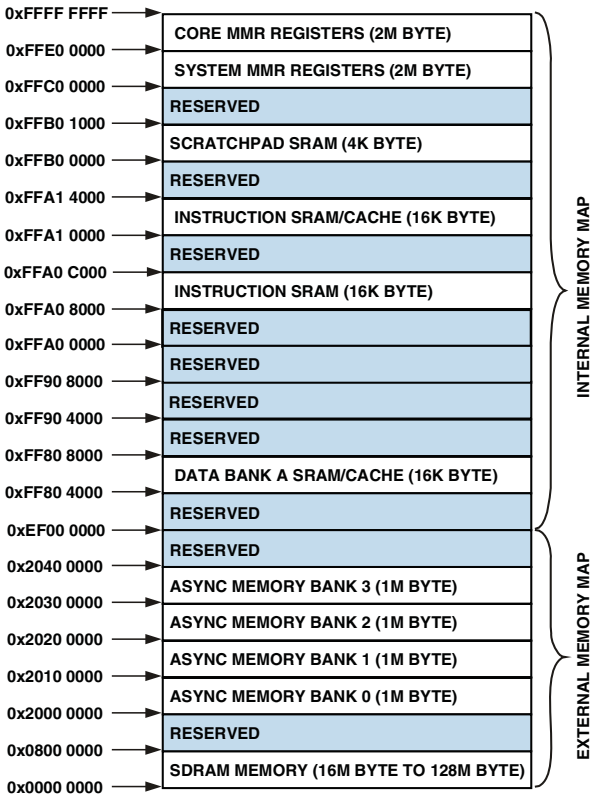


Figure 3. ADSP-BF531 Internal/External Memory Map

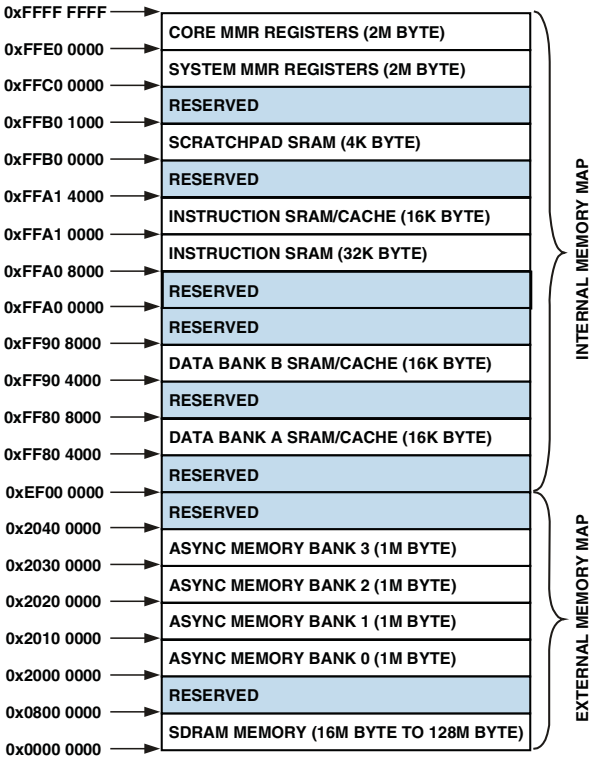


Figure 4. ADSP-BF532 Internal/External Memory Map

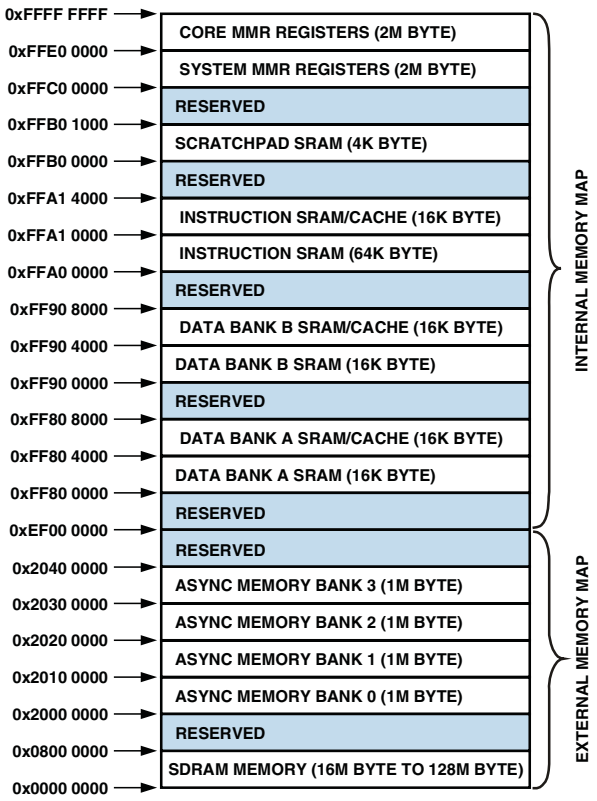


Figure 5. ADSP-BF533 Internal/External Memory Map

Event Handling

The event controller on the processors handle all asynchronous and synchronous events to the processor. The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provide event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher priority event takes precedence over servicing of a lower priority event. The controller provides support for five different types of events:

- Emulation – An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- Reset – This event resets the processor.
- Nonmaskable Interrupt (NMI) – The NMI event can be generated by the software watchdog timer or by the NMI input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- Exceptions – Events that occur synchronously to program flow (i.e., the exception is taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts – Events that occur asynchronously to program flow. They are caused by input pins, timers, and other peripherals, as well as by an explicit software instruction.

t_{NOM} is the duration running at $f_{CCLKNOM}$

t_{RED} is the duration running at $f_{CCLKRED}$

The percent power savings is calculated as:

$$\%\ power\ savings\ =\ (1 - power\ savings\ factor) \times 100\%$$

VOLTAGE REGULATION

The Blackfin processor provides an on-chip voltage regulator that can generate appropriate V_{DDINT} voltage levels from the V_{DDEXT} supply. See Operating Conditions on Page 20 for regulator tolerances and acceptable V_{DDEXT} ranges for specific models.

Figure 7 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power (V_{DDEXT}) supplied. While in the hibernate state, I/O power is still being applied, eliminating the need for external buffers. The voltage regulator can be activated from this power-down state either through an RTC wakeup or by asserting $\overline{\text{RESET}}$, both of which initiate a boot sequence. The regulator can also be disabled and bypassed at the user's discretion.

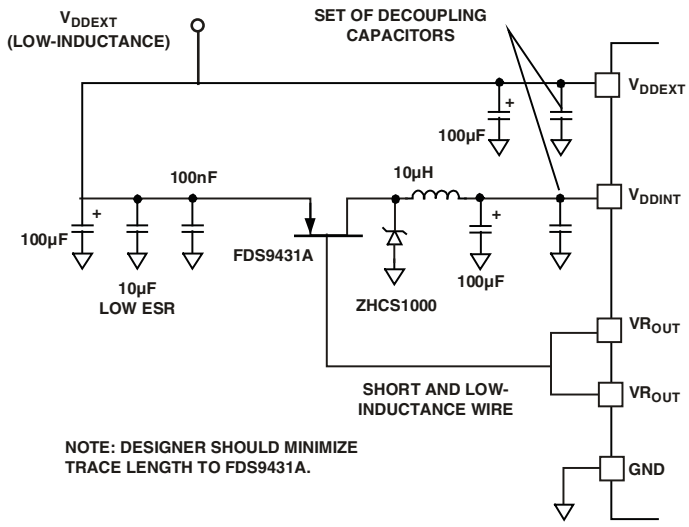


Figure 7. Voltage Regulator Circuit

Voltage Regulator Layout Guidelines

Regulator external component placement, board routing, and bypass capacitors all have a significant effect on noise injected into the other analog circuits on-chip. The VROUT1–0 traces and voltage regulator external components should be considered as noise sources when doing board layout and should not be routed or placed near sensitive circuits or components on the board. All internal and I/O power supplies should be well bypassed with bypass capacitors placed as close to the processors as possible.

For further details on the on-chip voltage regulator and related board design guidelines, see the *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228)* applications note on the Analog Devices web site (www.analog.com)—use site search on "EE-228".

CLOCK SIGNALS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the processors include an on-chip oscillator circuit, an external crystal can be used. For fundamental frequency operation, use the circuit shown in Figure 8.

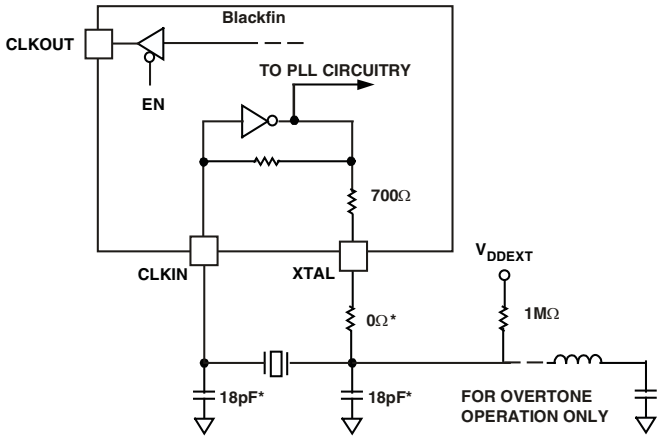


Figure 8. External Crystal Connections

A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor shown in Figure 8 fine tune the phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 8 are typical values only. The capacitor values are dependent upon the crystal manufacturer's load capacitance recommendations and the physical PCB layout. The resistor value depends on the drive level specified by the crystal manufacturer. System designs should verify the customized values based on careful investigation on multiple devices over the allowed temperature range.

A third-overtone crystal can be used at frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 8.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *“Analog Devices JTAG Emulation Technical Reference”* (EE-68) on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started With Blackfin Processors*
- *ADSP-BF533 Blackfin Processor Hardware Reference*
- *Blackfin Processor Programming Reference*
- *ADSP-BF531/ADSP-BF532/ADSP-BF533 Blackfin Processor Anomaly List*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 9. Pin Descriptions (Continued)

Pin Name	Type	Function	Driver Type[1]
Port F: GPIO/Parallel Peripheral Interface Port/SPI/Timers			
PF0/*SPISS*	I/O	GPIO/*SPI Slave Select Input*	C
PF1/*SPISEL1*/*TACLK*	I/O	GPIO/*SPI Slave Select Enable 1/Timer Alternate Clock Input*	C
PF2/*SPISEL2*	I/O	GPIO/*SPI Slave Select Enable 2*	C
PF3/*SPISEL3*/*PPI_FS3*	I/O	GPIO/*SPI Slave Select Enable 3/PPI Frame Sync 3*	C
PF4/*SPISEL4*/*PPI15*	I/O	GPIO/*SPI Slave Select Enable 4/PPI 15*	C
PF5/*SPISEL5*/*PPI14*	I/O	GPIO/*SPI Slave Select Enable 5/PPI 14*	C
PF6/*SPISEL6*/*PPI13*	I/O	GPIO/*SPI Slave Select Enable 6/PPI 13*	C
PF7/*SPISEL7*/*PPI12*	I/O	GPIO/*SPI Slave Select Enable 7/PPI 12*	C
PF8/*PPI11*	I/O	GPIO/*PPI 11*	C
PF9/*PPI10*	I/O	GPIO/*PPI 10*	C
PF10/*PPI9*	I/O	GPIO/*PPI 9*	C
PF11/*PPI8*	I/O	GPIO/*PPI 8*	C
PF12/*PPI7*	I/O	GPIO/*PPI 7*	C
PF13/*PPI6*	I/O	GPIO/*PPI 6*	C
PF14/*PPI5*	I/O	GPIO/*PPI 5*	C
PF15/*PPI4*	I/O	GPIO/*PPI 4*	C
JTAG Port			
TCK	I	JTAG Clock	
TDO	O	JTAG Serial Data Out	C
TDI	I	JTAG Serial Data In	
TMS	I	JTAG Mode Select	
$\overline{\text{TRST}}$	I	JTAG Reset (This pin should be pulled low if JTAG is not used.)	
$\overline{\text{EMU}}$	O	Emulation Output	C
SPI Port			
MOSI	I/O	Master Out Slave In	C
MISO	I/O	Master In Slave Out (This pin should be pulled high through a 4.7 kΩ resistor if booting via the SPI port.)	C
SCK	I/O	SPI Clock	D
Serial Ports			
RSCLK0	I/O	SPORT0 Receive Serial Clock	D
RFS0	I/O	SPORT0 Receive Frame Sync	C
DR0PRI	I	SPORT0 Receive Data Primary	
DR0SEC	I	SPORT0 Receive Data Secondary	
TSCLK0	I/O	SPORT0 Transmit Serial Clock	D
TFS0	I/O	SPORT0 Transmit Frame Sync	C
DT0PRI	O	SPORT0 Transmit Data Primary	C
DT0SEC	O	SPORT0 Transmit Data Secondary	C
RSCLK1	I/O	SPORT1 Receive Serial Clock	D

[5] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{TRST}$).
[6] Absolute value.
[7] Applies to three-statable pins.
[8] Applies to all signal pins.
[9] Guaranteed, but not tested.
[10] See the *ADSP-BF533 Blackfin Processor Hardware Reference Manual* for definitions of sleep, deep sleep, and hibernate operating modes.
[11] See Table 16 for the list of I_{DDINT} power vectors covered by various Activity Scaling Factors (ASF).

System designers should refer to *Estimating Power for the ADSP-BF531/BF532/BF533 Blackfin Processors (EE-229)*, which provides detailed information for optimizing designs for lowest power. All topics discussed in this section are described in detail in EE-229. Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 22 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 14 or Table 15), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 17).

The dynamic component is also subject to an Activity Scaling Factor (ASF) which represents application code running on the processor (Table 16).

Table 14. Static Current–500 MHz, 533 MHz, and 600 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})[2]														
T_J (°C)[2]	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V	1.45 V
–45	4.3	5.3	5.9	7.0	8.2	9.8	11.2	13.0	15.2	17.7	20.2	21.6	25.5	30.1	32.0
0	18.8	21.3	24.1	27.8	31.6	35.6	40.1	45.3	51.4	58.1	65.0	68.5	78.4	89.8	94.3
25	35.3	39.9	45.0	50.9	57.3	64.4	72.9	80.9	90.3	101.4	112.1	118.0	133.7	151.6	158.7
40	52.3	58.5	65.1	73.3	81.3	90.9	101.2	112.5	125.5	138.7	154.4	160.6	180.6	203.1	212.0
55	73.6	82.5	92.0	102.7	114.4	126.3	141.2	155.7	172.7	191.1	212.1	220.8	247.6	277.7	289.5
70	100.8	112.5	124.5	137.4	152.6	168.4	186.5	205.4	227.0	250.3	276.2	287.1	320.4	357.4	371.9
85	133.3	148.5	164.2	180.5	198.8	219.0	241.0	264.5	290.6	319.7	350.2	364.6	404.9	449.7	467.2
100	178.3	196.3	216.0	237.6	259.9	284.6	311.9	342.0	373.1	408.0	446.1	462.6	511.1	564.7	585.6
115	223.3	245.9	270.2	295.7	323.5	353.3	386.1	421.1	460.1	500.9	545.0	566.5	624.3	688.1	712.8
125	278.5	305.8	334.1	364.3	397.4	432.4	470.6	509.3	553.4	600.6	652.1	676.5	742.1	814.1	841.9

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 20.

Table 15. Static Current–400 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})[2]											
T_J (°C)[2]	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V
–45	0.9	1.1	1.3	1.5	1.8	2.2	2.6	3.1	3.8	4.4	5.0	5.4
0	3.3	3.7	4.2	4.8	5.5	6.3	7.2	8.1	8.9	10.1	11.2	11.9
25	7.5	8.4	9.4	10.0	11.2	12.6	14.1	15.5	17.2	19.0	21.2	21.9
40	12.0	13.1	14.3	15.9	17.4	19.4	21.5	23.5	25.8	28.1	30.8	32.0
55	18.3	20.0	21.9	23.6	26.0	28.2	30.8	33.7	36.8	39.8	43.4	45.0
70	27.7	30.3	32.6	35.3	38.2	41.7	45.2	49.0	52.8	57.6	62.4	64.2
85	38.2	41.7	44.9	48.6	52.7	57.3	61.7	66.7	72.0	77.5	83.9	86.5
100	54.1	58.1	63.2	67.8	73.2	78.8	84.9	91.5	98.4	106.0	113.8	117.2
115	73.9	80.0	86.3	91.9	99.1	106.6	114.1	122.4	131.1	140.9	151.1	155.5
125	98.7	106.3	113.8	122.1	130.8	140.2	149.7	160.4	171.9	183.8	197.0	202.4

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 20.

PACKAGE INFORMATION

The information presented in Figure 10 and Table 20 provides details about the package branding for the Blackfin processors. For a complete listing of product availability, see the Ordering Guide on Page 63.

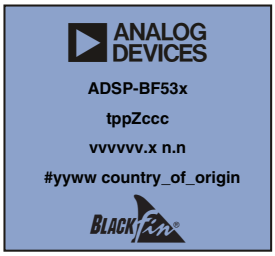


Figure 10. Product Information on Package

Table 20. Package Brand Information[1]

Brand Key	Field Description
ADSP-BF53x	Either ADSP-BF531, ADSP-BF532, or ADSP-BF533
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

[1] Non Automotive only. For branding information specific to Automotive products, contact Analog Devices Inc.

External Port Bus Request and Grant Cycle Timing

Table 26 and Figure 16 describe external port bus request and bus grant operations.

Table 26. External Port Bus Request and Grant Cycle Timing

Parameter	V_{DDEXT} = 1.8 V LQFP/PBGA Packages		V_{DDEXT} = 1.8 V CSP_BGA Package		V_{DDEXT} = 2.5 V/3.3 V All Packages		Unit
	Min	Max	Min	Max	Min	Max	
Timing Requirements							
t_{BS} $\overline{BR}$ Asserted to CLKOUT High Setup	4.6		4.6		4.6		ns
t_{BH} CLKOUT High to $\overline{BR}$ Deasserted Hold Time	1.0		1.0		0.0		ns
Switching Characteristics							
t_{SD} CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Disable		4.5		4.5		4.5	ns
t_{SE} CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Enable		4.5		4.5		4.5	ns
t_{DBG} CLKOUT High to $\overline{BG}$ High Setup		6.0		5.5		3.6	ns
t_{EBG} CLKOUT High to $\overline{BG}$ Deasserted Hold Time		6.0		4.6		3.6	ns
t_{DBH} CLKOUT High to $\overline{BGH}$ High Setup		6.0		5.5		3.6	ns
t_{EBH} CLKOUT High to $\overline{BGH}$ Deasserted Hold Time		6.0		4.6		3.6	ns

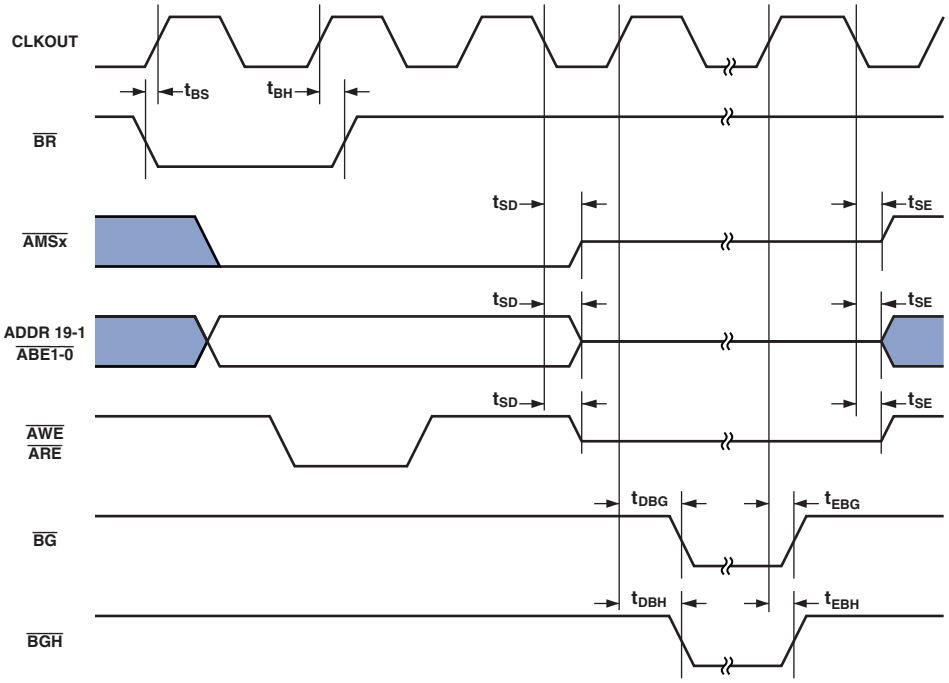


Figure 16. External Port Bus Request and Grant Cycle Timing

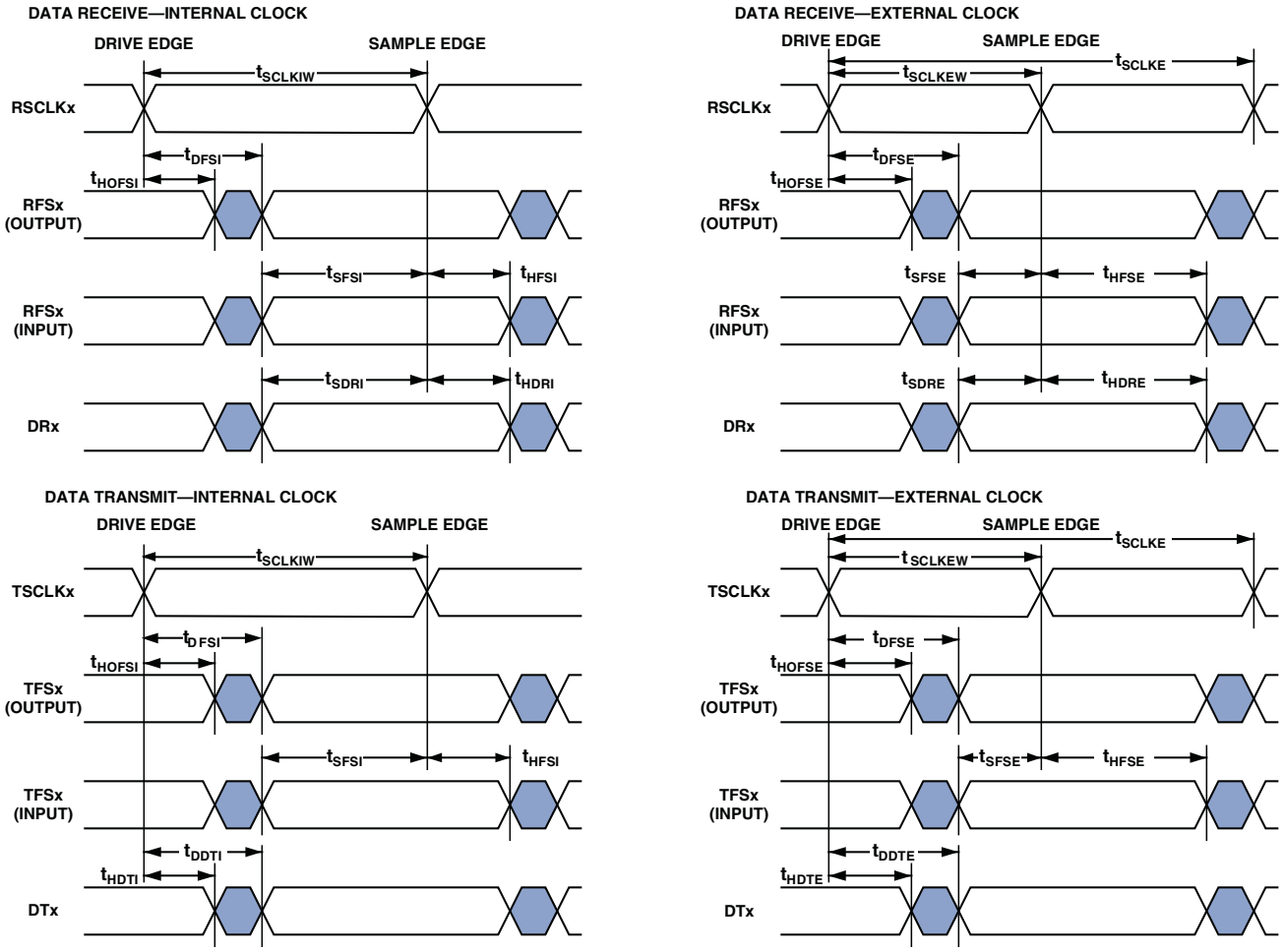


Figure 23. Serial Ports

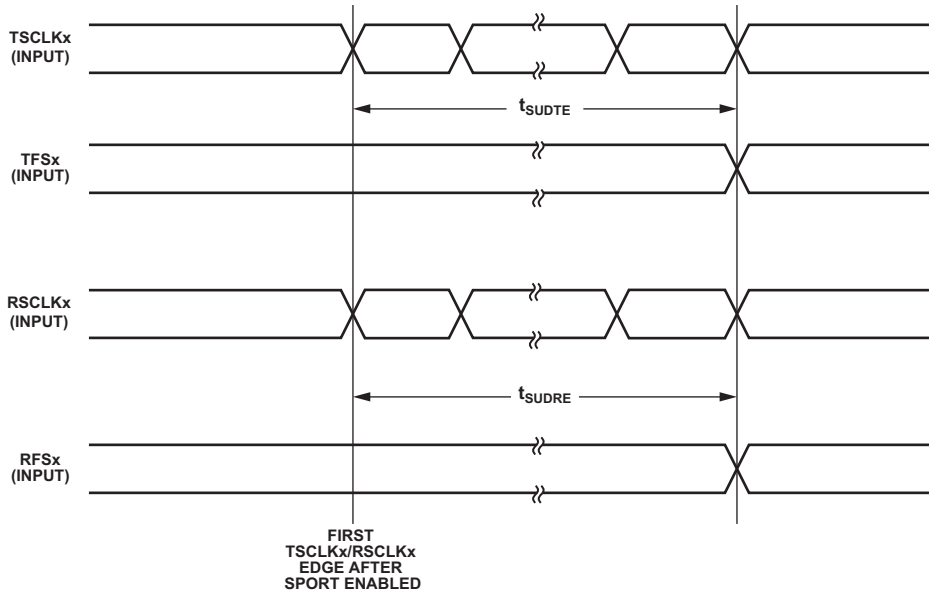


Figure 24. Serial Port Start Up with External Clock and Frame Sync

Serial Peripheral Interface (SPI) Port—Master Timing

Table 32. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Timing Requirements								
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	10.5		9		7.5		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	–1.5		–1.5		–1.5		ns
Switching Characteristics								
t_{SDSCIM}	$\overline{SPISELx}$ Low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISELx}$ High	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)		6		6		6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	–1.0		–1.0		–1.0		ns

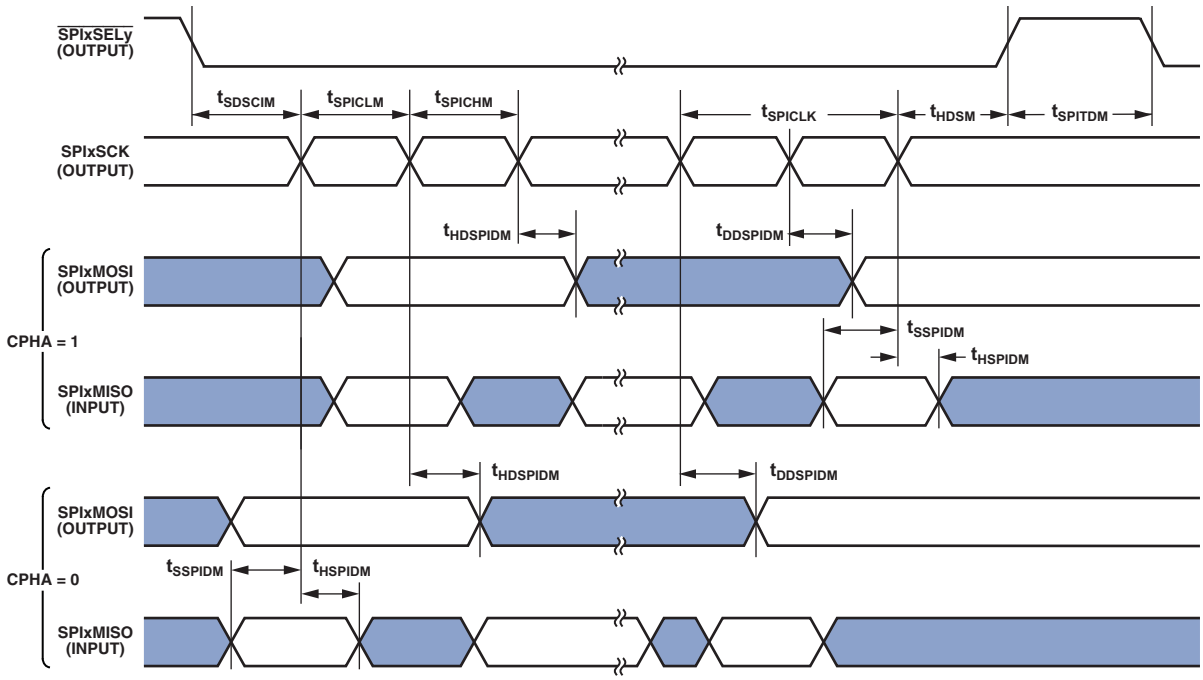


Figure 27. Serial Peripheral Interface (SPI) Port—Master Timing

JTAG Test and Emulation Port Timing

Table 37. JTAG Port Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{TCK}	TCK Period	20		20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		4		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	5		5		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width[2] (Measured in TCK Cycles)	4		4		TCK
Switching Characteristics						
t_{DTDO}	TDO Delay from TCK Low		10		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0	12	0	12	ns

[1] System Inputs = DATA15–0, ARDY, TMR2–0, PF15–0, PPI_CLK, RSCLK0–1, RFS0–1, DR0PRI, DR0SEC, TSCLK0–1, TFS0–1, DR1PRI, DR1SEC, MOSI, MISO, SCK, RX, $\overline{RESET}$, NMI, BMODE1–0, $\overline{BR}$, PPI3–0.

[2] 50 MHz maximum.

[3] System Outputs = DATA15–0, ADDR19–1, $\overline{ABE1–0}$, $\overline{AOE}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AMS3–0}$, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SCKE, CLKOUT, SA10, $\overline{SMS}$, TMR2–0, PF15–0, RSCLK0–1, RFS0–1, TSCLK0–1, TFS0–1, DT0PRI, DT0SEC, DT1PRI, DT1SEC, MOSI, MISO, SCK, TX, $\overline{BG}$, $\overline{BGH}$, PPI3–0.

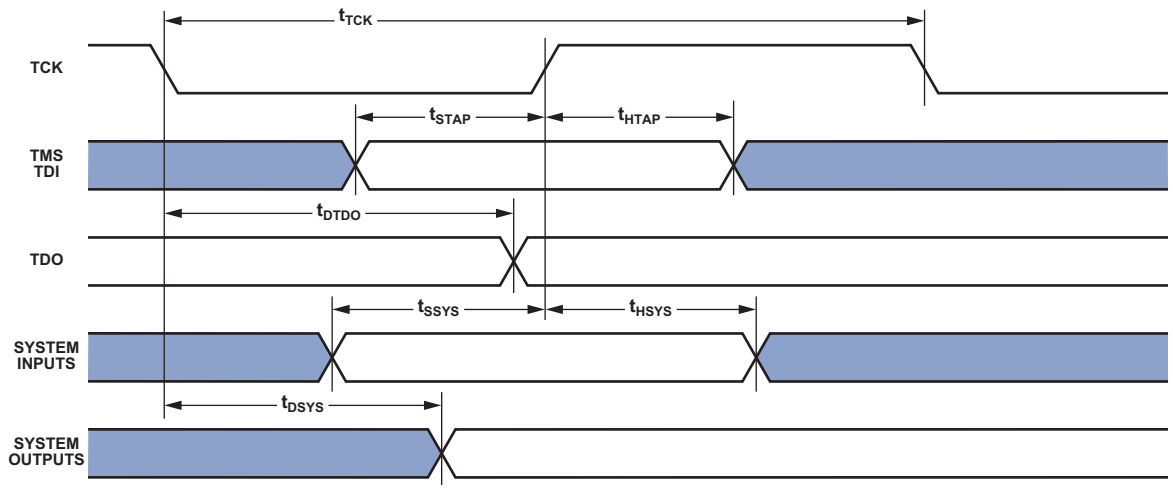


Figure 32. JTAG Port Timing

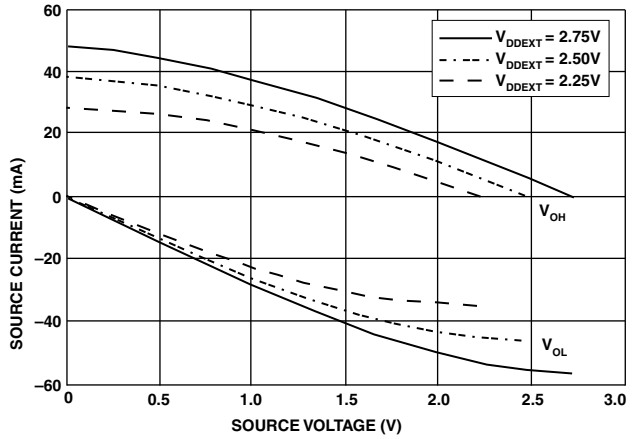


Figure 39. Drive Current C (V_{DDEXT} = 2.5 V)

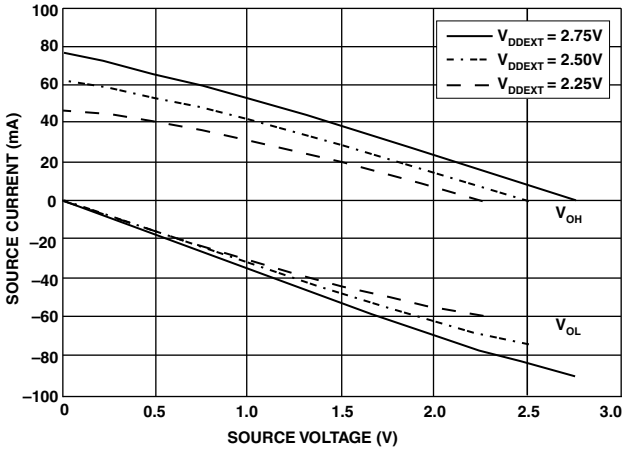


Figure 42. Drive Current D (V_{DDEXT} = 2.5 V)

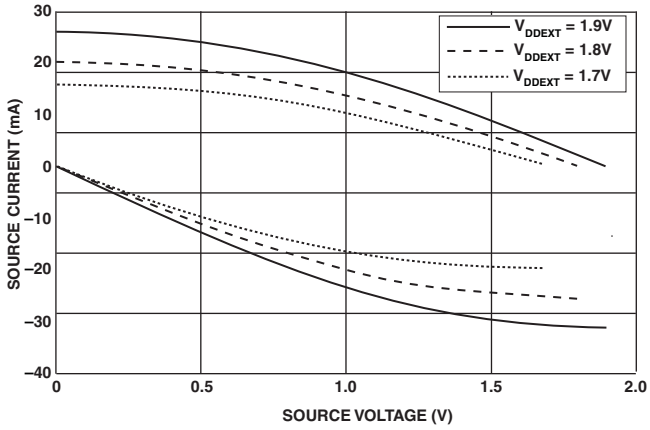


Figure 40. Drive Current C (V_{DDEXT} = 1.8 V)

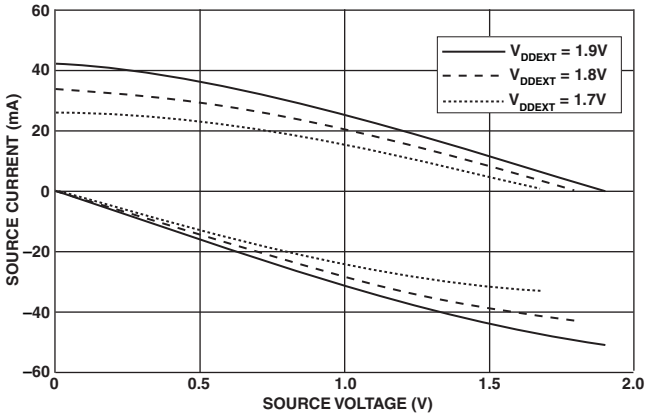


Figure 43. Drive Current D (V_{DDEXT} = 1.8 V)

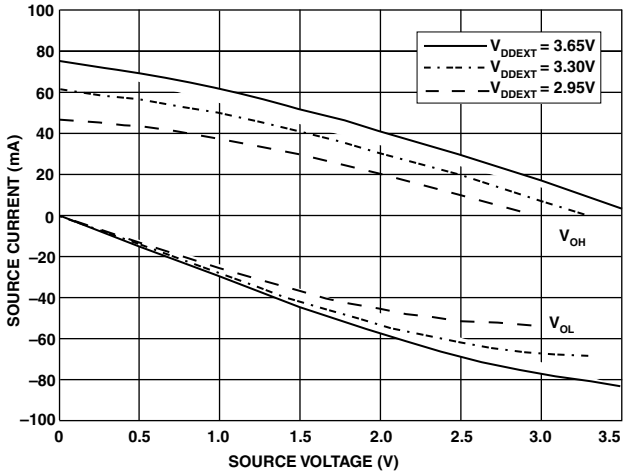


Figure 41. Drive Current C (V_{DDEXT} = 3.3 V)

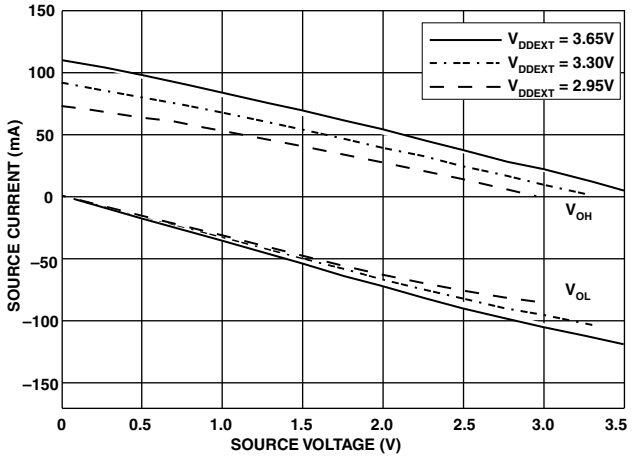


Figure 44. Drive Current D (V_{DDEXT} = 3.3 V)

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 45 shows the measurement point for ac measurements (except output enable/disable). The measurement point V_{MEAS} is 0.95 V for V_{DDEXT} (nominal) = 1.8 V or 1.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V.

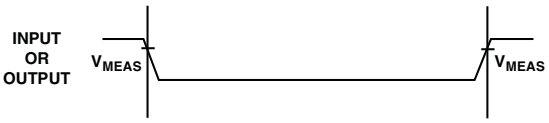


Figure 45. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 46.

The time $t_{ENA\_MEASURED}$ is the interval, from when the reference signal switches, to when the output voltage reaches V_{TRIP}(high) or V_{TRIP} (low).

For V_{DDEXT} (nominal) = 1.8 V—V_{TRIP} (high) is 1.3 V and V_{TRIP} (low) is 0.7 V.

For V_{DDEXT} (nominal) = 2.5 V/3.3 V—V_{TRIP} (high) is 2.0 V and V_{TRIP} (low) is 1.0 V.

Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the V_{TRIP} (high) or V_{TRIP} (low) trip voltage.

Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 45.

$$t_{DIS} = t_{DIS\_MEASURED} - t_{DECAY}$$

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load C_L and the load current I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.1 V for V_{DDEXT} (nominal) = 1.8 V or 0.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V.

The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches, to when the output voltage decays ΔV from the measured output high or output low voltage.

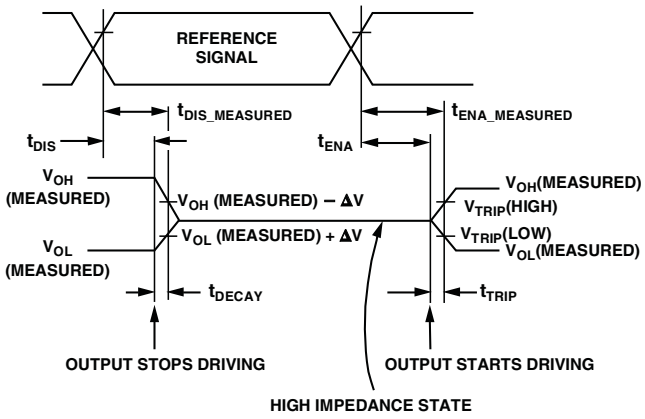


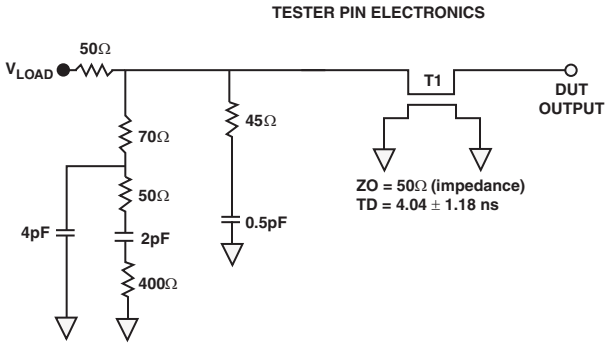
Figure 46. Output Enable/Disable

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the processor's output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time is t_{DECAY} plus the various output disable times as specified in the Timing Specifications on Page 27 (for example t_{DSDAT} for an SDRAM write cycle as shown in SDRAM Interface Timing on Page 30).

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 47). V_{LOAD} is 0.95 V for V_{DDEXT} (nominal) = 1.8 V or 1.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V. Figure 48 through Figure 59 on Page 48 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 47. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

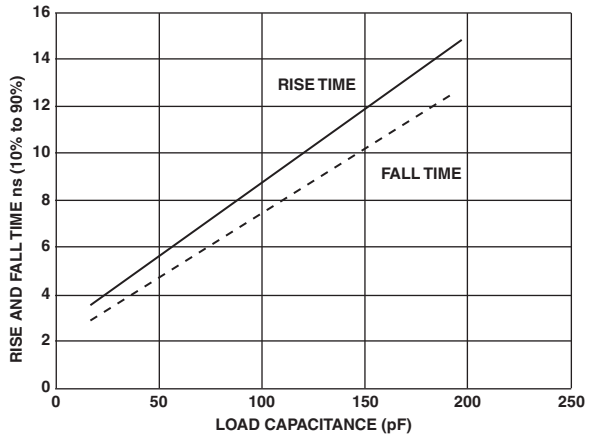


Figure 48. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 1.75 V

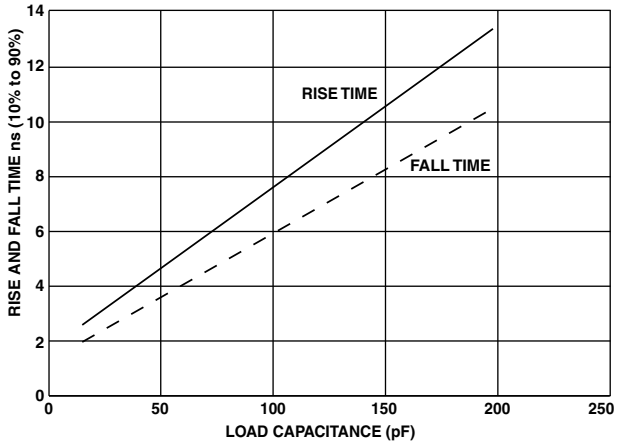


Figure 49. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 2.25 V

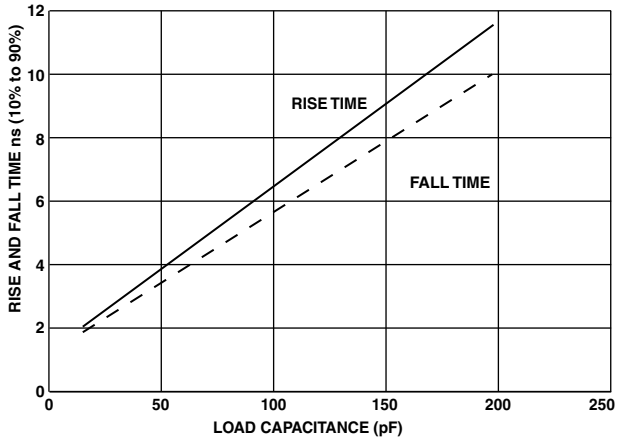


Figure 50. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 3.65 V

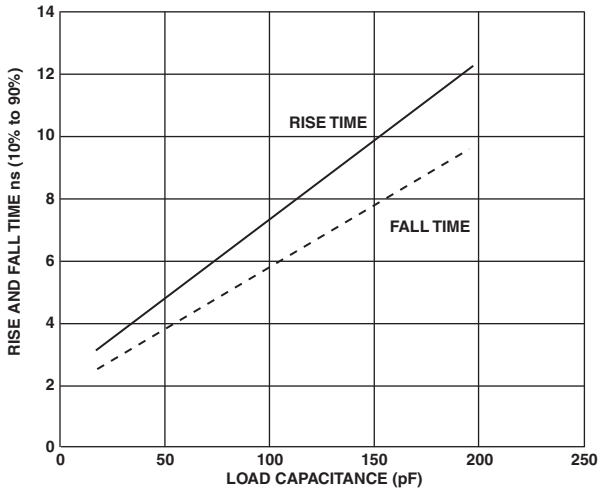


Figure 51. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 1.75 V

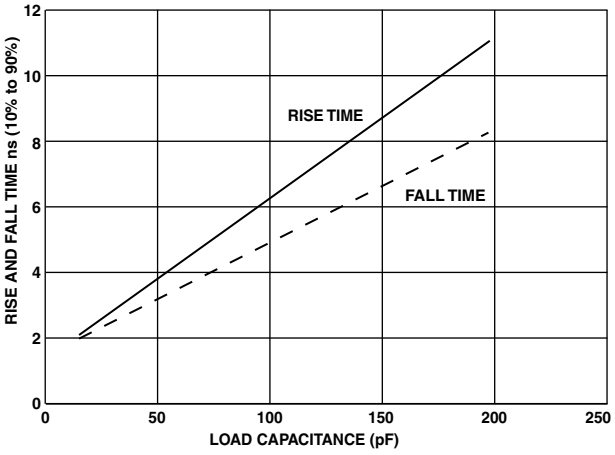


Figure 52. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 2.25 V

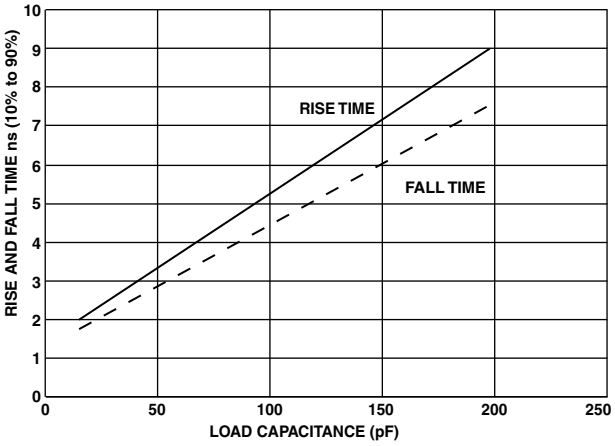


Figure 53. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 3.65 V

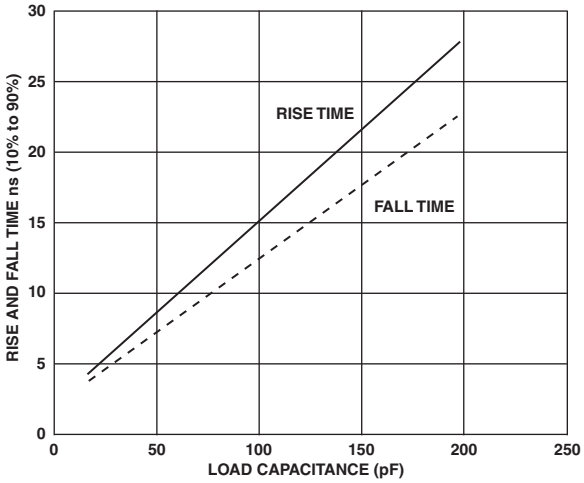


Figure 54. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 1.75 V

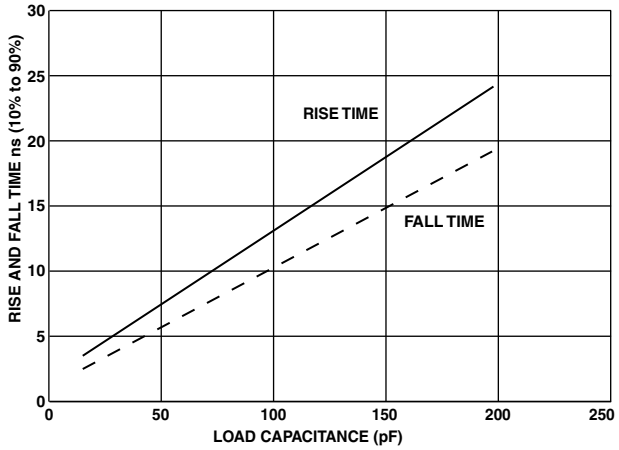


Figure 55. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 2.25 V

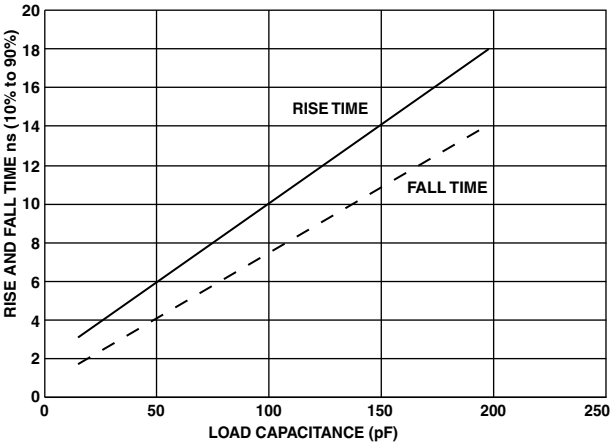


Figure 56. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 3.65 V

Table 42. 160-Ball CSP_BGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	V_{DDEXT}	C13	$\overline{SMS}$	H1	DT0PRI	M3	TDI
A2	PF8	C14	$\overline{SCAS}$	H2	DT0SEC	M4	GND
A3	PF9	D1	SCK	H3	TFS0	M5	DATA12
A4	PF10	D2	PF0	H4	GND	M6	DATA9
A5	PF11	D3	MOSI	H11	GND	M7	DATA6
A6	PF14	D4	GND	H12	$\overline{ABE1}$	M8	DATA3
A7	PPI2	D5	V_{DDEXT}	H13	$\overline{ABE0}$	M9	DATA0
A8	RTXO	D6	V_{DDINT}	H14	$\overline{AWE}$	M10	GND
A9	RTXI	D7	GND	J1	TSCLK0	M11	ADDR15
A10	GND	D8	GND	J2	DR0SEC	M12	ADDR9
A11	XTAL	D9	V_{DDEXT}	J3	RFS0	M13	ADDR10
A12	CLKIN	D10	GND	J4	V_{DDEXT}	M14	ADDR11
A13	VROUT0	D11	GND	J11	V_{DDINT}	N1	$\overline{TRST}$
A14	GND	D12	$\overline{SWE}$	J12	V_{DDEXT}	N2	TMS
B1	PF4	D13	$\overline{SRAS}$	J13	ADDR4	N3	TDO
B2	PF5	D14	$\overline{BR}$	J14	ADDR1	N4	BMODE0
B3	PF6	E1	TFS1	K1	DR0PRI	N5	DATA13
B4	PF7	E2	MISO	K2	TMR2	N6	DATA10
B5	PF12	E3	DT1SEC	K3	TX	N7	DATA7
B6	PF13	E4	V_{DDINT}	K4	GND	N8	DATA4
B7	PPI3	E11	V_{DDINT}	K11	GND	N9	DATA1
B8	PPI1	E12	SA10	K12	ADDR7	N10	$\overline{BGH}$
B9	V_{DDRTC}	E13	ARDY	K13	ADDR5	N11	ADDR16
B10	NMI	E14	$\overline{AMS0}$	K14	ADDR2	N12	ADDR14
B11	GND	F1	TSCLK1	L1	RSCLK0	N13	ADDR13
B12	VROUT1	F2	DT1PRI	L2	TMR0	N14	ADDR12
B13	SCKE	F3	DR1SEC	L3	RX	P1	V_{DDEXT}
B14	CLKOUT	F4	GND	L4	V_{DDINT}	P2	TCK
C1	PF1	F11	GND	L5	GND	P3	BMODE1
C2	PF2	F12	V_{DDEXT}	L6	GND	P4	DATA15
C3	PF3	F13	$\overline{AMS2}$	L7	V_{DDEXT}	P5	DATA14
C4	GND	F14	$\overline{AMS1}$	L8	GND	P6	DATA11
C5	GND	G1	RSCLK1	L9	V_{DDINT}	P7	DATA8
C6	PF15	G2	RFS1	L10	GND	P8	DATA5
C7	V_{DDEXT}	G3	DR1PRI	L11	V_{DDEXT}	P9	DATA2
C8	PPI0	G4	V_{DDEXT}	L12	ADDR8	P10	$\overline{BG}$
C9	PPI_CLK	G11	GND	L13	ADDR6	P11	ADDR19
C10	$\overline{RESET}$	G12	$\overline{AMS3}$	L14	ADDR3	P12	ADDR18
C11	GND	G13	$\overline{AOE}$	M1	TMR1	P13	ADDR17
C12	V_{DDEXT}	G14	$\overline{ARE}$	M2	$\overline{EMU}$	P14	GND

Figure 60 shows the top view of the CSP_BGA ball configuration. Figure 61 shows the bottom view of the CSP_BGA ball configuration.

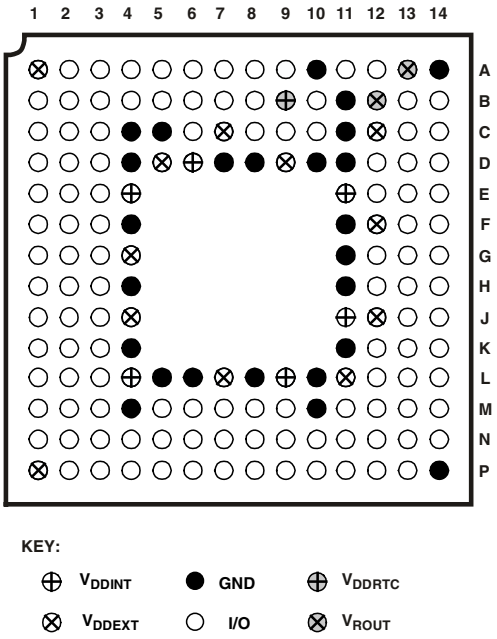


Figure 60. 160-Ball CSP_BGA Ground Configuration (Top View)

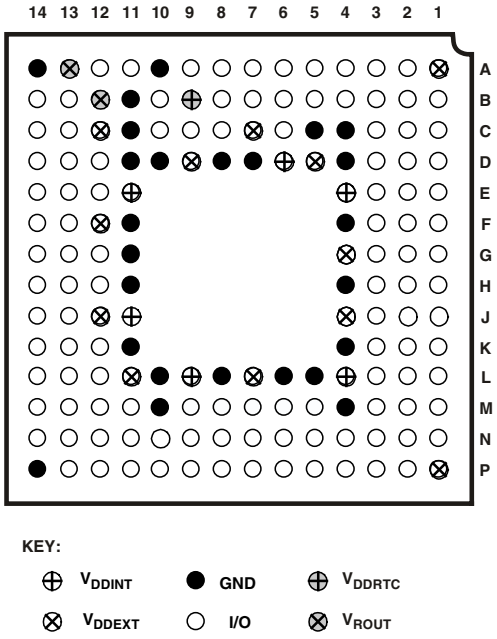


Figure 61. 160-Ball CSP_BGA Ground Configuration (Bottom View)

169-BALL PBGA BALL ASSIGNMENT

Table 43 lists the PBGA ball assignment by signal. Table 44 on Page 54 lists the PBGA ball assignment by ball number.

Table 43. 169-Ball PBGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{ABE0}$	H16	DATA4	U12	GND	K9	RTXI	A10	V_{DDEXT}	K6
$\overline{ABE1}$	H17	DATA5	U11	GND	K10	RTXO	A11	V_{DDEXT}	L6
ADDR1	J16	DATA6	T10	GND	K11	RX	T1	V_{DDEXT}	M6
ADDR2	J17	DATA7	U10	GND	L7	SA10	B15	V_{DDEXT}	M7
ADDR3	K16	DATA8	T9	GND	L8	$\overline{SCAS}$	A16	V_{DDEXT}	M8
ADDR4	K17	DATA9	U9	GND	L9	SCK	D1	V_{DDEXT}	T2
ADDR5	L16	DATA10	T8	GND	L10	SCKE	B14	VROUT0	B12
ADDR6	L17	DATA11	U8	GND	L11	$\overline{SMS}$	A17	VROUT1	B13
ADDR7	M16	DATA12	U7	GND	M9	$\overline{SRAS}$	A15	XTAL	A13
ADDR8	M17	DATA13	T7	GND	T16	$\overline{SWE}$	B17		
ADDR9	N17	DATA14	U6	MISO	E2	TCK	U4		
ADDR10	N16	DATA15	T6	MOSI	E1	TDI	U3		
ADDR11	P17	DR0PRI	M2	NMI	B11	TDO	T4		
ADDR12	P16	DR0SEC	M1	PF0	D2	TFS0	L1		
ADDR13	R17	DR1PRI	H1	PF1	C1	TFS1	G2		
ADDR14	R16	DR1SEC	H2	PF2	B1	TMR0	R1		
ADDR15	T17	DT0PRI	K2	PF3	C2	TMR1	P2		
ADDR16	U15	DT0SEC	K1	PF4	A1	TMR2	P1		
ADDR17	T15	DT1PRI	F1	PF5	A2	TMS	T3		
ADDR18	U16	DT1SEC	F2	PF6	B3	$\overline{TRST}$	U2		
ADDR19	T14	$\overline{EMU}$	U1	PF7	A3	TSCLK0	L2		
$\overline{AMS0}$	D17	GND	B16	PF8	B4	TSCLK1	G1		
$\overline{AMS1}$	E16	GND	F11	PF9	A4	TX	R2		
$\overline{AMS2}$	E17	GND	G7	PF10	B5	VDD	F12		
$\overline{AMS3}$	F16	GND	G8	PF11	A5	VDD	G12		
$\overline{AOE}$	F17	GND	G9	PF12	A6	VDD	H12		
ARDY	C16	GND	G10	PF13	B6	VDD	J12		
$\overline{ARE}$	G16	GND	G11	PF14	A7	VDD	K12		
$\overline{AWE}$	G17	GND	H7	PF15	B7	VDD	L12		
$\overline{BG}$	T13	GND	H8	PPI_CLK	B10	VDD	M10		
$\overline{BGH}$	U17	GND	H9	PPI0	B9	VDD	M11		
BMODE0	U5	GND	H10	PPI1	A9	VDD	M12		
BMODE1	T5	GND	H11	PPI2	B8	V_{DDEXT}	B2		
$\overline{BR}$	C17	GND	J7	PPI3	A8	V_{DDEXT}	F6		
CLKIN	A14	GND	J8	$\overline{RESET}$	A12	V_{DDEXT}	F7		
CLKOUT	D16	GND	J9	RFS0	N1	V_{DDEXT}	F8		
DATA0	U14	GND	J10	RFS1	J1	V_{DDEXT}	F9		
DATA1	T12	GND	J11	RSCLK0	N2	V_{DDEXT}	G6		
DATA2	U13	GND	K7	RSCLK1	J2	V_{DDEXT}	H6		
DATA3	T11	GND	K8	RTCVDD	F10	V_{DDEXT}	J6		

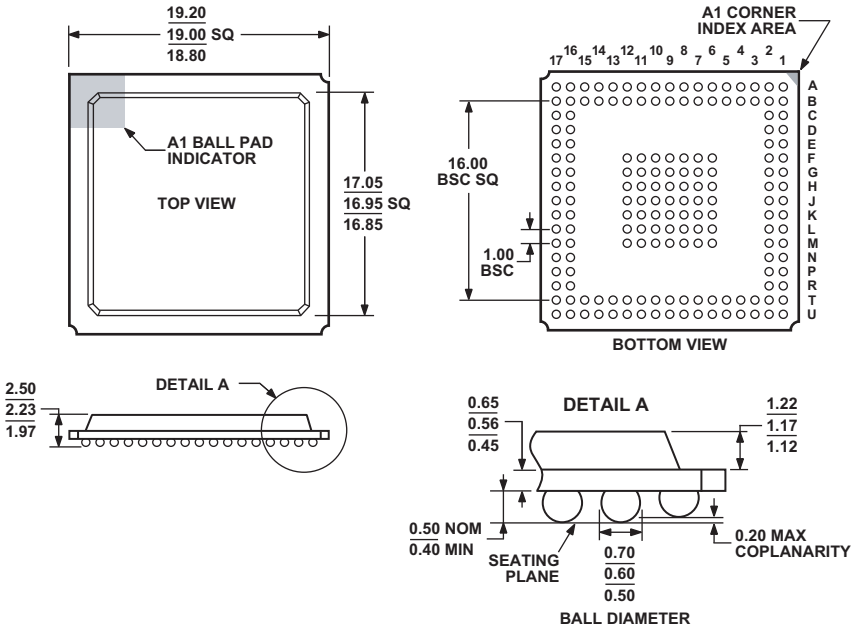


Figure 66. 169-Ball Plastic Ball Grid Array [PBGA]
(B-169)
Dimensions shown in millimeters