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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	400MHz
Non-Volatile Memory	ROM (1kB)
On-Chip RAM	84kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf532wbstz406

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REVISION HISTORY

8/13— Rev. H to Rev. I

Updated Development Tools 15

Corrected Conditions value of the V_{IL} specification in Operating Conditions 20

Added notes to Table 30 in Serial Ports—Enable and Three-State 36

Added Timer Clock Timing 41

Revised Timer Cycle Timing 41

Updated Ordering Guide 63

PFx pins defined as inputs can be configured to generate hardware interrupts, while output PFx pins can be triggered by software interrupts.

- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual PFx pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

PARALLEL PERIPHERAL INTERFACE

The processors provide a parallel peripheral interface (PPI) that can connect directly to parallel ADCs and DACs, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bi-directional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bi-directional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications.

Three distinct sub modes are supported:

- Input mode – Frame syncs and data are inputs into the PPI.
- Frame capture mode – Frame syncs are outputs from the PPI, but data are inputs.
- Output mode – Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (e.g., for frame capture). The processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct sub modes are supported:

- Active video only mode
- Vertical blanking only mode
- Entire field mode

Active Video Only Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that can be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

DYNAMIC POWER MANAGEMENT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provides four operating modes, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

t_{NOM} is the duration running at $f_{CCLKNOM}$

t_{RED} is the duration running at $f_{CCLKRED}$

The percent power savings is calculated as:

$$\%\ power\ savings\ =\ (1 - power\ savings\ factor) \times 100\%$$

VOLTAGE REGULATION

The Blackfin processor provides an on-chip voltage regulator that can generate appropriate V_{DDINT} voltage levels from the V_{DDEXT} supply. See Operating Conditions on Page 20 for regulator tolerances and acceptable V_{DDEXT} ranges for specific models.

Figure 7 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power (V_{DDEXT}) supplied. While in the hibernate state, I/O power is still being applied, eliminating the need for external buffers. The voltage regulator can be activated from this power-down state either through an RTC wakeup or by asserting $\overline{\text{RESET}}$, both of which initiate a boot sequence. The regulator can also be disabled and bypassed at the user's discretion.

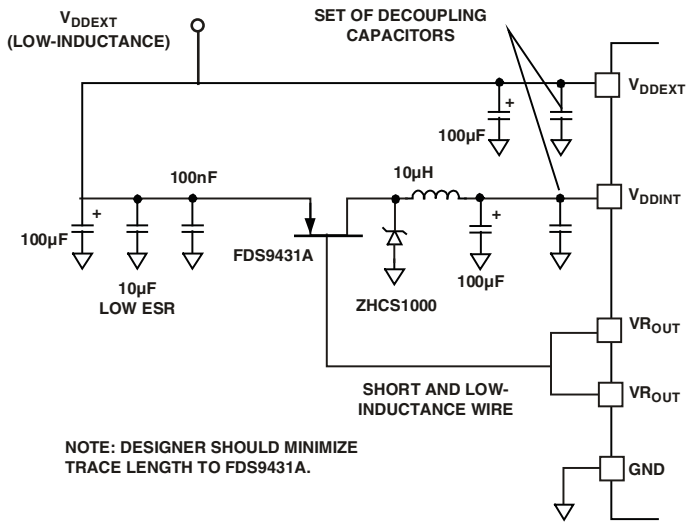


Figure 7. Voltage Regulator Circuit

Voltage Regulator Layout Guidelines

Regulator external component placement, board routing, and bypass capacitors all have a significant effect on noise injected into the other analog circuits on-chip. The VROUT1–0 traces and voltage regulator external components should be considered as noise sources when doing board layout and should not be routed or placed near sensitive circuits or components on the board. All internal and I/O power supplies should be well bypassed with bypass capacitors placed as close to the processors as possible.

For further details on the on-chip voltage regulator and related board design guidelines, see the *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228)* applications note on the Analog Devices web site (www.analog.com)—use site search on "EE-228".

CLOCK SIGNALS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the processors include an on-chip oscillator circuit, an external crystal can be used. For fundamental frequency operation, use the circuit shown in Figure 8.

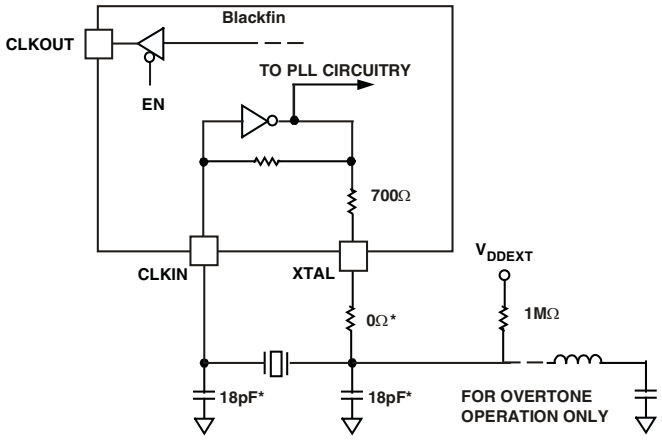


Figure 8. External Crystal Connections

A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor shown in Figure 8 fine tune the phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 8 are typical values only. The capacitor values are dependent upon the crystal manufacturer's load capacitance recommendations and the physical PCB layout. The resistor value depends on the drive level specified by the crystal manufacturer. System designs should verify the customized values based on careful investigation on multiple devices over the allowed temperature range.

A third-overtone crystal can be used at frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 8.

[5] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{TRST}$).
[6] Absolute value.
[7] Applies to three-statable pins.
[8] Applies to all signal pins.
[9] Guaranteed, but not tested.
[10] See the *ADSP-BF533 Blackfin Processor Hardware Reference Manual* for definitions of sleep, deep sleep, and hibernate operating modes.
[11] See Table 16 for the list of I_{DDINT} power vectors covered by various Activity Scaling Factors (ASF).

System designers should refer to *Estimating Power for the ADSP-BF531/BF532/BF533 Blackfin Processors (EE-229)*, which provides detailed information for optimizing designs for lowest power. All topics discussed in this section are described in detail in EE-229. Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 22 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 14 or Table 15), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 17).

The dynamic component is also subject to an Activity Scaling Factor (ASF) which represents application code running on the processor (Table 16).

Table 14. Static Current–500 MHz, 533 MHz, and 600 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})[2]														
T_J (°C)[2]	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V	1.45 V
–45	4.3	5.3	5.9	7.0	8.2	9.8	11.2	13.0	15.2	17.7	20.2	21.6	25.5	30.1	32.0
0	18.8	21.3	24.1	27.8	31.6	35.6	40.1	45.3	51.4	58.1	65.0	68.5	78.4	89.8	94.3
25	35.3	39.9	45.0	50.9	57.3	64.4	72.9	80.9	90.3	101.4	112.1	118.0	133.7	151.6	158.7
40	52.3	58.5	65.1	73.3	81.3	90.9	101.2	112.5	125.5	138.7	154.4	160.6	180.6	203.1	212.0
55	73.6	82.5	92.0	102.7	114.4	126.3	141.2	155.7	172.7	191.1	212.1	220.8	247.6	277.7	289.5
70	100.8	112.5	124.5	137.4	152.6	168.4	186.5	205.4	227.0	250.3	276.2	287.1	320.4	357.4	371.9
85	133.3	148.5	164.2	180.5	198.8	219.0	241.0	264.5	290.6	319.7	350.2	364.6	404.9	449.7	467.2
100	178.3	196.3	216.0	237.6	259.9	284.6	311.9	342.0	373.1	408.0	446.1	462.6	511.1	564.7	585.6
115	223.3	245.9	270.2	295.7	323.5	353.3	386.1	421.1	460.1	500.9	545.0	566.5	624.3	688.1	712.8
125	278.5	305.8	334.1	364.3	397.4	432.4	470.6	509.3	553.4	600.6	652.1	676.5	742.1	814.1	841.9

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 20.

Table 15. Static Current–400 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})[2]											
T_J (°C)[2]	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V
–45	0.9	1.1	1.3	1.5	1.8	2.2	2.6	3.1	3.8	4.4	5.0	5.4
0	3.3	3.7	4.2	4.8	5.5	6.3	7.2	8.1	8.9	10.1	11.2	11.9
25	7.5	8.4	9.4	10.0	11.2	12.6	14.1	15.5	17.2	19.0	21.2	21.9
40	12.0	13.1	14.3	15.9	17.4	19.4	21.5	23.5	25.8	28.1	30.8	32.0
55	18.3	20.0	21.9	23.6	26.0	28.2	30.8	33.7	36.8	39.8	43.4	45.0
70	27.7	30.3	32.6	35.3	38.2	41.7	45.2	49.0	52.8	57.6	62.4	64.2
85	38.2	41.7	44.9	48.6	52.7	57.3	61.7	66.7	72.0	77.5	83.9	86.5
100	54.1	58.1	63.2	67.8	73.2	78.8	84.9	91.5	98.4	106.0	113.8	117.2
115	73.9	80.0	86.3	91.9	99.1	106.6	114.1	122.4	131.1	140.9	151.1	155.5
125	98.7	106.3	113.8	122.1	130.8	140.2	149.7	160.4	171.9	183.8	197.0	202.4

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 20.

Table 16. Activity Scaling Factors

I_{DDINT} Power Vector[1]	Activity Scaling Factor (ASF)[2]
$I_{DD-PEAK}$	1.27
$I_{DD-HIGH}$	1.25
I_{DD-TYP}	1.00
I_{DD-APP}	0.86
I_{DD-NOP}	0.72
$I_{DD-IDLE}$	0.41

[1] See EE-229 for power vector definitions.
[2] All ASF values determined using a 10:1 CCLK:SCLK ratio.

Table 17. Dynamic Current (mA, with ASF = 1.0)[1]

	Voltage (V_{DDINT})[2]														
Frequency (MHz)[2]	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V	1.45 V
50	12.7	13.9	15.3	16.8	18.1	19.4	21.0	22.3	24.0	25.4	26.4	27.2	28.7	30.3	30.7
100	22.6	24.2	26.2	28.1	30.1	31.8	34.7	36.2	38.4	40.5	43.0	43.4	45.7	47.9	48.9
200	40.8	44.1	46.9	50.3	53.3	56.9	59.9	63.1	66.7	70.2	73.8	75.0	78.7	82.4	84.6
250	50.1	53.8	57.2	61.4	64.7	68.9	72.9	76.8	81.0	85.1	89.3	90.8	95.2	99.6	102.0
300	N/A	63.5	67.4	72.4	76.2	81.0	85.9	90.6	95.2	100.0	104.8	106.6	111.8	116.9	119.4
375	N/A	N/A	N/A	88.6	93.5	99.0	104.6	110.3	116.0	122.1	128.0	130.0	136.2	142.4	145.5
400	N/A	N/A	N/A	93.9	99.3	105.0	110.8	116.8	123.0	129.4	135.7	137.9	144.6	151.2	154.3
425	N/A	N/A	N/A	N/A	N/A	111.0	117.3	123.5	129.9	136.8	143.2	145.6	152.6	159.7	162.8
475	N/A	N/A	N/A	N/A	N/A	N/A	130.3	136.8	143.8	151.4	158.1	161.1	168.9	176.6	179.7
500	N/A	N/A	N/A	N/A	N/A	N/A	N/A	143.5	150.7	158.7	165.6	168.8	177.0	185.2	188.2
533	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	160.4	168.8	176.5	179.6	188.2	196.8	200.5
600	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	196.2	199.6	209.3	219.0	222.6

[1] The values are not guaranteed as stand-alone maximum specifications, they must be combined with static current per the equations of Electrical Characteristics on Page 22.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 20.

PACKAGE INFORMATION

The information presented in Figure 10 and Table 20 provides details about the package branding for the Blackfin processors. For a complete listing of product availability, see the Ordering Guide on Page 63.

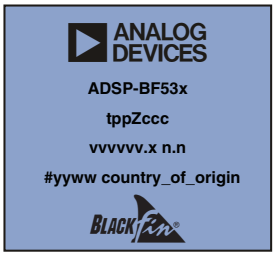


Figure 10. Product Information on Package

Table 20. Package Brand Information[1]

Brand Key	Field Description
ADSP-BF53x	Either ADSP-BF531, ADSP-BF532, or ADSP-BF533
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

[1] Non Automotive only. For branding information specific to Automotive products, contact Analog Devices Inc.

Parallel Peripheral Interface Timing

Table 27 and Figure 17 through Figure 22 describe parallel peripheral interface operations.

Table 27. Parallel Peripheral Interface Timing

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Timing Requirements								
t_{PCLKW}	PPI_CLK Width	8.0		8.0		6.0		ns
t_{PCLK}	PPI_CLK Period[1]	20.0		20.0		15.0		ns
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK Edge (Nonsampling Edge for Rx, Sampling Edge for Tx)	6.0		6.0		4.0[2]		ns ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.0[2]		1.0[2]		1.0[2]		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	3.5		3.5		3.5		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	1.5		1.5		1.5		ns
Switching Characteristics—GP Output and Frame Capture Modes								
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		11.0		8.0		8.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	1.7		1.7		1.7		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		11.0		9.0		9.0	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	1.8		1.8		1.8		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$.
[2] Applies when PPI_CONTROL Bit 8 is cleared. See Figure 19 and Figure 22.

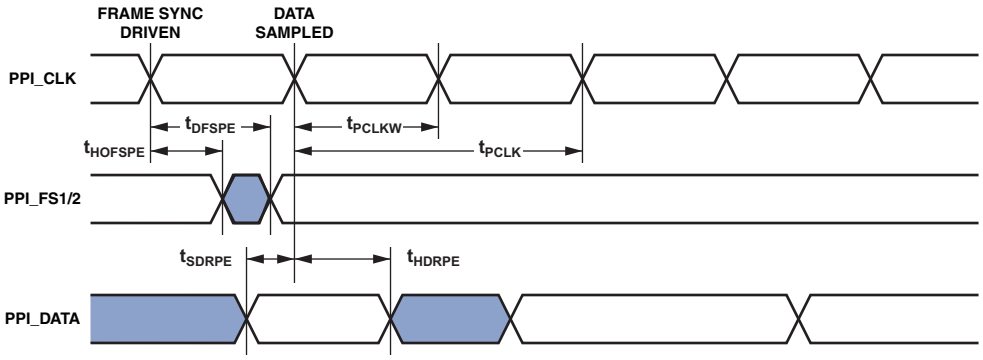


Figure 17. PPI GP Rx Mode with Internal Frame Sync Timing

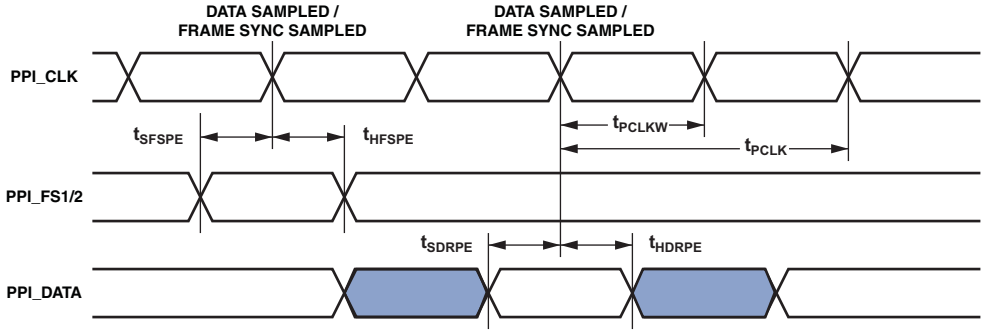


Figure 18. PPI GP Rx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 1)

Serial Port Timing

Table 28 through Table 31 on Page 37 and Figure 23 on Page 35 through Figure 26 on Page 37 describe Serial Port operations.

Table 28. Serial Ports—External Clock

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{SFSE}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	3.0		3.0		ns
t_{HFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	3.0		3.0		ns
t_{SDRE}	Receive Data Setup Before RSCLKx[1]	3.0		3.0		ns
t_{HDRE}	Receive Data Hold After RSCLKx[1]	3.0		3.0		ns
t_{SCLKEW}	TSCLKx/RSCLKx Width	8.0		4.5		ns
t_{SCLKE}	TSCLKx/RSCLKx Period	20.0		15.0[2]		ns
t_{SUDTE}	Start-Up Delay From SPORT Enable To First External TFSx[3]	4.0 × t_{SCLKE}		4.0 × t_{SCLKE}		ns
t_{SUDRE}	Start-Up Delay From SPORT Enable To First External RFSx[3]	4.0 × t_{SCLKE}		4.0 × t_{SCLKE}		ns
Switching Characteristics						
t_{DFSE}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[4]		10.0		10.0	ns
t_{HOFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[1]	0.0		0.0		ns
t_{DDTE}	Transmit Data Delay After TSCLKx[1]		10.0		10.0	ns
t_{HDTE}	Transmit Data Hold After TSCLKx[1]	0.0		0.0		ns

[1] Referenced to sample edge.
[2] For receive mode with external RSCLKx and external RFSx only, the maximum specification is 11.11 ns (90 MHz).
[3] Verified in design but untested. After being enabled, the serial port requires external clock pulses—before the first external frame sync edge—to initialize the serial port.
[4] Referenced to drive edge.

Table 29. Serial Ports—Internal Clock

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{SFSI}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	11.0		9.0		ns
t_{HFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	–2.0		–2.0		ns
t_{SDRI}	Receive Data Setup Before RSCLKx[1]	9.5		9.0		ns
t_{HDRI}	Receive Data Hold After RSCLKx[1]	0.0		0.0		ns
Switching Characteristics						
t_{DFSI}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]		3.0		3.0	ns
t_{HOFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[1]	–1.0		–1.0		ns
t_{DDTI}	Transmit Data Delay After TSCLKx[1]		3.0		3.0	ns
t_{HDTI}	Transmit Data Hold After TSCLKx[1]	–2.5		–2.0		ns
t_{SCLKIW}	TSCLKx/RSCLKx Width	6.0		4.5		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

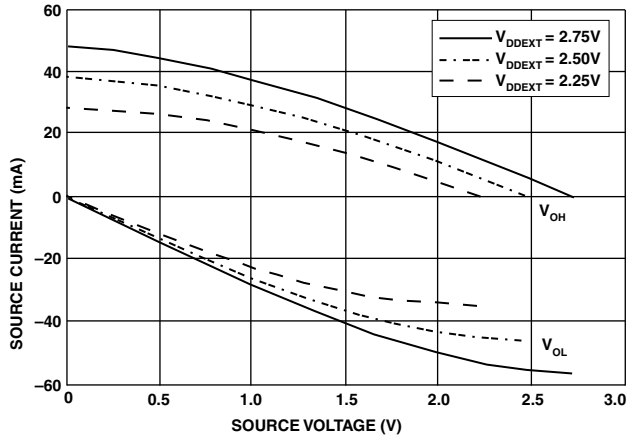


Figure 39. Drive Current C (V_{DDEXT} = 2.5 V)

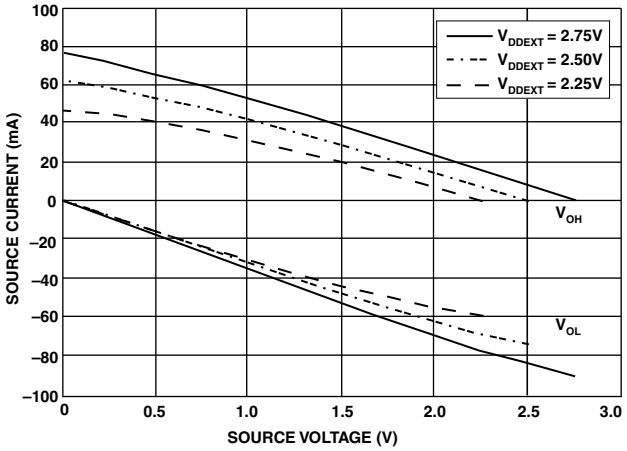


Figure 42. Drive Current D (V_{DDEXT} = 2.5 V)

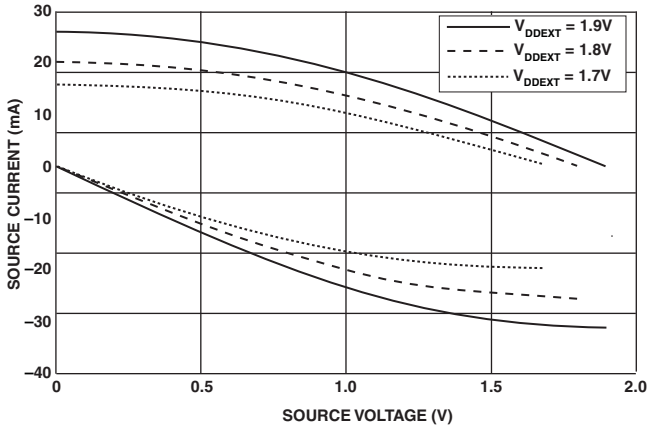


Figure 40. Drive Current C (V_{DDEXT} = 1.8 V)

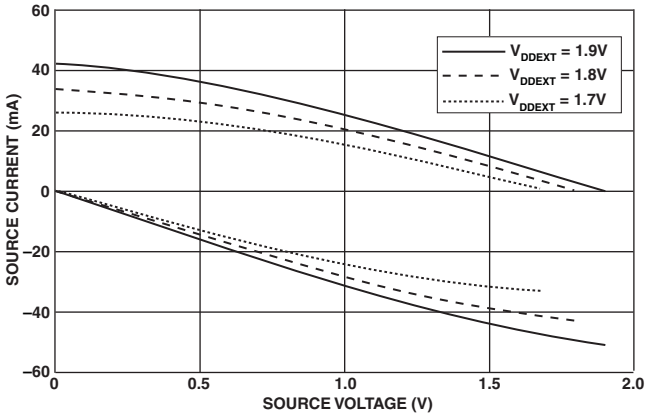


Figure 43. Drive Current D (V_{DDEXT} = 1.8 V)

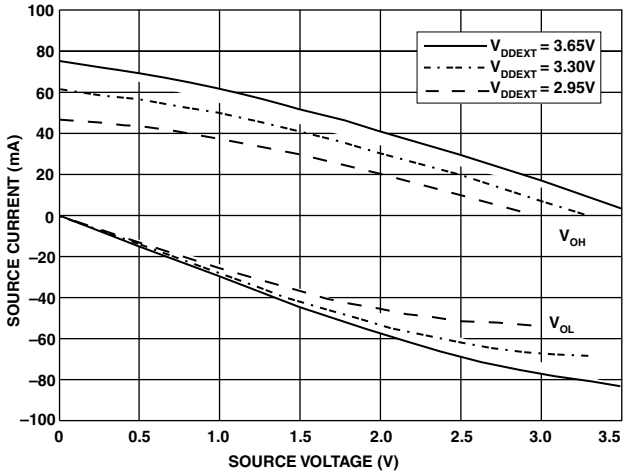


Figure 41. Drive Current C (V_{DDEXT} = 3.3 V)

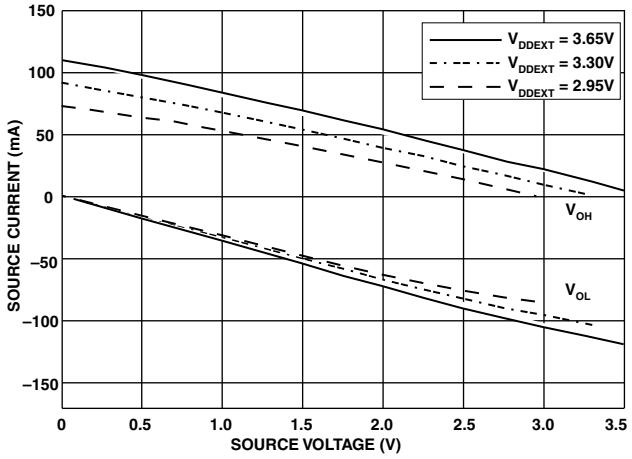
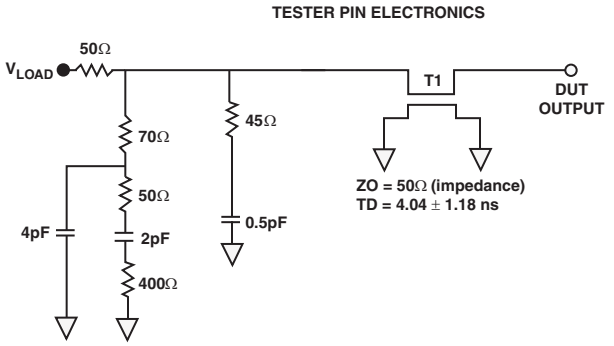


Figure 44. Drive Current D (V_{DDEXT} = 3.3 V)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 47). V_{LOAD} is 0.95 V for V_{DDEXT} (nominal) = 1.8 V or 1.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V. Figure 48 through Figure 59 on Page 48 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 47. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

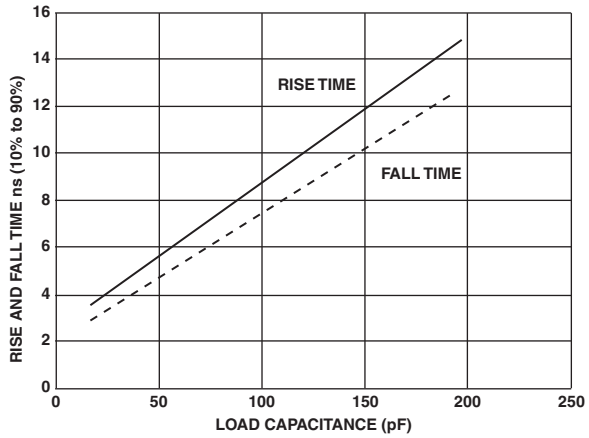


Figure 48. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 1.75 V

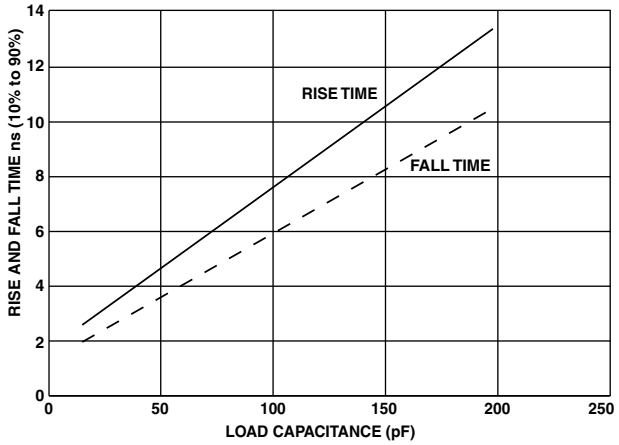


Figure 49. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 2.25 V

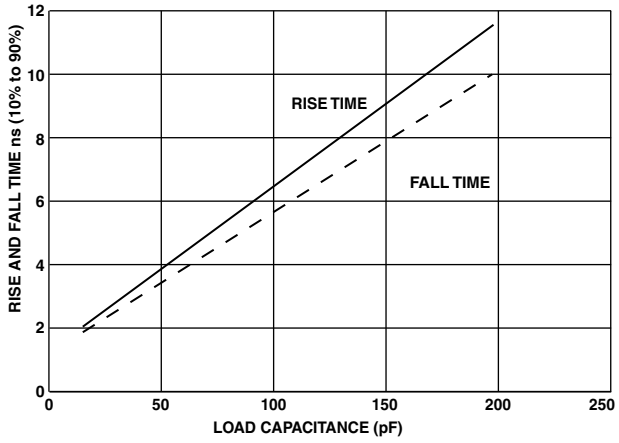


Figure 50. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 3.65 V

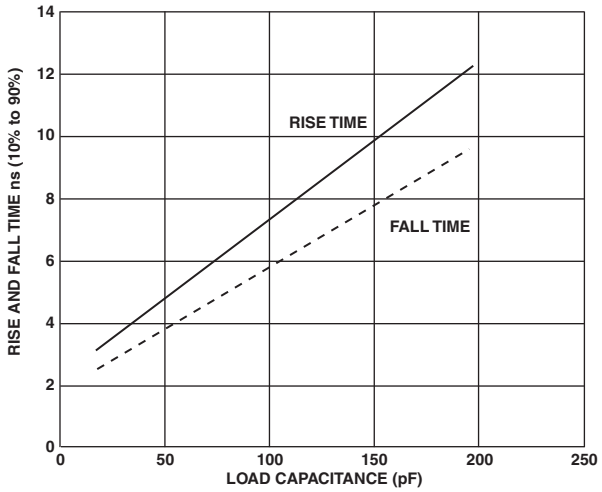


Figure 51. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 1.75 V

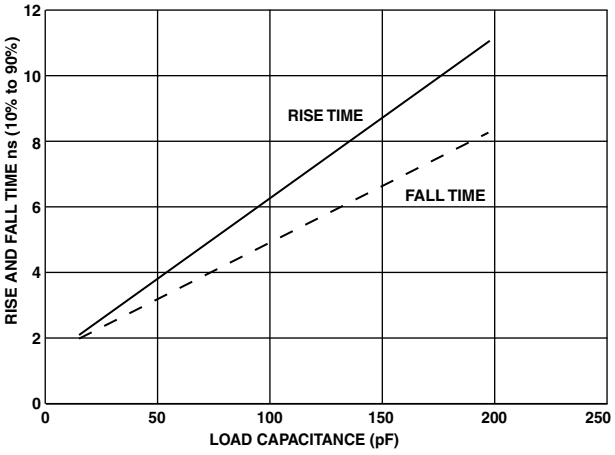


Figure 52. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 2.25 V

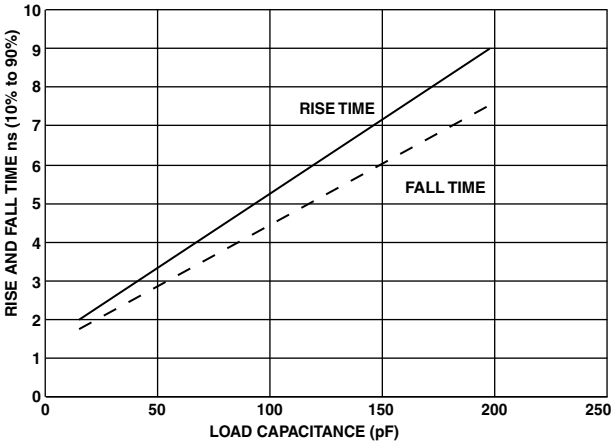


Figure 53. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 3.65 V

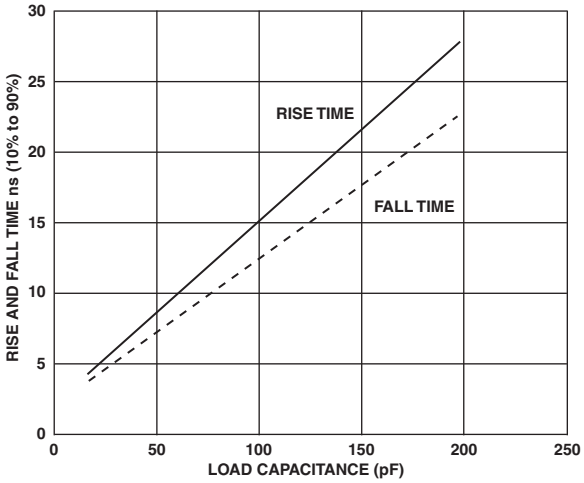


Figure 54. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 1.75 V

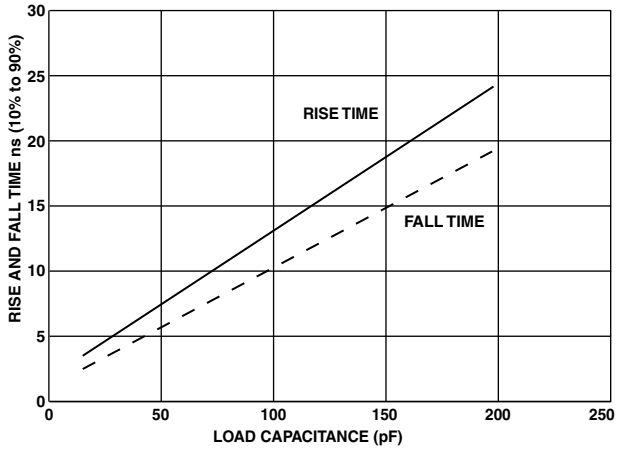


Figure 55. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 2.25 V

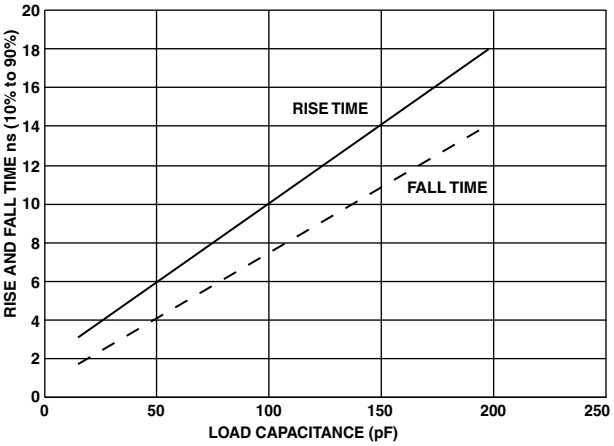


Figure 56. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 3.65 V

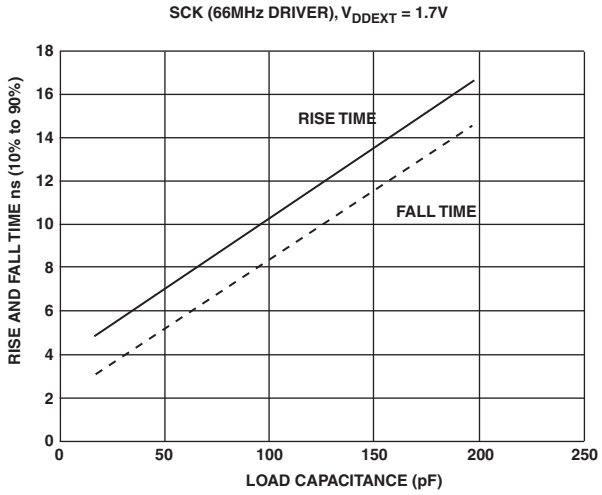


Figure 57. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at V_{DDEXT} = 1.75 V

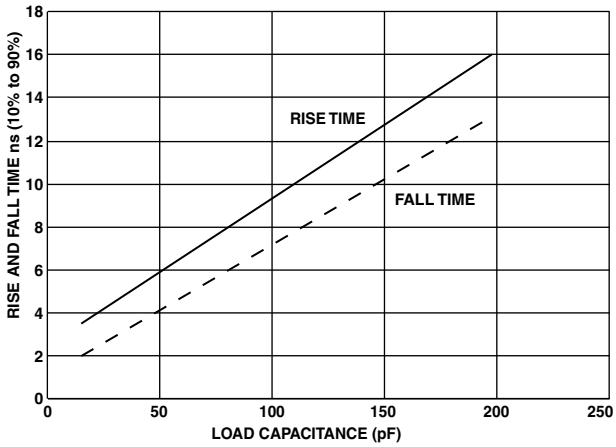


Figure 58. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at V_{DDEXT} = 2.25 V

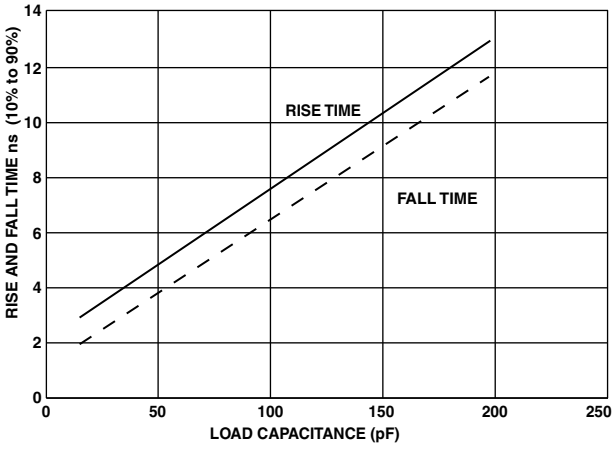


Figure 59. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at V_{DDEXT} = 3.65 V

Table 42. 160-Ball CSP_BGA Ball Assignment (Numerical by Ball Number)

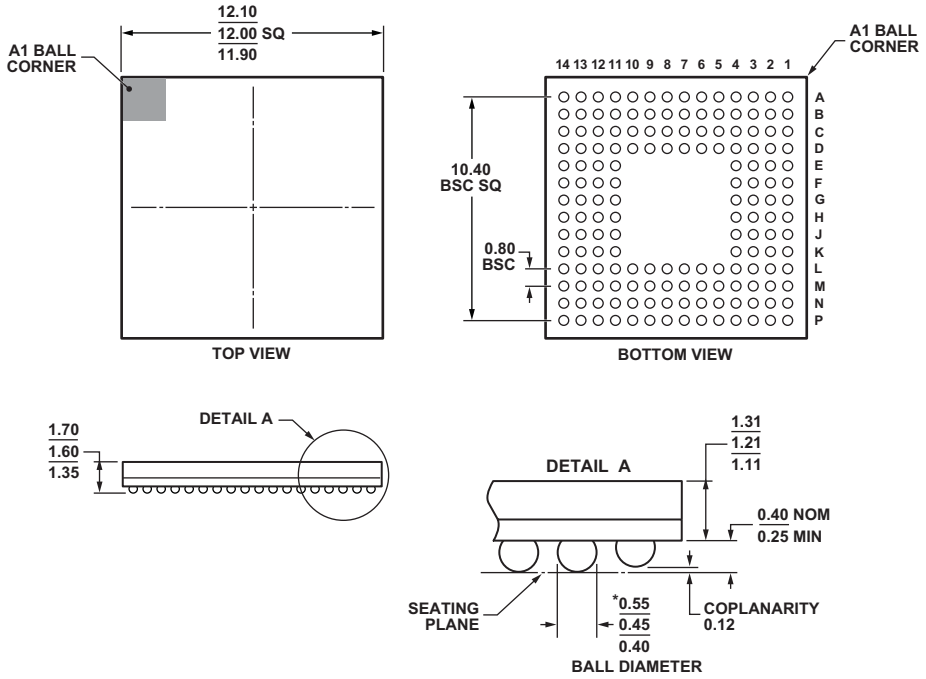
Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	V_{DDEXT}	C13	$\overline{SMS}$	H1	DT0PRI	M3	TDI
A2	PF8	C14	$\overline{SCAS}$	H2	DT0SEC	M4	GND
A3	PF9	D1	SCK	H3	TFS0	M5	DATA12
A4	PF10	D2	PF0	H4	GND	M6	DATA9
A5	PF11	D3	MOSI	H11	GND	M7	DATA6
A6	PF14	D4	GND	H12	$\overline{ABE1}$	M8	DATA3
A7	PPI2	D5	V_{DDEXT}	H13	$\overline{ABE0}$	M9	DATA0
A8	RTXO	D6	V_{DDINT}	H14	$\overline{AWE}$	M10	GND
A9	RTXI	D7	GND	J1	TSCLK0	M11	ADDR15
A10	GND	D8	GND	J2	DR0SEC	M12	ADDR9
A11	XTAL	D9	V_{DDEXT}	J3	RFS0	M13	ADDR10
A12	CLKIN	D10	GND	J4	V_{DDEXT}	M14	ADDR11
A13	VROUT0	D11	GND	J11	V_{DDINT}	N1	$\overline{TRST}$
A14	GND	D12	$\overline{SWE}$	J12	V_{DDEXT}	N2	TMS
B1	PF4	D13	$\overline{SRAS}$	J13	ADDR4	N3	TDO
B2	PF5	D14	$\overline{BR}$	J14	ADDR1	N4	BMODE0
B3	PF6	E1	TFS1	K1	DR0PRI	N5	DATA13
B4	PF7	E2	MISO	K2	TMR2	N6	DATA10
B5	PF12	E3	DT1SEC	K3	TX	N7	DATA7
B6	PF13	E4	V_{DDINT}	K4	GND	N8	DATA4
B7	PPI3	E11	V_{DDINT}	K11	GND	N9	DATA1
B8	PPI1	E12	SA10	K12	ADDR7	N10	$\overline{BGH}$
B9	V_{DDRTC}	E13	ARDY	K13	ADDR5	N11	ADDR16
B10	NMI	E14	$\overline{AMS0}$	K14	ADDR2	N12	ADDR14
B11	GND	F1	TSCLK1	L1	RSCLK0	N13	ADDR13
B12	VROUT1	F2	DT1PRI	L2	TMR0	N14	ADDR12
B13	SCKE	F3	DR1SEC	L3	RX	P1	V_{DDEXT}
B14	CLKOUT	F4	GND	L4	V_{DDINT}	P2	TCK
C1	PF1	F11	GND	L5	GND	P3	BMODE1
C2	PF2	F12	V_{DDEXT}	L6	GND	P4	DATA15
C3	PF3	F13	$\overline{AMS2}$	L7	V_{DDEXT}	P5	DATA14
C4	GND	F14	$\overline{AMS1}$	L8	GND	P6	DATA11
C5	GND	G1	RSCLK1	L9	V_{DDINT}	P7	DATA8
C6	PF15	G2	RFS1	L10	GND	P8	DATA5
C7	V_{DDEXT}	G3	DR1PRI	L11	V_{DDEXT}	P9	DATA2
C8	PPI0	G4	V_{DDEXT}	L12	ADDR8	P10	$\overline{BG}$
C9	PPI_CLK	G11	GND	L13	ADDR6	P11	ADDR19
C10	$\overline{RESET}$	G12	$\overline{AMS3}$	L14	ADDR3	P12	ADDR18
C11	GND	G13	$\overline{AOE}$	M1	TMR1	P13	ADDR17
C12	V_{DDEXT}	G14	$\overline{ARE}$	M2	$\overline{EMU}$	P14	GND

169-BALL PBGA BALL ASSIGNMENT

Table 43 lists the PBGA ball assignment by signal. Table 44 on Page 54 lists the PBGA ball assignment by ball number.

Table 43. 169-Ball PBGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{ABE0}$	H16	DATA4	U12	GND	K9	RTXI	A10	V_{DDEXT}	K6
$\overline{ABE1}$	H17	DATA5	U11	GND	K10	RTXO	A11	V_{DDEXT}	L6
ADDR1	J16	DATA6	T10	GND	K11	RX	T1	V_{DDEXT}	M6
ADDR2	J17	DATA7	U10	GND	L7	SA10	B15	V_{DDEXT}	M7
ADDR3	K16	DATA8	T9	GND	L8	$\overline{SCAS}$	A16	V_{DDEXT}	M8
ADDR4	K17	DATA9	U9	GND	L9	SCK	D1	V_{DDEXT}	T2
ADDR5	L16	DATA10	T8	GND	L10	SCKE	B14	VROUT0	B12
ADDR6	L17	DATA11	U8	GND	L11	$\overline{SMS}$	A17	VROUT1	B13
ADDR7	M16	DATA12	U7	GND	M9	$\overline{SRAS}$	A15	XTAL	A13
ADDR8	M17	DATA13	T7	GND	T16	$\overline{SWE}$	B17		
ADDR9	N17	DATA14	U6	MISO	E2	TCK	U4		
ADDR10	N16	DATA15	T6	MOSI	E1	TDI	U3		
ADDR11	P17	DR0PRI	M2	NMI	B11	TDO	T4		
ADDR12	P16	DR0SEC	M1	PF0	D2	TFS0	L1		
ADDR13	R17	DR1PRI	H1	PF1	C1	TFS1	G2		
ADDR14	R16	DR1SEC	H2	PF2	B1	TMR0	R1		
ADDR15	T17	DT0PRI	K2	PF3	C2	TMR1	P2		
ADDR16	U15	DT0SEC	K1	PF4	A1	TMR2	P1		
ADDR17	T15	DT1PRI	F1	PF5	A2	TMS	T3		
ADDR18	U16	DT1SEC	F2	PF6	B3	$\overline{TRST}$	U2		
ADDR19	T14	$\overline{EMU}$	U1	PF7	A3	TSCLK0	L2		
$\overline{AMS0}$	D17	GND	B16	PF8	B4	TSCLK1	G1		
$\overline{AMS1}$	E16	GND	F11	PF9	A4	TX	R2		
$\overline{AMS2}$	E17	GND	G7	PF10	B5	VDD	F12		
$\overline{AMS3}$	F16	GND	G8	PF11	A5	VDD	G12		
$\overline{AOE}$	F17	GND	G9	PF12	A6	VDD	H12		
ARDY	C16	GND	G10	PF13	B6	VDD	J12		
$\overline{ARE}$	G16	GND	G11	PF14	A7	VDD	K12		
$\overline{AWE}$	G17	GND	H7	PF15	B7	VDD	L12		
$\overline{BG}$	T13	GND	H8	PPI_CLK	B10	VDD	M10		
$\overline{BGH}$	U17	GND	H9	PPI0	B9	VDD	M11		
BMODE0	U5	GND	H10	PPI1	A9	VDD	M12		
BMODE1	T5	GND	H11	PPI2	B8	V_{DDEXT}	B2		
$\overline{BR}$	C17	GND	J7	PPI3	A8	V_{DDEXT}	F6		
CLKIN	A14	GND	J8	$\overline{RESET}$	A12	V_{DDEXT}	F7		
CLKOUT	D16	GND	J9	RFS0	N1	V_{DDEXT}	F8		
DATA0	U14	GND	J10	RFS1	J1	V_{DDEXT}	F9		
DATA1	T12	GND	J11	RSCLK0	N2	V_{DDEXT}	G6		
DATA2	U13	GND	K7	RSCLK1	J2	V_{DDEXT}	H6		
DATA3	T11	GND	K8	RTCVDD	F10	V_{DDEXT}	J6		



*COMPLIANT TO JEDEC STANDARDS MO-205-AE WITH THE EXCEPTION TO BALL DIAMETER.

Figure 65. 160-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-160-2)
Dimensions shown in millimeters

AUTOMOTIVE PRODUCTS

The ADBF531W, ADBF532W, and ADBF533W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 48 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 48. Automotive Products

Product Family[1,2]	Temperature Range[3]	Speed Grade (Max)	Package Description	Package Option
ADBF531WBSTZ4xx	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADBF531WBBCZ4xx	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF531WYBCZ4xx	–40°C to +105°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF532WBSTZ4xx	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADBF532WBBCZ4xx	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF532WYBCZ4xx	–40°C to +105°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF533WBBCZ5xx	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADBF533WBBZ5xx	–40°C to +85°C	533 MHz	169-Ball PBGA	B-169
ADBF533WYBCZ4xx	–40°C to +105°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF533WYBBZ4xx	–40°C to +105°C	400 MHz	169-Ball PBGA	B-169

[1] Z = RoHS compliant part.
[2] xx denotes silicon revision.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 20 for junction temperature (T_J) specification which is the only temperature specification.

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