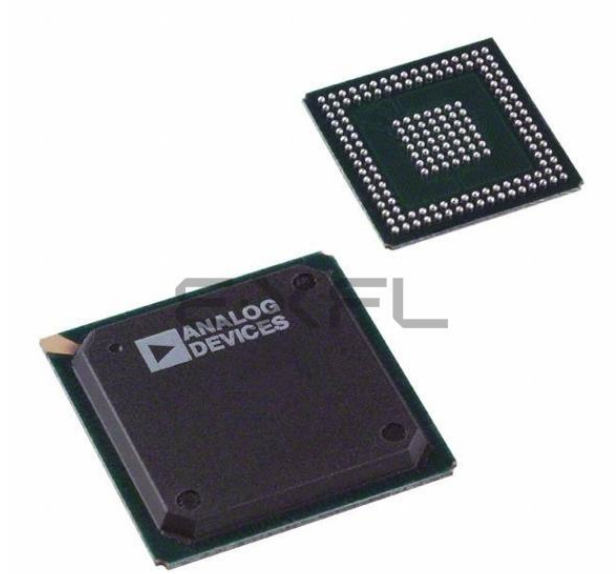

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	400MHz
Non-Volatile Memory	ROM (1kB)
On-Chip RAM	52kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-BBGA
Supplier Device Package	169-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf531sbb400

GENERAL DESCRIPTION

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are members of the Blackfin® family of products, incorporating the Analog Devices, Inc./Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single instruction, multiple data (SIMD) multimedia capabilities into a single instruction set architecture.

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are completely code and pin-compatible, differing only with respect to their performance and on-chip memory. Specific performance and memory configurations are shown in Table 1.

Table 1. Processor Comparison

Features		ADSP-BF531	ADSP-BF532	ADSP-BF533
SPORTs		2	2	2
UART		1	1	1
SPI		1	1	1
GP Timers		3	3	3
Watchdog Timers		1	1	1
RTC		1	1	1
Parallel Peripheral Interface		1	1	1
GPIOs		16	16	16
Memory Configuration	L1 Instruction SRAM/Cache	16K bytes	16K bytes	16K bytes
	L1 Instruction SRAM	16K bytes	32K bytes	64K bytes
	L1 Data SRAM/Cache	16K bytes	32K bytes	32K bytes
	L1 Data SRAM			32K bytes
	L1 Scratchpad	4K bytes	4K bytes	4K bytes
	L3 Boot ROM	1K bytes	1K bytes	1K bytes
Maximum Speed Grade		400 MHz	400 MHz	600 MHz
Package Options: CSP_BGA Plastic BGA LQFP		 160-Ball 169-Ball 176-Lead	 160-Ball 169-Ball 176-Lead	 160-Ball 169-Ball 176-Lead

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

PORTABLE LOW POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. Blackfin processors are designed in a low power and low voltage design methodology and feature dynamic power management—the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. Varying the voltage and frequency can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This translates into longer battery life for portable appliances.

SYSTEM INTEGRATION

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are highly integrated system-on-a-chip solutions for the next generation of digital communication and consumer multimedia applications. By combining industry-standard interfaces with a high performance signal processing core, users can develop cost-effective solutions quickly without the need for costly external components. The system peripherals include a UART port, an SPI port, two serial ports (SPORTs), four general-purpose timers (three with PWM capability), a real-time clock, a watchdog timer, and a parallel peripheral interface.

PROCESSOR PERIPHERALS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors contain a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the functional block diagram in Figure 1 on Page 1). The general-purpose peripherals include functions such as UART, timers with PWM (pulse-width modulation) and pulse measurement capability, general-purpose I/O pins, a real-time clock, and a watchdog timer. This set of functions satisfies a wide variety of typical system support needs and is augmented by the system expansion capabilities of the part. In addition to these general-purpose peripherals, the processors contain high speed serial and parallel ports for interfacing to a variety of audio, video, and modem codec functions; an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources; and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

All of the peripherals, except for general-purpose I/O, real-time clock, and timers, are supported by a flexible DMA structure. There is also a separate memory DMA channel dedicated to data transfers between the processor's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses running at up to 133 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The processors include an on-chip voltage regulator in support of the processor's dynamic power management capability. The voltage regulator provides a range of core voltage levels from V_{DDEXT}. The voltage regulator can be bypassed at the user's discretion.

PFx pins defined as inputs can be configured to generate hardware interrupts, while output PFx pins can be triggered by software interrupts.

- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual PFx pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

PARALLEL PERIPHERAL INTERFACE

The processors provide a parallel peripheral interface (PPI) that can connect directly to parallel ADCs and DACs, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bi-directional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bi-directional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications.

Three distinct sub modes are supported:

- Input mode – Frame syncs and data are inputs into the PPI.
- Frame capture mode – Frame syncs are outputs from the PPI, but data are inputs.
- Output mode – Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (e.g., for frame capture). The processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct sub modes are supported:

- Active video only mode
- Vertical blanking only mode
- Entire field mode

Active Video Only Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that can be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

DYNAMIC POWER MANAGEMENT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provides four operating modes, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Power Savings

In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. DMA access is available to appropriately configured L1 memories.

In the active mode, it is possible to disable the PLL through the PLL control register (PLL_CTL). If disabled, the PLL must be re-enabled before it can transition to the full-on or sleep modes.

Table 4. Power Settings

Mode	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)	Internal Power (V_{DDINT})
Full On	Enabled	No	Enabled	Enabled	On
Active	Enabled/ Disabled	Yes	Enabled	Enabled	On
Sleep	Enabled	—	Disabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event or RTC activity will wake up the processor. When in the sleep mode, assertion of wakeup causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor will transition to the full-on mode. If BYPASS is enabled, the processor will transition to the active mode.

When in the sleep mode, system DMA access to L1 memory is not supported.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals, such as the RTC, may still be running but cannot access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. When in deep sleep mode, an RTC asynchronous interrupt causes the processor to transition to the active mode. Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full-on mode.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and to all the synchronous peripherals (SCLK). The internal voltage regulator for the processor can be shut off by writing b#00 to the FREQ bits of the VR_CTL register. In addition to disabling the clocks, this sets the internal power supply voltage (V_{DDINT}) to 0 V to provide the lowest static power dissipation. Any critical information stored internally (memory contents, register contents, etc.) must be written to a nonvolatile storage device prior to removing power if the processor state is to be preserved. Since V_{DDEXT} is still supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current. The internal supply regulator can be woken up either by a real-time clock wakeup or by asserting the $\overline{\text{RESET}}$ pin.

Power Savings

As shown in Table 5, the processors support three different power domains. The use of multiple power domains maximizes flexibility, while maintaining compliance with industry standards and conventions. By isolating the internal logic of the processor into its own power domain, separate from the RTC and other I/O, the processor can take advantage of dynamic power management without affecting the RTC or other I/O devices. There are no sequencing requirements for the various power domains.

Table 5. Power Domains

Power Domain	V_{DD} Range
All internal logic, except RTC	V_{DDINT}
RTC internal logic and crystal I/O	V_{DDRTC}
All other I/O	V_{DDEXT}

The power dissipated by a processor is largely a function of the clock frequency of the processor and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic.

The dynamic power management feature of the processor allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The savings in power dissipation can be modeled using the power savings factor and % power savings calculations.

The power savings factor is calculated as:

$$\textit{power savings factor} = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{t_{RED}}{t_{NOM}}\right)$$

where the variables in the equation are:

$f_{CCLKNOM}$ is the nominal core clock frequency

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage

$V_{DDINTRED}$ is the reduced internal supply voltage

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *“Analog Devices JTAG Emulation Technical Reference”* (EE-68) on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started With Blackfin Processors*
- *ADSP-BF533 Blackfin Processor Hardware Reference*
- *Blackfin Processor Programming Reference*
- *ADSP-BF531/ADSP-BF532/ADSP-BF533 Blackfin Processor Anomaly List*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

SPECIFICATIONS

Component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 400 MHz and 500 MHz speed grade models[2]	0.8	1.2	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 533 MHz speed grade models[2]	0.8	1.25	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	600 MHz speed grade models[2]	0.8	1.30	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	Automotive 400 MHz speed grade models[2]	0.95	1.2	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	Automotive 533 MHz speed grade models[2]	0.95	1.25	1.45	V
V_{DDEXT}	External Supply Voltage[3]	Nonautomotive grade models[2]	1.75	1.8/3.3	3.6	V
V_{DDEXT}	External Supply Voltage	Automotive grade models[2]	2.7	3.3	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage	Nonautomotive grade models[2]	1.75	1.8/3.3	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage	Automotive grade models[2]	2.7	3.3	3.6	V
V_{IH}	High Level Input Voltage[4, 5]	V_{DDEXT} = 1.85 V	1.3			V
V_{IH}	High Level Input Voltage[4, 5]	V_{DDEXT} = Maximum	2.0			V
$V_{IHCLKIN}$	High Level Input Voltage[6]	V_{DDEXT} = Maximum	2.2			V
V_{IL}	Low Level Input Voltage[7]	V_{DDEXT} = 1.75 V			+0.3	V
V_{IL}	Low Level Input Voltage[7]	V_{DDEXT} = 2.7 V			+0.6	V
T_J	Junction Temperature	160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = 0°C to +70°C	0		+95	°C
T_J	Junction Temperature	160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C
T_J	Junction Temperature	169-Ball Plastic Ball Grid Array (PBGA) @ $T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C
T_J	Junction Temperature	169-Ball Plastic Ball Grid Array (PBGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	176-Lead Quad Flatpack (LQFP) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+100	°C

[1] The regulator can generate V_{DDINT} at levels of 0.85 V to 1.2 V with –5% to +10% tolerance, 1.25 V with –4% to +10% tolerance, and 1.3 V with –0% to +10% tolerance.

[2] See Ordering Guide on Page 63.

[3] When V_{DDEXT} < 2.25 V, on-chip voltage regulation is not supported.

[4] Applies to all input and bidirectional pins except CLKIN.

[5] The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are 3.3 V tolerant (always accepts up to 3.6 V maximum V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}, because V_{OH} (maximum) approximately equals V_{DDEXT} (maximum). This 3.3 V tolerance applies to bidirectional pins (DATA15–0, TMR2–0, PF15–0, PPI3–0, RSCLK1–0, TSCLK1–0, RFS1–0, TFS1–0, MOSI, MISO, SCK) and input only pins ($\overline{BR}$, ARDY, PPI_CLK, DR0PRI, DR0SEC, DR1PRI, DR1SEC, RX, RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, NMI, and BMODE1–0).

[6] Applies to CLKIN pin only.

[7] Applies to all input and bidirectional pins.

The following three tables describe the voltage/frequency requirements for the processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock (Table 10 and Table 11) and system clock (Table 13) specifications. Table 12 describes phase-locked loop operating conditions.

Table 10. Core Clock (CCLK) Requirements—500 MHz, 533 MHz, and 600 MHz Models

Parameter		Internal Regulator Setting	Max	Unit
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.3 V Minimum)[1]	1.30 V	600	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.2 V Minimum)[2]	1.25 V	533	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.14 V Minimum)[3]	1.20 V	500	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	444	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	400	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V	333	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V	250	MHz

[1] Applies to 600 MHz models only. See Ordering Guide on Page 63.
[2] Applies to 533 MHz and 600 MHz models only. See Ordering Guide on Page 63. 533 MHz models cannot support internal regulator levels above 1.25 V.
[3] Applies to 500 MHz, 533 MHz, and 600 MHz models. See Ordering Guide on Page 63. 500 MHz models cannot support internal regulator levels above 1.20 V.

Table 11. Core Clock (CCLK) Requirements—400 MHz Models[1]

Parameter		Internal Regulator Setting	T_J = 125°C Max	All[2] Other T_J Max	Unit
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	400	400	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	333	364	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	295	333	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V		280	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V		250	MHz

[1] See Ordering Guide on Page 63.
[2] See Operating Conditions on Page 20.

Table 12. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	50	Max f_{CCLK}	MHz

Table 13. System Clock (SCLK) Requirements

Parameter[1]		V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
CSP_BGA/PBGA				
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} \geq$ 1.14 V)	100	133	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.14 V)	100	100	MHz
LQFP				
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} \geq$ 1.14 V)	100	133	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.14 V)	83	83	MHz

[1] t_{SCLK} (= $1/f_{SCLK}$) must be greater than or equal to t_{CCLK}.

[5] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{TRST}$).
[6] Absolute value.
[7] Applies to three-statable pins.
[8] Applies to all signal pins.
[9] Guaranteed, but not tested.
[10] See the *ADSP-BF533 Blackfin Processor Hardware Reference Manual* for definitions of sleep, deep sleep, and hibernate operating modes.
[11] See Table 16 for the list of I_{DDINT} power vectors covered by various Activity Scaling Factors (ASF).

System designers should refer to *Estimating Power for the ADSP-BF531/BF532/BF533 Blackfin Processors (EE-229)*, which provides detailed information for optimizing designs for lowest power. All topics discussed in this section are described in detail in EE-229. Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 22 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 14 or Table 15), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 17).

The dynamic component is also subject to an Activity Scaling Factor (ASF) which represents application code running on the processor (Table 16).

Table 14. Static Current–500 MHz, 533 MHz, and 600 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})[2]														
T_J (°C)[2]	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V	1.45 V
–45	4.3	5.3	5.9	7.0	8.2	9.8	11.2	13.0	15.2	17.7	20.2	21.6	25.5	30.1	32.0
0	18.8	21.3	24.1	27.8	31.6	35.6	40.1	45.3	51.4	58.1	65.0	68.5	78.4	89.8	94.3
25	35.3	39.9	45.0	50.9	57.3	64.4	72.9	80.9	90.3	101.4	112.1	118.0	133.7	151.6	158.7
40	52.3	58.5	65.1	73.3	81.3	90.9	101.2	112.5	125.5	138.7	154.4	160.6	180.6	203.1	212.0
55	73.6	82.5	92.0	102.7	114.4	126.3	141.2	155.7	172.7	191.1	212.1	220.8	247.6	277.7	289.5
70	100.8	112.5	124.5	137.4	152.6	168.4	186.5	205.4	227.0	250.3	276.2	287.1	320.4	357.4	371.9
85	133.3	148.5	164.2	180.5	198.8	219.0	241.0	264.5	290.6	319.7	350.2	364.6	404.9	449.7	467.2
100	178.3	196.3	216.0	237.6	259.9	284.6	311.9	342.0	373.1	408.0	446.1	462.6	511.1	564.7	585.6
115	223.3	245.9	270.2	295.7	323.5	353.3	386.1	421.1	460.1	500.9	545.0	566.5	624.3	688.1	712.8
125	278.5	305.8	334.1	364.3	397.4	432.4	470.6	509.3	553.4	600.6	652.1	676.5	742.1	814.1	841.9

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 20.

Table 15. Static Current–400 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})[2]											
T_J (°C)[2]	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V
–45	0.9	1.1	1.3	1.5	1.8	2.2	2.6	3.1	3.8	4.4	5.0	5.4
0	3.3	3.7	4.2	4.8	5.5	6.3	7.2	8.1	8.9	10.1	11.2	11.9
25	7.5	8.4	9.4	10.0	11.2	12.6	14.1	15.5	17.2	19.0	21.2	21.9
40	12.0	13.1	14.3	15.9	17.4	19.4	21.5	23.5	25.8	28.1	30.8	32.0
55	18.3	20.0	21.9	23.6	26.0	28.2	30.8	33.7	36.8	39.8	43.4	45.0
70	27.7	30.3	32.6	35.3	38.2	41.7	45.2	49.0	52.8	57.6	62.4	64.2
85	38.2	41.7	44.9	48.6	52.7	57.3	61.7	66.7	72.0	77.5	83.9	86.5
100	54.1	58.1	63.2	67.8	73.2	78.8	84.9	91.5	98.4	106.0	113.8	117.2
115	73.9	80.0	86.3	91.9	99.1	106.6	114.1	122.4	131.1	140.9	151.1	155.5
125	98.7	106.3	113.8	122.1	130.8	140.2	149.7	160.4	171.9	183.8	197.0	202.4

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 20.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 18 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Table 18. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.45 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.5 V to +3.8 V
Input Voltage[1, 2]	–0.5 V to +3.8 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	125°C

[1] Applies to 100% transient duty cycle. For other duty cycles see Table 19.
[2] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2 V.

Table 19. Maximum Duty Cycle for Input Transient Voltage[1]

V_{IN} Min (V)[2]	V_{IN} Max (V)[2]	Maximum Duty Cycle[3]
–0.50	+3.80	100%
–0.70	+4.00	40%
–0.80	+4.10	25%
–0.90	+4.20	15%
–1.00	+4.30	10%

[1] Applies to all signal pins with the exception of CLKIN, XTAL, VROUT1–0.
[2] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.
[3] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Parallel Peripheral Interface Timing

Table 27 and Figure 17 through Figure 22 describe parallel peripheral interface operations.

Table 27. Parallel Peripheral Interface Timing

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Timing Requirements								
t_{PCLKW}	PPI_CLK Width	8.0		8.0		6.0		ns
t_{PCLK}	PPI_CLK Period[1]	20.0		20.0		15.0		ns
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK Edge (Nonsampling Edge for Rx, Sampling Edge for Tx)	6.0		6.0		4.0[2]		ns ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.0[2]		1.0[2]		1.0[2]		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	3.5		3.5		3.5		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	1.5		1.5		1.5		ns
Switching Characteristics—GP Output and Frame Capture Modes								
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		11.0		8.0		8.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	1.7		1.7		1.7		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		11.0		9.0		9.0	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	1.8		1.8		1.8		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$.
[2] Applies when PPI_CONTROL Bit 8 is cleared. See Figure 19 and Figure 22.

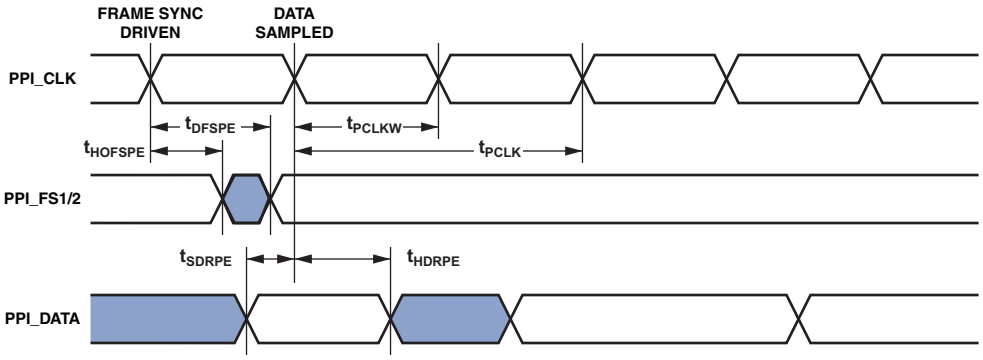

Figure 17. PPI GP Rx Mode with Internal Frame Sync Timing

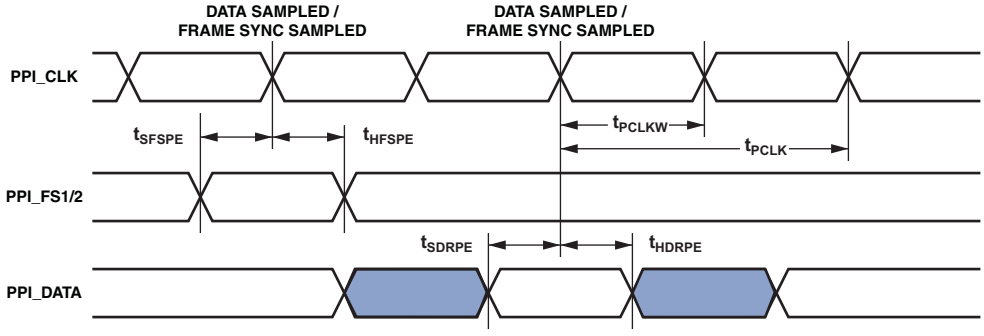

Figure 18. PPI GP Rx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 1)

Table 30. Serial Ports—Enable and Three-State

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Switching Characteristics						
t_{DTENE}	Data Enable Delay from External TSCLKx[1]	0		0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx[1, 2, 3]		10.0		10.0	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx[1]	−2.0		−2.0		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx[1, 2, 3]		3.0		3.0	ns

[1] Referenced to drive edge.
[2] Applicable to multichannel mode only.
[3] TSCLKx is tied to RSCLKx.

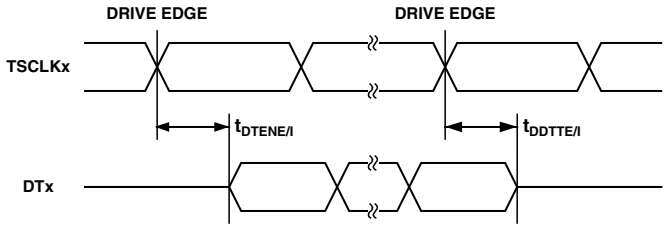

Figure 25. Enable and Three-State

Serial Peripheral Interface (SPI) Port—Master Timing

Table 32. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Timing Requirements								
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	10.5		9		7.5		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	–1.5		–1.5		–1.5		ns
Switching Characteristics								
t_{SDSCIM}	$\overline{SPISELx}$ Low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISELx}$ High	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)		6		6		6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	–1.0		–1.0		–1.0		ns

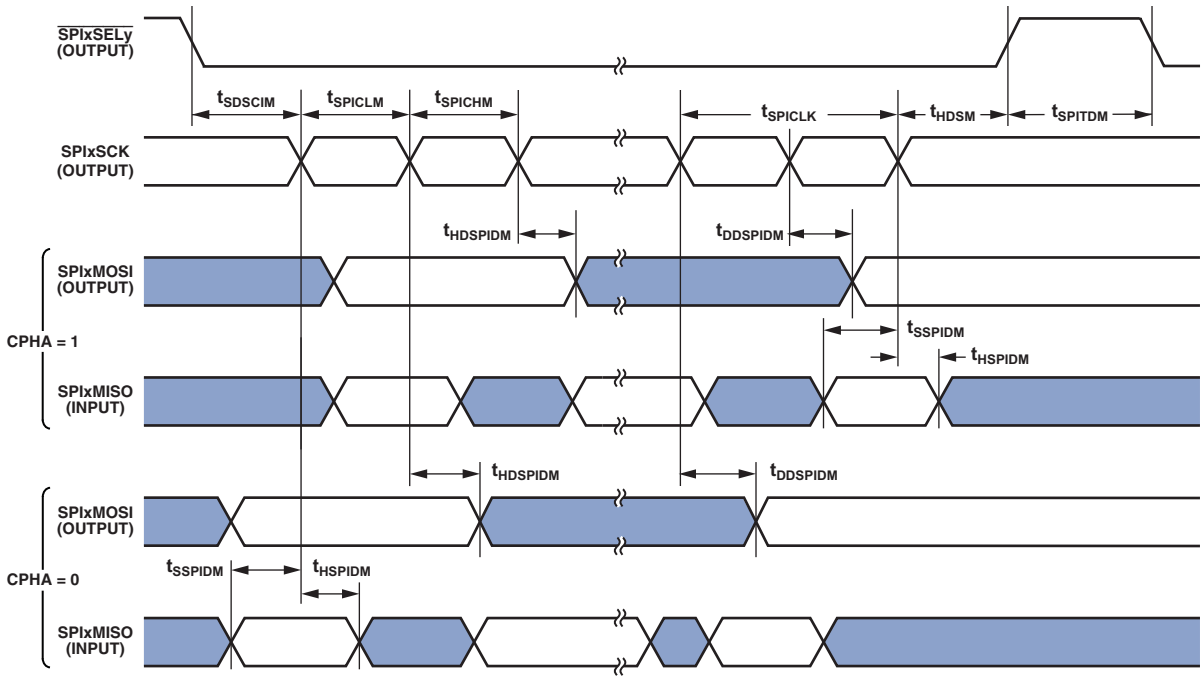

Figure 27. Serial Peripheral Interface (SPI) Port—Master Timing

General-Purpose I/O Port F Pin Cycle Timing

Table 34. General-Purpose I/O Port F Pin Cycle Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirement						
t_{WFI}	GPIO Input Pulse Width	t_{SCLK} + 1		t_{SCLK} + 1		ns
Switching Characteristic						
t_{GPOD}	GPIO Output Delay from CLKOUT Low		6		6	ns

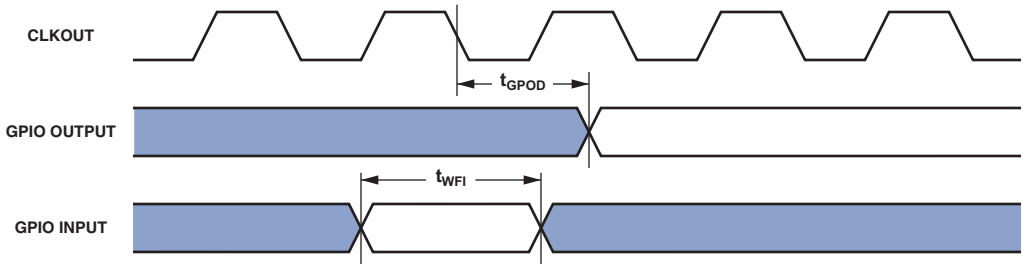

Figure 29. GPIO Cycle Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

For information on the UART port receive and transmit operations, see the *ADSP-BF533 Blackfin Processor Hardware Reference*.

OUTPUT DRIVE CURRENTS

Figure 33 through Figure 44 show typical current-voltage characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

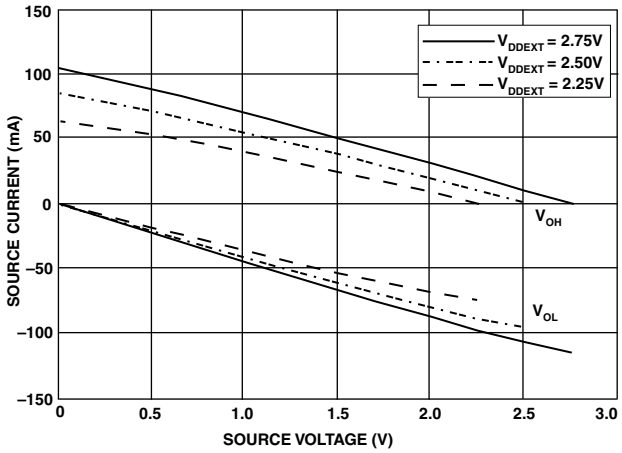

Figure 33. Drive Current A (V_{DDEXT} = 2.5 V)

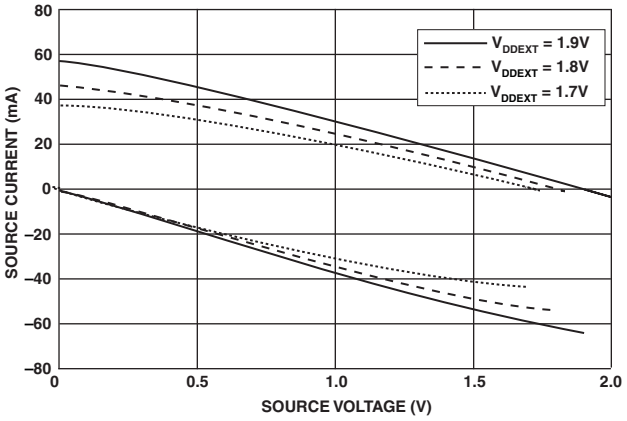

Figure 34. Drive Current A (V_{DDEXT} = 1.8 V)

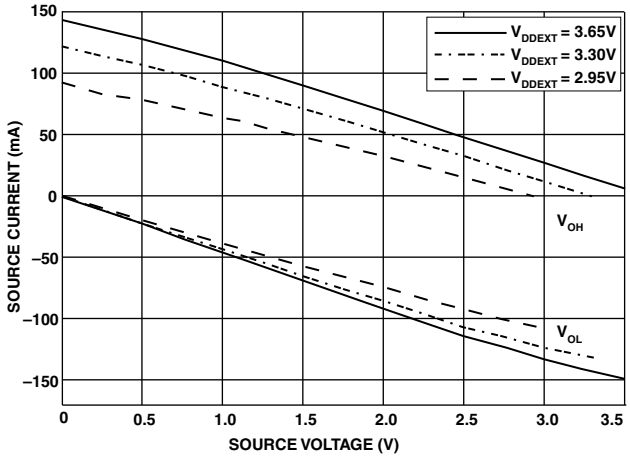

Figure 35. Drive Current A (V_{DDEXT} = 3.3 V)

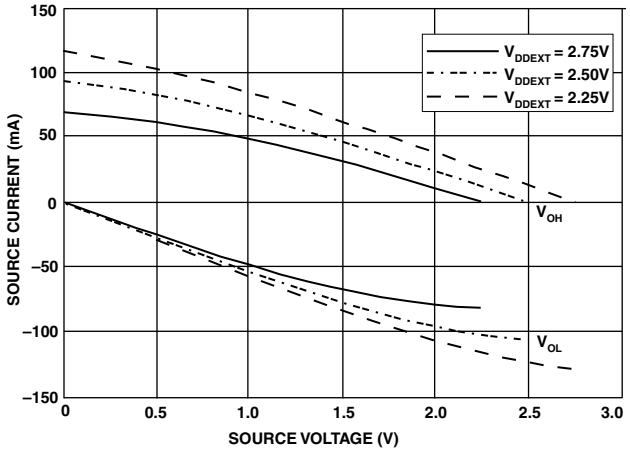

Figure 36. Drive Current B (V_{DDEXT} = 2.5 V)

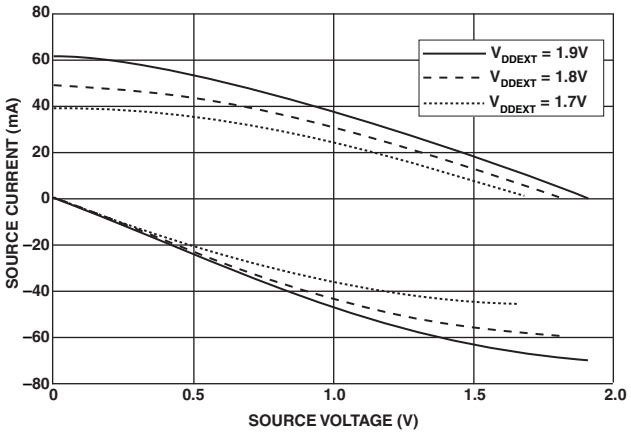

Figure 37. Drive Current B (V_{DDEXT} = 1.8 V)

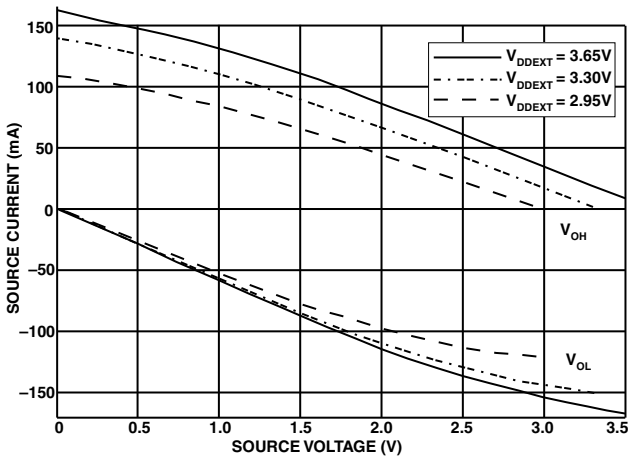

Figure 38. Drive Current B (V_{DDEXT} = 3.3 V)

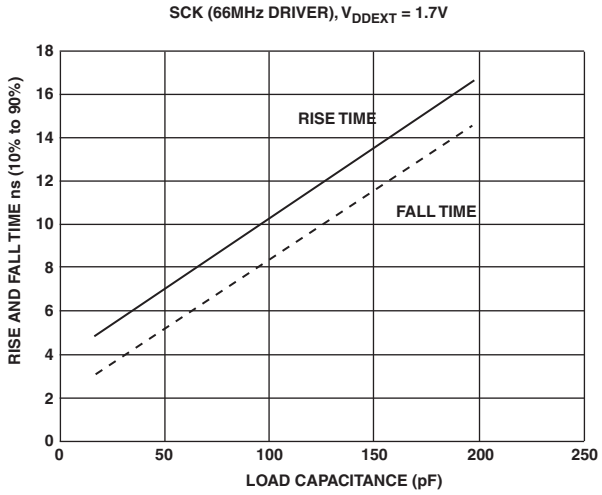

Figure 57. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at V_{DDEXT} = 1.75 V

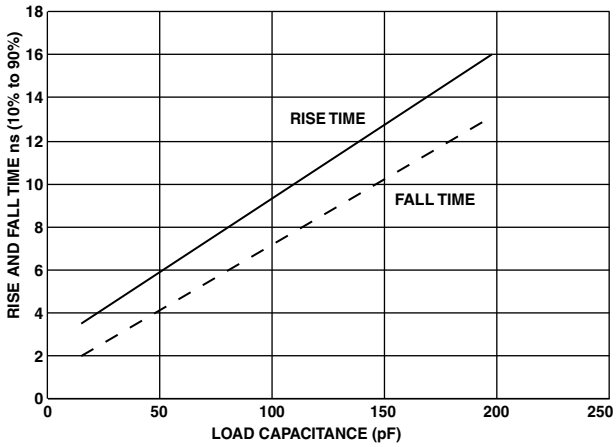

Figure 58. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at V_{DDEXT} = 2.25 V

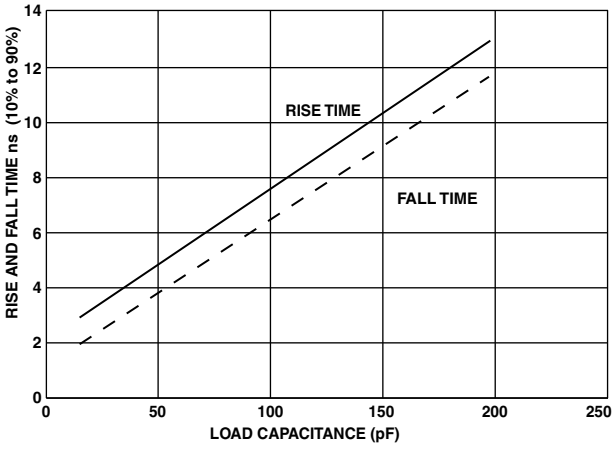

Figure 59. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at V_{DDEXT} = 3.65 V

Table 44. 169-Ball PBGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	PF4	D16	CLKOUT	J2	RSCLK1	M12	VDD	U9	DATA9
A2	PF5	D17	$\overline{\text{AMS0}}$	J6	V_{DDEXT}	M16	ADDR7	U10	DATA7
A3	PF7	E1	MOSI	J7	GND	M17	ADDR8	U11	DATA5
A4	PF9	E2	MISO	J8	GND	N1	RFS0	U12	DATA4
A5	PF11	E16	$\overline{\text{AMS1}}$	J9	GND	N2	RSCLK0	U13	DATA2
A6	PF12	E17	$\overline{\text{AMS2}}$	J10	GND	N16	ADDR10	U14	DATA0
A7	PF14	F1	DT1PRI	J11	GND	N17	ADDR9	U15	ADDR16
A8	PPI3	F2	DT1SEC	J12	VDD	P1	TMR2	U16	ADDR18
A9	PPI1	F6	V_{DDEXT}	J16	ADDR1	P2	TMR1	U17	$\overline{\text{BGH}}$
A10	RTXI	F7	V_{DDEXT}	J17	ADDR2	P16	ADDR12		
A11	RTXO	F8	V_{DDEXT}	K1	DT0SEC	P17	ADDR11		
A12	$\overline{\text{RESET}}$	F9	V_{DDEXT}	K2	DT0PRI	R1	TMR0		
A13	XTAL	F10	RTCVDD	K6	V_{DDEXT}	R2	TX		
A14	CLKIN	F11	GND	K7	GND	R16	ADDR14		
A15	$\overline{\text{SRAS}}$	F12	VDD	K8	GND	R17	ADDR13		
A16	$\overline{\text{SCAS}}$	F16	$\overline{\text{AMS3}}$	K9	GND	T1	RX		
A17	$\overline{\text{SMS}}$	F17	$\overline{\text{AOE}}$	K10	GND	T2	V_{DDEXT}		
B1	PF2	G1	TSCLK1	K11	GND	T3	TMS		
B2	V_{DDEXT}	G2	TFS1	K12	VDD	T4	TDO		
B3	PF6	G6	V_{DDEXT}	K16	ADDR3	T5	BMODE1		
B4	PF8	G7	GND	K17	ADDR4	T6	DATA15		
B5	PF10	G8	GND	L1	TFS0	T7	DATA13		
B6	PF13	G9	GND	L2	TSCLK0	T8	DATA10		
B7	PF15	G10	GND	L6	V_{DDEXT}	T9	DATA8		
B8	PPI2	G11	GND	L7	GND	T10	DATA6		
B9	PPI0	G12	VDD	L8	GND	T11	DATA3		
B10	PPI_CLK	G16	$\overline{\text{ARE}}$	L9	GND	T12	DATA1		
B11	NMI	G17	$\overline{\text{AWE}}$	L10	GND	T13	$\overline{\text{BG}}$		
B12	VROUT0	H1	DR1PRI	L11	GND	T14	ADDR19		
B13	VROUT1	H2	DR1SEC	L12	VDD	T15	ADDR17		
B14	SCKE	H6	V_{DDEXT}	L16	ADDR5	T16	GND		
B15	SA10	H7	GND	L17	ADDR6	T17	ADDR15		
B16	GND	H8	GND	M1	DR0SEC	U1	$\overline{\text{EMU}}$		
B17	$\overline{\text{SWE}}$	H9	GND	M2	DR0PRI	U2	$\overline{\text{TRST}}$		
C1	PF1	H10	GND	M6	V_{DDEXT}	U3	TDI		
C2	PF3	H11	GND	M7	V_{DDEXT}	U4	TCK		
C16	ARDY	H12	VDD	M8	V_{DDEXT}	U5	BMODE0		
C17	$\overline{\text{BR}}$	H16	$\overline{\text{ABE0}}$	M9	GND	U6	DATA14		
D1	SCK	H17	$\overline{\text{ABE1}}$	M10	VDD	U7	DATA12		
D2	PF0	J1	RFS1	M11	VDD	U8	DATA11		

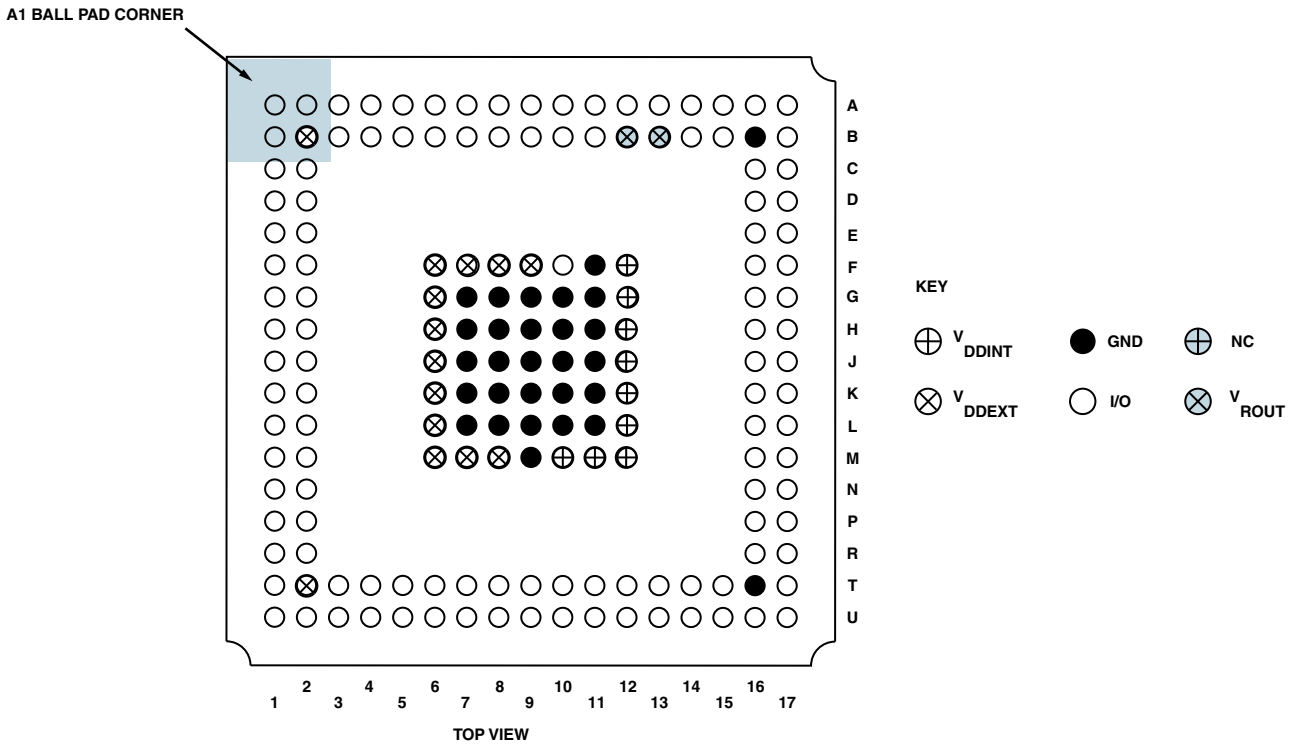

Figure 62. 169-Ball PBGA Ground Configuration (Top View)

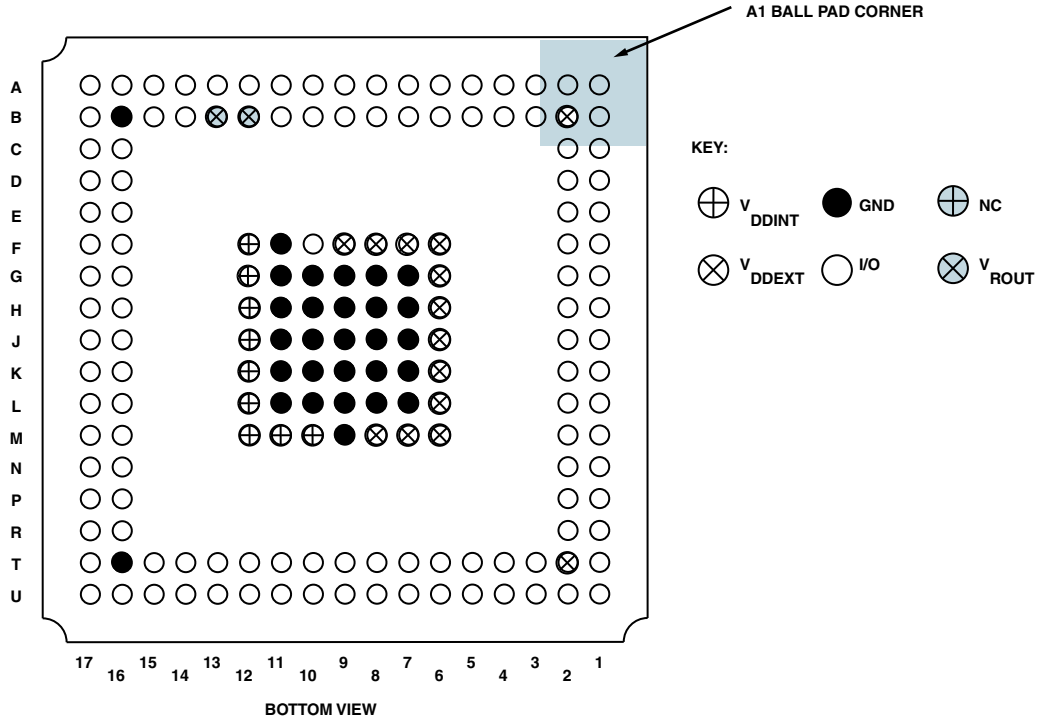

Figure 63. 169-Ball PBGA Ground Configuration (Bottom View)

176-LEAD LQFP PINOUT

Table 45 lists the LQFP pinout by signal. Table 46 on Page 57 lists the LQFP pinout by lead number.

Table 45. 176-Lead LQFP Pin Assignment (Alphabetical by Signal)

Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.
$\overline{ABE0}$	151	DATA3	113	GND	88	PPI_CLK	21	V_{DDEXT}	71
$\overline{ABE1}$	150	DATA4	112	GND	89	PPI0	22	V_{DDEXT}	93
ADDR1	149	DATA5	110	GND	90	PPI1	23	V_{DDEXT}	107
ADDR2	148	DATA6	109	GND	91	PPI2	24	V_{DDEXT}	118
ADDR3	147	DATA7	108	GND	92	PPI3	26	V_{DDEXT}	134
ADDR4	146	DATA8	105	GND	97	$\overline{RESET}$	13	V_{DDEXT}	145
ADDR5	142	DATA9	104	GND	106	RFS0	75	V_{DDEXT}	156
ADDR6	141	DATA10	103	GND	117	RFS1	64	V_{DDEXT}	171
ADDR7	140	DATA11	102	GND	128	RSCLK0	76	V_{DDINT}	25
ADDR8	139	DATA12	101	GND	129	RSCLK1	65	V_{DDINT}	52
ADDR9	138	DATA13	100	GND	130	RTXI	17	V_{DDINT}	66
ADDR10	137	DATA14	99	GND	131	RTXO	16	V_{DDINT}	80
ADDR11	136	DATA15	98	GND	132	RX	82	V_{DDINT}	111
ADDR12	135	DR0PRI	74	GND	133	SA10	164	V_{DDINT}	143
ADDR13	127	DR0SEC	73	GND	144	$\overline{SCAS}$	166	V_{DDINT}	157
ADDR14	126	DR1PRI	63	GND	155	SCK	53	V_{DDINT}	168
ADDR15	125	DR1SEC	62	GND	170	SCKE	173	V_{DDRTC}	18
ADDR16	124	DT0PRI	68	GND	174	$\overline{SMS}$	172	VROUT0	5
ADDR17	123	DT0SEC	67	GND	175	$\overline{SRAS}$	167	VROUT1	4
ADDR18	122	DT1PRI	59	GND	176	$\overline{SWE}$	165	XTAL	11
ADDR19	121	DT1SEC	58	MISO	54	TCK	94		
$\overline{AMS0}$	161	$\overline{EMU}$	83	MOSI	55	TDI	86		
$\overline{AMS1}$	160	GND	1	NMI	14	TDO	87		
$\overline{AMS2}$	159	GND	2	PF0	51	TFS0	69		
$\overline{AMS3}$	158	GND	3	PF1	50	TFS1	60		
$\overline{AOE}$	154	GND	7	PF2	49	TMR0	79		
ARDY	162	GND	8	PF3	48	TMR1	78		
$\overline{ARE}$	153	GND	9	PF4	47	TMR2	77		
$\overline{AWE}$	152	GND	15	PF5	46	TMS	85		
$\overline{BG}$	119	GND	19	PF6	38	$\overline{TRST}$	84		
$\overline{BGH}$	120	GND	30	PF7	37	TSCLK0	72		
BMODE0	96	GND	39	PF8	36	TSCLK1	61		
BMODE1	95	GND	40	PF9	35	TX	81		
$\overline{BR}$	163	GND	41	PF10	34	V_{DDEXT}	6		
CLKIN	10	GND	42	PF11	33	V_{DDEXT}	12		
CLKOUT	169	GND	43	PF12	32	V_{DDEXT}	20		
DATA0	116	GND	44	PF13	29	V_{DDEXT}	31		
DATA1	115	GND	56	PF14	28	V_{DDEXT}	45		
DATA2	114	GND	70	PF15	27	V_{DDEXT}	57		

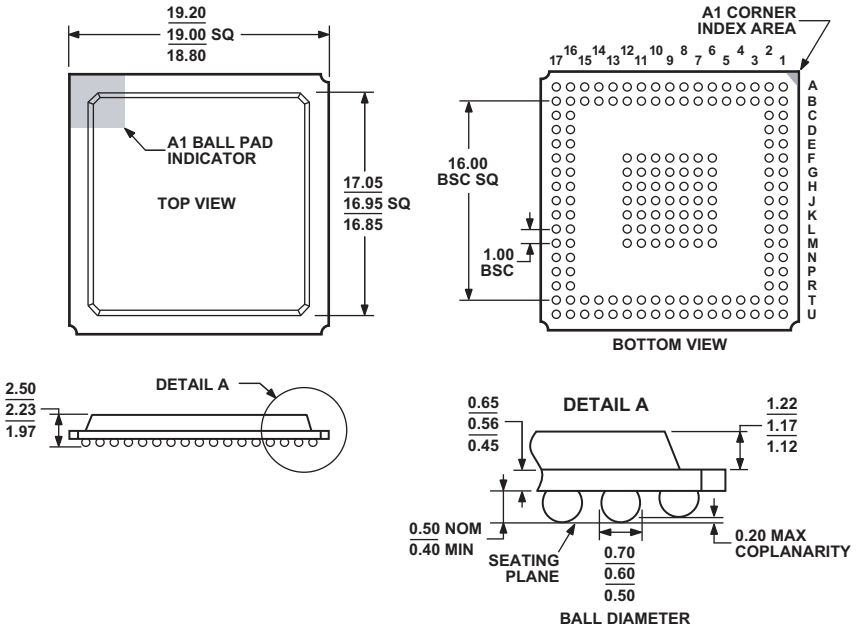

Figure 66. 169-Ball Plastic Ball Grid Array [PBGA]
(B-169)
Dimensions shown in millimeters

AUTOMOTIVE PRODUCTS

The ADBF531W, ADBF532W, and ADBF533W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 48 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 48. Automotive Products

Product Family[1,2]	Temperature Range[3]	Speed Grade (Max)	Package Description	Package Option
ADBF531WBSTZ4xx	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADBF531WBBCZ4xx	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF531WYBCZ4xx	–40°C to +105°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF532WBSTZ4xx	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADBF532WBBCZ4xx	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF532WYBCZ4xx	–40°C to +105°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF533WBBCZ5xx	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADBF533WBBZ5xx	–40°C to +85°C	533 MHz	169-Ball PBGA	B-169
ADBF533WYBCZ4xx	–40°C to +105°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF533WYBBZ4xx	–40°C to +105°C	400 MHz	169-Ball PBGA	B-169

[1] Z = RoHS compliant part.
[2] xx denotes silicon revision.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 20 for junction temperature (T_J) specification which is the only temperature specification.