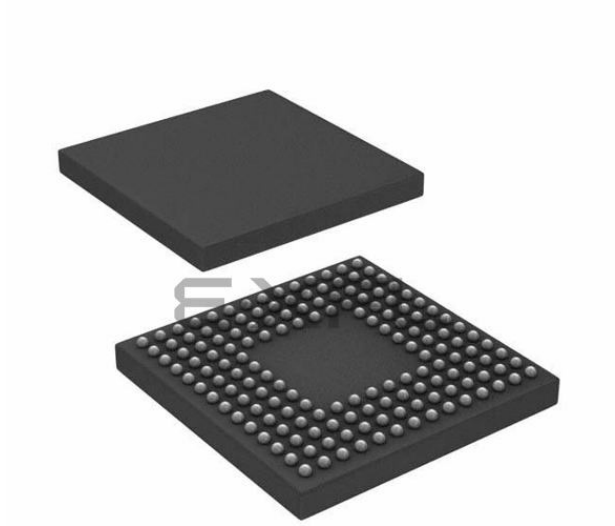

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	400MHz
Non-Volatile Memory	ROM (1kB)
On-Chip RAM	52kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LFBGA, CSPBGA
Supplier Device Package	160-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf531sbbc400

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REVISION HISTORY

8/13— Rev. H to Rev. I

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Updated Ordering Guide 63

PFx pins defined as inputs can be configured to generate hardware interrupts, while output PFx pins can be triggered by software interrupts.

- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual PFx pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

PARALLEL PERIPHERAL INTERFACE

The processors provide a parallel peripheral interface (PPI) that can connect directly to parallel ADCs and DACs, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bi-directional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bi-directional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications.

Three distinct sub modes are supported:

- Input mode – Frame syncs and data are inputs into the PPI.
- Frame capture mode – Frame syncs are outputs from the PPI, but data are inputs.
- Output mode – Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (e.g., for frame capture). The processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct sub modes are supported:

- Active video only mode
- Vertical blanking only mode
- Entire field mode

Active Video Only Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that can be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

DYNAMIC POWER MANAGEMENT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provides four operating modes, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

t_{NOM} is the duration running at $f_{CCLKNOM}$

t_{RED} is the duration running at $f_{CCLKRED}$

The percent power savings is calculated as:

$$\%\ power\ savings\ =\ (1 - power\ savings\ factor) \times 100\%$$

VOLTAGE REGULATION

The Blackfin processor provides an on-chip voltage regulator that can generate appropriate V_{DDINT} voltage levels from the V_{DDEXT} supply. See Operating Conditions on Page 20 for regulator tolerances and acceptable V_{DDEXT} ranges for specific models.

Figure 7 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power (V_{DDEXT}) supplied. While in the hibernate state, I/O power is still being applied, eliminating the need for external buffers. The voltage regulator can be activated from this power-down state either through an RTC wakeup or by asserting $\overline{\text{RESET}}$, both of which initiate a boot sequence. The regulator can also be disabled and bypassed at the user's discretion.

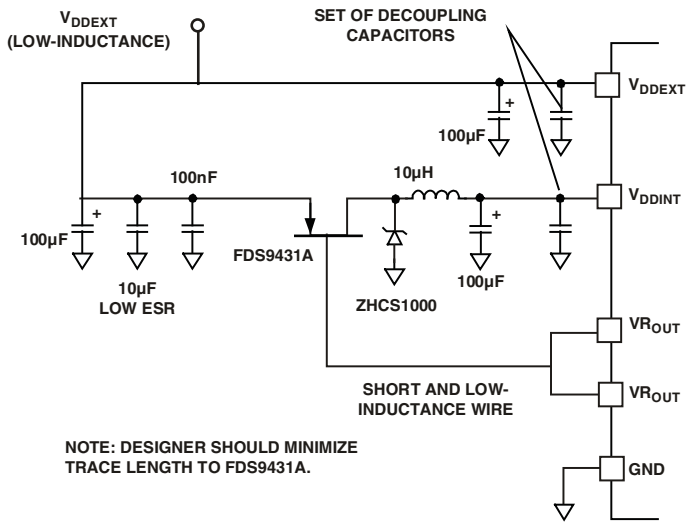


Figure 7. Voltage Regulator Circuit

Voltage Regulator Layout Guidelines

Regulator external component placement, board routing, and bypass capacitors all have a significant effect on noise injected into the other analog circuits on-chip. The VROUT1–0 traces and voltage regulator external components should be considered as noise sources when doing board layout and should not be routed or placed near sensitive circuits or components on the board. All internal and I/O power supplies should be well bypassed with bypass capacitors placed as close to the processors as possible.

For further details on the on-chip voltage regulator and related board design guidelines, see the *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228)* applications note on the Analog Devices web site (www.analog.com)—use site search on "EE-228".

CLOCK SIGNALS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the processors include an on-chip oscillator circuit, an external crystal can be used. For fundamental frequency operation, use the circuit shown in Figure 8.

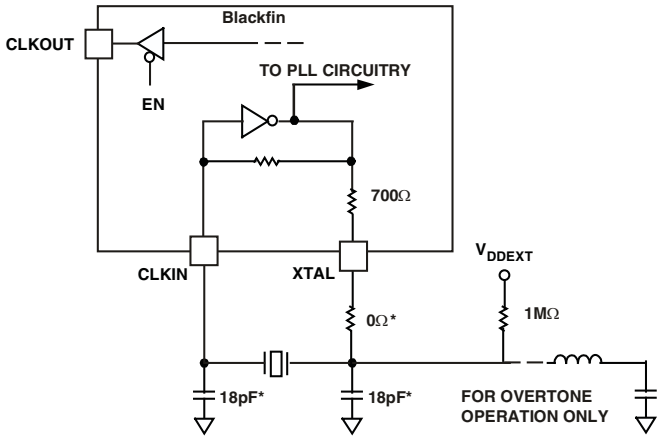


Figure 8. External Crystal Connections

A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor shown in Figure 8 fine tune the phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 8 are typical values only. The capacitor values are dependent upon the crystal manufacturer's load capacitance recommendations and the physical PCB layout. The resistor value depends on the drive level specified by the crystal manufacturer. System designs should verify the customized values based on careful investigation on multiple devices over the allowed temperature range.

A third-overtone crystal can be used at frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 8.

PIN DESCRIPTIONS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors pin definitions are listed in Table 9.

All pins are three-stated during and immediately after reset, except the memory interface, asynchronous memory control, and synchronous memory control pins. These pins are all driven high, with the exception of CLKOUT, which toggles at the system clock rate. During hibernate, all outputs are three-stated unless otherwise noted in Table 9.

If $\overline{BR}$ is active (whether or not $\overline{RESET}$ is asserted), the memory pins are also three-stated. All unused I/O pins have their input buffers disabled with the exception of the pins that need pull-ups or pull-downs as noted in the table.

In order to maintain maximum functionality and reduce package size and pin count, some pins have dual, multiplexed functionality. In cases where pin functionality is reconfigurable, the default state is shown in plain text, while alternate functionality is shown in italics.

Table 9. Pin Descriptions

Pin Name	Type	Function	Driver Type[1]
Memory Interface			
ADDR19–1	O	Address Bus for Async/Sync Access	A
DATA15–0	I/O	Data Bus for Async/Sync Access	A
$\overline{ABE1–0}$/SDQM1–0	O	Byte Enables/Data Masks for Async/Sync Access	A
$\overline{BR}$	I	Bus Request (This pin should be pulled high if not used.)	
$\overline{BG}$	O	Bus Grant	A
$\overline{BGH}$	O	Bus Grant Hang	A
Asynchronous Memory Control			
$\overline{AMS3–0}$	O	Bank Select (Require pull-ups if hibernate is used.)	A
ARDY	I	Hardware Ready Control (This pin should be pulled high if not used.)	
$\overline{AOE}$	O	Output Enable	A
$\overline{ARE}$	O	Read Enable	A
$\overline{AWE}$	O	Write Enable	A
Synchronous Memory Control			
$\overline{SRAS}$	O	Row Address Strobe	A
$\overline{SCAS}$	O	Column Address Strobe	A
$\overline{SWE}$	O	Write Enable	A
SCKE	O	Clock Enable (Requires pull-down if hibernate is used.)	A
CLKOUT	O	Clock Output	B
SA10	O	A10 Pin	A
$\overline{SMS}$	O	Bank Select	A
Timers			
TMR0	I/O	Timer 0	C
TMR1/*PPI_FS1*	I/O	Timer 1/*PPI Frame Sync1*	C
TMR2/*PPI_FS2*	I/O	Timer 2/*PPI Frame Sync2*	C
PPI Port			
PPI3–0	I/O	PPI3–0	C
PPI_CLK/*TMRCLK*	I	PPI Clock/*External Timer Reference*	

Table 9. Pin Descriptions (Continued)

Pin Name	Type	Function	Driver Type[1]
RFS1	I/O	SPORT1 Receive Frame Sync	C
DR1PRI	I	SPORT1 Receive Data Primary	
DR1SEC	I	SPORT1 Receive Data Secondary	
TSCLK1	I/O	SPORT1 Transmit Serial Clock	D
TFS1	I/O	SPORT1 Transmit Frame Sync	C
DT1PRI	O	SPORT1 Transmit Data Primary	C
DT1SEC	O	SPORT1 Transmit Data Secondary	C
UART Port			
RX	I	UART Receive	
TX	O	UART Transmit	C
Real-Time Clock			
RTXI	I	RTC Crystal Input (This pin should be pulled low when not used.)	
RTXO	O	RTC Crystal Output (Does not three-state in hibernate.)	
Clock			
CLKIN	I	Clock/Crystal Input (This pin needs to be at a level or clocking.)	
XTAL	O	Crystal Output	
Mode Controls			
$\overline{\text{RESET}}$	I	Reset (This pin is always active during core power-on.)	
NMI	I	Nonmaskable Interrupt (This pin should be pulled low when not used.)	
BMODE1–0	I	Boot Mode Strap (These pins must be pulled to the state required for the desired boot mode.)	
Voltage Regulator			
VROUT1–0	O	External FET Drive (These pins should be left unconnected when unused and are driven high during hibernate.)	
Supplies			
V_{DDEXT}	P	I/O Power Supply	
V_{DDINT}	P	Core Power Supply	
V_{DDRTC}	P	Real-Time Clock Power Supply (This pin should be connected to V_{DDEXT} when not used and should remain powered at all times.)	
GND	G	External Ground	

[1] Refer to Figure 33 on Page 43 to Figure 44 on Page 44.

SPECIFICATIONS

Component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 400 MHz and 500 MHz speed grade models[2]	0.8	1.2	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 533 MHz speed grade models[2]	0.8	1.25	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	600 MHz speed grade models[2]	0.8	1.30	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	Automotive 400 MHz speed grade models[2]	0.95	1.2	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	Automotive 533 MHz speed grade models[2]	0.95	1.25	1.45	V
V_{DDEXT}	External Supply Voltage[3]	Nonautomotive grade models[2]	1.75	1.8/3.3	3.6	V
V_{DDEXT}	External Supply Voltage	Automotive grade models[2]	2.7	3.3	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage	Nonautomotive grade models[2]	1.75	1.8/3.3	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage	Automotive grade models[2]	2.7	3.3	3.6	V
V_{IH}	High Level Input Voltage[4, 5]	V_{DDEXT} = 1.85 V	1.3			V
V_{IH}	High Level Input Voltage[4, 5]	V_{DDEXT} = Maximum	2.0			V
$V_{IHCLKIN}$	High Level Input Voltage[6]	V_{DDEXT} = Maximum	2.2			V
V_{IL}	Low Level Input Voltage[7]	V_{DDEXT} = 1.75 V			+0.3	V
V_{IL}	Low Level Input Voltage[7]	V_{DDEXT} = 2.7 V			+0.6	V
T_J	Junction Temperature	160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = 0°C to +70°C	0		+95	°C
T_J	Junction Temperature	160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C
T_J	Junction Temperature	169-Ball Plastic Ball Grid Array (PBGA) @ $T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C
T_J	Junction Temperature	169-Ball Plastic Ball Grid Array (PBGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	176-Lead Quad Flatpack (LQFP) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+100	°C

[1] The regulator can generate V_{DDINT} at levels of 0.85 V to 1.2 V with –5% to +10% tolerance, 1.25 V with –4% to +10% tolerance, and 1.3 V with –0% to +10% tolerance.

[2] See Ordering Guide on Page 63.

[3] When V_{DDEXT} < 2.25 V, on-chip voltage regulation is not supported.

[4] Applies to all input and bidirectional pins except CLKIN.

[5] The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are 3.3 V tolerant (always accepts up to 3.6 V maximum V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}, because V_{OH} (maximum) approximately equals V_{DDEXT} (maximum). This 3.3 V tolerance applies to bidirectional pins (DATA15–0, TMR2–0, PF15–0, PPI3–0, RSCLK1–0, TSCLK1–0, RFS1–0, TFS1–0, MOSI, MISO, SCK) and input only pins ($\overline{BR}$, ARDY, PPI_CLK, DR0PRI, DR0SEC, DR1PRI, DR1SEC, RX, RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, NMI, and BMODE1–0).

[6] Applies to CLKIN pin only.

[7] Applies to all input and bidirectional pins.

The following three tables describe the voltage/frequency requirements for the processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock (Table 10 and Table 11) and system clock (Table 13) specifications. Table 12 describes phase-locked loop operating conditions.

Table 10. Core Clock (CCLK) Requirements—500 MHz, 533 MHz, and 600 MHz Models

Parameter		Internal Regulator Setting	Max	Unit
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.3 V Minimum)[1]	1.30 V	600	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.2 V Minimum)[2]	1.25 V	533	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.14 V Minimum)[3]	1.20 V	500	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	444	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	400	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V	333	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V	250	MHz

[1] Applies to 600 MHz models only. See Ordering Guide on Page 63.
[2] Applies to 533 MHz and 600 MHz models only. See Ordering Guide on Page 63. 533 MHz models cannot support internal regulator levels above 1.25 V.
[3] Applies to 500 MHz, 533 MHz, and 600 MHz models. See Ordering Guide on Page 63. 500 MHz models cannot support internal regulator levels above 1.20 V.

Table 11. Core Clock (CCLK) Requirements—400 MHz Models[1]

Parameter		Internal Regulator Setting	T_J = 125°C Max	All[2] Other T_J Max	Unit
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	400	400	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	333	364	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	295	333	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V		280	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V		250	MHz

[1] See Ordering Guide on Page 63.
[2] See Operating Conditions on Page 20.

Table 12. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	50	Max f_{CCLK}	MHz

Table 13. System Clock (SCLK) Requirements

Parameter[1]		V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
CSP_BGA/PBGA				
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} \geq$ 1.14 V)	100	133	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.14 V)	100	100	MHz
LQFP				
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} \geq$ 1.14 V)	100	133	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.14 V)	83	83	MHz

[1] t_{SCLK} (= $1/f_{SCLK}$) must be greater than or equal to t_{CCLK}.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	400 MHz[1] Min	400 MHz[1] Typical	400 MHz[1] Max	500 MHz/533 MHz/600 MHz[2] Min	500 MHz/533 MHz/600 MHz[2] Typical	500 MHz/533 MHz/600 MHz[2] Max	Unit
V_{OH}	High Level Output Voltage[3]	V_{DDEXT} = 1.75 V, I_{OH} = –0.5 mA V_{DDEXT} = 2.25 V, I_{OH} = –0.5 mA V_{DDEXT} = 3.0 V, I_{OH} = –0.5 mA	1.5 1.9 2.4			1.5 1.9 2.4			V V V
V_{OL}	Low Level Output Voltage[3]	V_{DDEXT} = 1.75 V, I_{OL} = 2.0 mA V_{DDEXT} = 2.25 V/3.0 V, I_{OL} = 2.0 mA			0.2 0.4			0.2 0.4	V V
I_{IH}	High Level Input Current[4]	V_{DDEXT} = Max, V_{IN} = V_{DD} Max			10.0			10.0	µA
I_{IHP}	High Level Input Current JTAG[5]	V_{DDEXT} = Max, V_{IN} = V_{DD} Max			50.0			50.0	µA
I_{IL}[6]	Low Level Input Current[4]	V_{DDEXT} = Max, V_{IN} = 0 V			10.0			10.0	µA
I_{OZH}	Three-State Leakage Current[7]	V_{DDEXT} = Max, V_{IN} = V_{DD} Max			10.0			10.0	µA
I_{OZL}[6]	Three-State Leakage Current[7]	V_{DDEXT} = Max, V_{IN} = 0 V			10.0			10.0	µA
C_{IN}	Input Capacitance[8]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		4	8[9]		4	8[9]	pF
$I_{DDDEEPSLEEP}$[10]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.0 V, f_{CCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		7.5			32.5		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 0.8 V, T_J = 25°C, SCLK = 25 MHz			10			37.5	mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.14 V, f_{CCLK} = 400 MHz, T_J = 25°C		125			152		mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.2 V, f_{CCLK} = 500 MHz, T_J = 25°C					190		mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.2 V, f_{CCLK} = 533 MHz, T_J = 25°C					200		mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.3 V, f_{CCLK} = 600 MHz, T_J = 25°C					245		mA
$I_{DDHIBERNATE}$[10]	V_{DDEXT} Current in Hibernate State	V_{DDEXT} = 3.6 V, CLKIN = 0 MHz, T_J = Max, voltage regulator off (V_{DDINT} = 0 V)		50	100		50	100	µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J = 25°C		20			20		µA
$I_{DDDEEPSLEEP}$[10]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz		6	Table 15		16	Table 14	mA
I_{DD-INT}	V_{DDINT} Current	f_{CCLK} > 0 MHz			$I_{DDDEEPSLEEP}$ + (Table 17 × ASF)			$I_{DDDEEPSLEEP}$ + (Table 17 × ASF)	mA

[1] Applies to all 400 MHz speed grade models. See Ordering Guide on Page 63.
[2] Applies to all 500 MHz, 533 MHz, and 600 MHz speed grade models. See Ordering Guide on Page 63.
[3] Applies to output and bidirectional pins.
[4] Applies to input pins except JTAG inputs.

Table 16. Activity Scaling Factors

I_{DDINT} Power Vector[1]	Activity Scaling Factor (ASF)[2]
$I_{DD-PEAK}$	1.27
$I_{DD-HIGH}$	1.25
I_{DD-TYP}	1.00
I_{DD-APP}	0.86
I_{DD-NOP}	0.72
$I_{DD-IDLE}$	0.41

[1] See EE-229 for power vector definitions.
[2] All ASF values determined using a 10:1 CCLK:SCLK ratio.

Table 17. Dynamic Current (mA, with ASF = 1.0)[1]

	Voltage (V_{DDINT})[2]														
Frequency (MHz)[2]	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V	1.45 V
50	12.7	13.9	15.3	16.8	18.1	19.4	21.0	22.3	24.0	25.4	26.4	27.2	28.7	30.3	30.7
100	22.6	24.2	26.2	28.1	30.1	31.8	34.7	36.2	38.4	40.5	43.0	43.4	45.7	47.9	48.9
200	40.8	44.1	46.9	50.3	53.3	56.9	59.9	63.1	66.7	70.2	73.8	75.0	78.7	82.4	84.6
250	50.1	53.8	57.2	61.4	64.7	68.9	72.9	76.8	81.0	85.1	89.3	90.8	95.2	99.6	102.0
300	N/A	63.5	67.4	72.4	76.2	81.0	85.9	90.6	95.2	100.0	104.8	106.6	111.8	116.9	119.4
375	N/A	N/A	N/A	88.6	93.5	99.0	104.6	110.3	116.0	122.1	128.0	130.0	136.2	142.4	145.5
400	N/A	N/A	N/A	93.9	99.3	105.0	110.8	116.8	123.0	129.4	135.7	137.9	144.6	151.2	154.3
425	N/A	N/A	N/A	N/A	N/A	111.0	117.3	123.5	129.9	136.8	143.2	145.6	152.6	159.7	162.8
475	N/A	N/A	N/A	N/A	N/A	N/A	130.3	136.8	143.8	151.4	158.1	161.1	168.9	176.6	179.7
500	N/A	N/A	N/A	N/A	N/A	N/A	N/A	143.5	150.7	158.7	165.6	168.8	177.0	185.2	188.2
533	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	160.4	168.8	176.5	179.6	188.2	196.8	200.5
600	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	196.2	199.6	209.3	219.0	222.6

[1] The values are not guaranteed as stand-alone maximum specifications, they must be combined with static current per the equations of Electrical Characteristics on Page 22.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 20.

Parallel Peripheral Interface Timing

Table 27 and Figure 17 through Figure 22 describe parallel peripheral interface operations.

Table 27. Parallel Peripheral Interface Timing

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Timing Requirements								
t_{PCLKW}	PPI_CLK Width	8.0		8.0		6.0		ns
t_{PCLK}	PPI_CLK Period[1]	20.0		20.0		15.0		ns
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK Edge (Nonsampling Edge for Rx, Sampling Edge for Tx)	6.0		6.0		4.0[2]		ns ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.0[2]		1.0[2]		1.0[2]		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	3.5		3.5		3.5		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	1.5		1.5		1.5		ns
Switching Characteristics—GP Output and Frame Capture Modes								
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		11.0		8.0		8.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	1.7		1.7		1.7		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		11.0		9.0		9.0	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	1.8		1.8		1.8		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$.
[2] Applies when PPI_CONTROL Bit 8 is cleared. See Figure 19 and Figure 22.

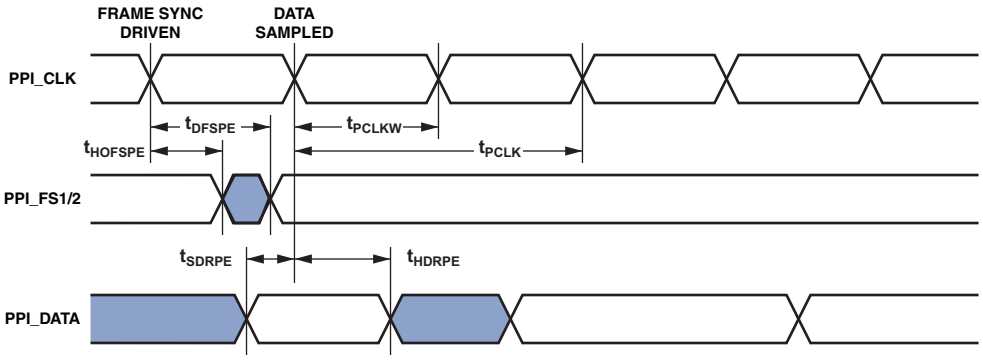


Figure 17. PPI GP Rx Mode with Internal Frame Sync Timing

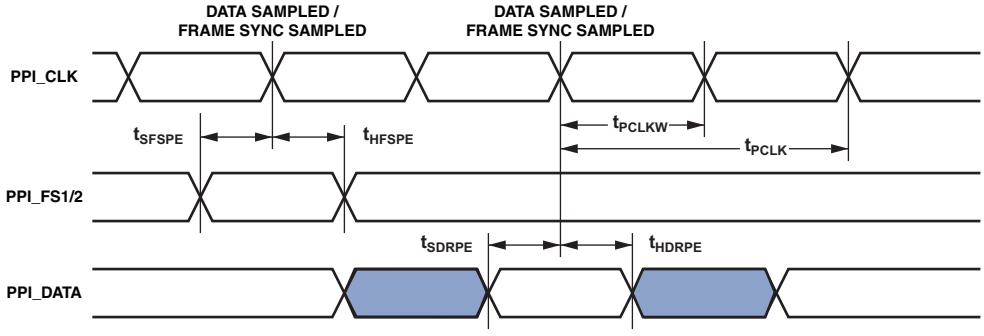


Figure 18. PPI GP Rx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 1)

Serial Port Timing

Table 28 through Table 31 on Page 37 and Figure 23 on Page 35 through Figure 26 on Page 37 describe Serial Port operations.

Table 28. Serial Ports—External Clock

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{SFSE}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	3.0		3.0		ns
t_{HFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	3.0		3.0		ns
t_{SDRE}	Receive Data Setup Before RSCLKx[1]	3.0		3.0		ns
t_{HDRE}	Receive Data Hold After RSCLKx[1]	3.0		3.0		ns
t_{SCLKEW}	TSCLKx/RSCLKx Width	8.0		4.5		ns
t_{SCLKE}	TSCLKx/RSCLKx Period	20.0		15.0[2]		ns
t_{SUDTE}	Start-Up Delay From SPORT Enable To First External TFSx[3]	4.0 × t_{SCLKE}		4.0 × t_{SCLKE}		ns
t_{SUDRE}	Start-Up Delay From SPORT Enable To First External RFSx[3]	4.0 × t_{SCLKE}		4.0 × t_{SCLKE}		ns
Switching Characteristics						
t_{DFSE}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[4]		10.0		10.0	ns
t_{HOFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[1]	0.0		0.0		ns
t_{DDTE}	Transmit Data Delay After TSCLKx[1]		10.0		10.0	ns
t_{HDTE}	Transmit Data Hold After TSCLKx[1]	0.0		0.0		ns

[1] Referenced to sample edge.
[2] For receive mode with external RSCLKx and external RFSx only, the maximum specification is 11.11 ns (90 MHz).
[3] Verified in design but untested. After being enabled, the serial port requires external clock pulses—before the first external frame sync edge—to initialize the serial port.
[4] Referenced to drive edge.

Table 29. Serial Ports—Internal Clock

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{SFSI}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	11.0		9.0		ns
t_{HFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	–2.0		–2.0		ns
t_{SDRI}	Receive Data Setup Before RSCLKx[1]	9.5		9.0		ns
t_{HDRI}	Receive Data Hold After RSCLKx[1]	0.0		0.0		ns
Switching Characteristics						
t_{DFSI}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]		3.0		3.0	ns
t_{HOFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[1]	–1.0		–1.0		ns
t_{DDTI}	Transmit Data Delay After TSCLKx[1]		3.0		3.0	ns
t_{HDTI}	Transmit Data Hold After TSCLKx[1]	–2.5		–2.0		ns
t_{SCLKIW}	TSCLKx/RSCLKx Width	6.0		4.5		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

OUTPUT DRIVE CURRENTS

Figure 33 through Figure 44 show typical current-voltage characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

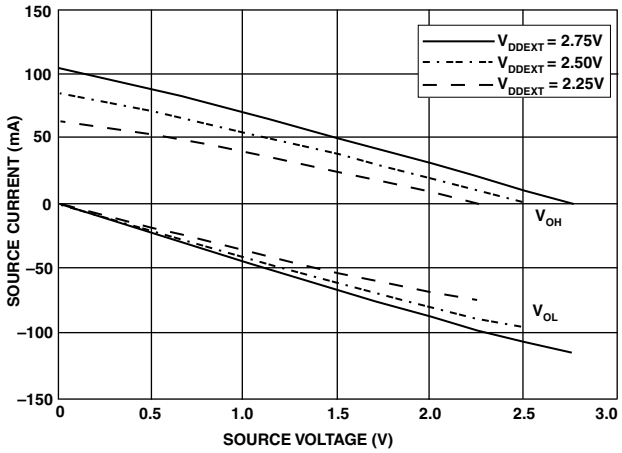


Figure 33. Drive Current A (V_{DDEXT} = 2.5 V)

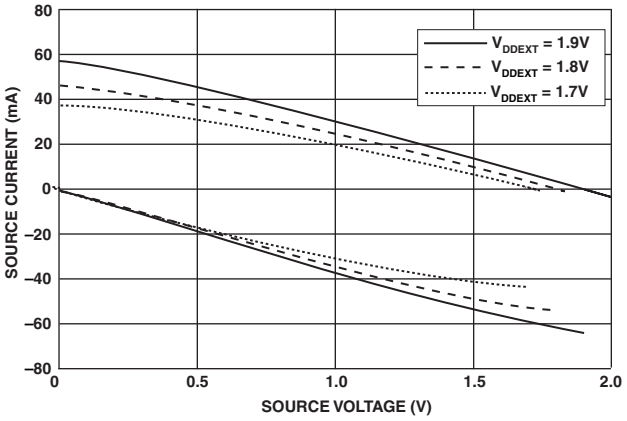


Figure 34. Drive Current A (V_{DDEXT} = 1.8 V)

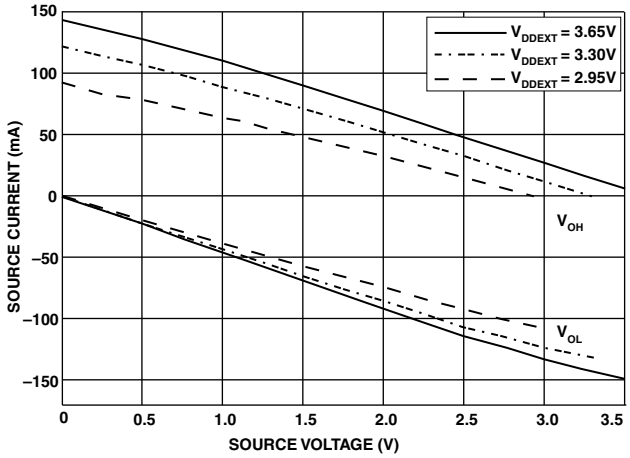


Figure 35. Drive Current A (V_{DDEXT} = 3.3 V)

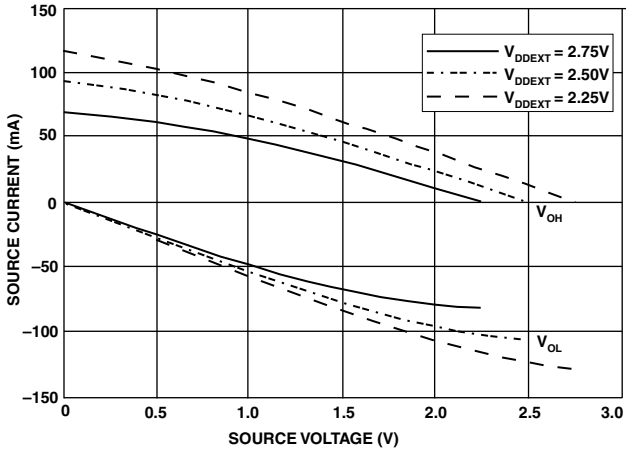


Figure 36. Drive Current B (V_{DDEXT} = 2.5 V)

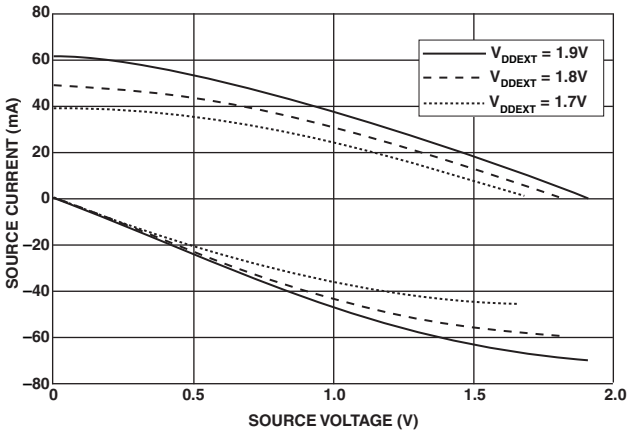


Figure 37. Drive Current B (V_{DDEXT} = 1.8 V)

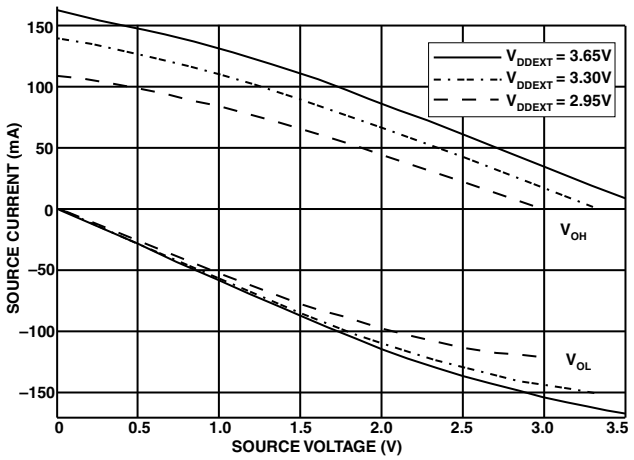


Figure 38. Drive Current B (V_{DDEXT} = 3.3 V)

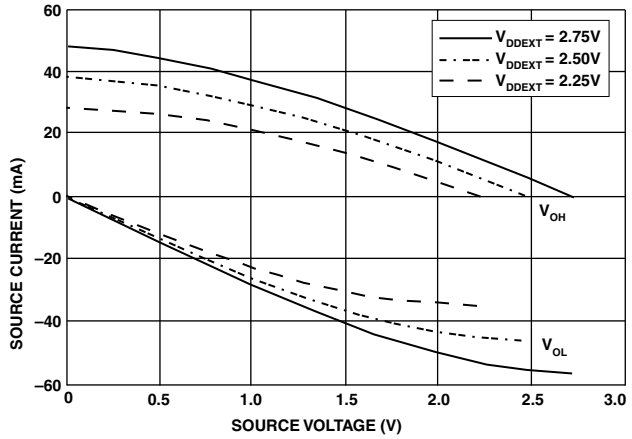


Figure 39. Drive Current C (V_{DDEXT} = 2.5 V)

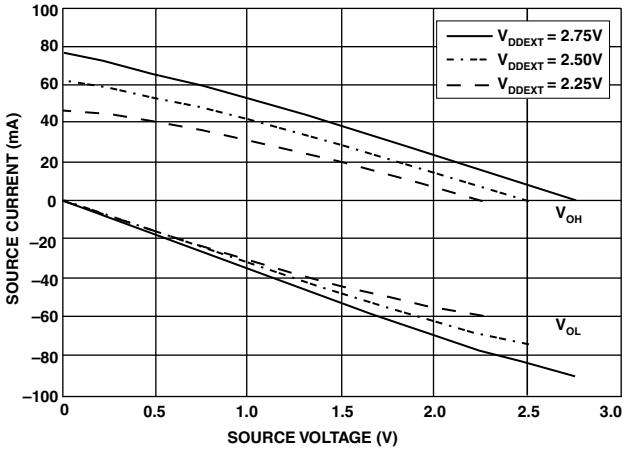


Figure 42. Drive Current D (V_{DDEXT} = 2.5 V)

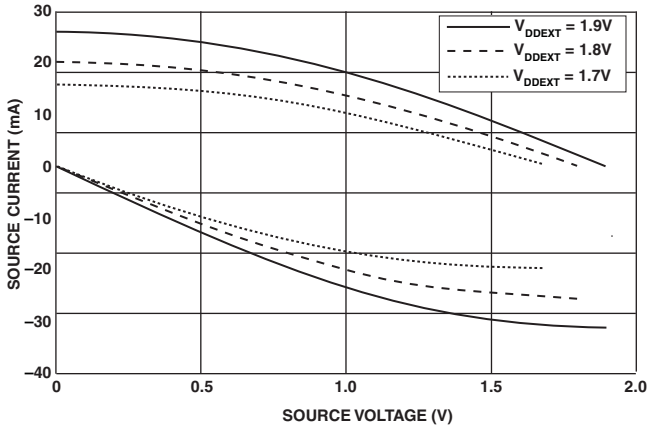


Figure 40. Drive Current C (V_{DDEXT} = 1.8 V)

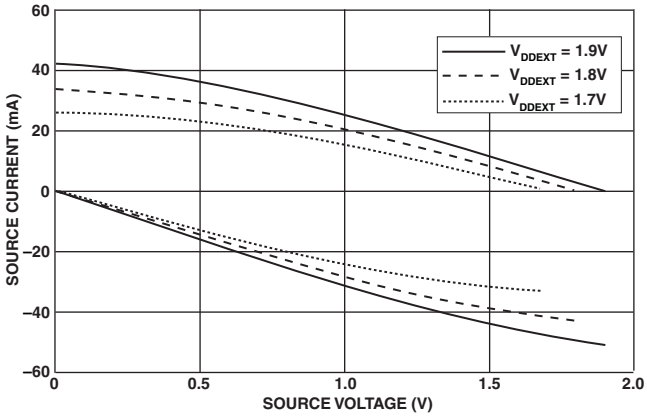


Figure 43. Drive Current D (V_{DDEXT} = 1.8 V)

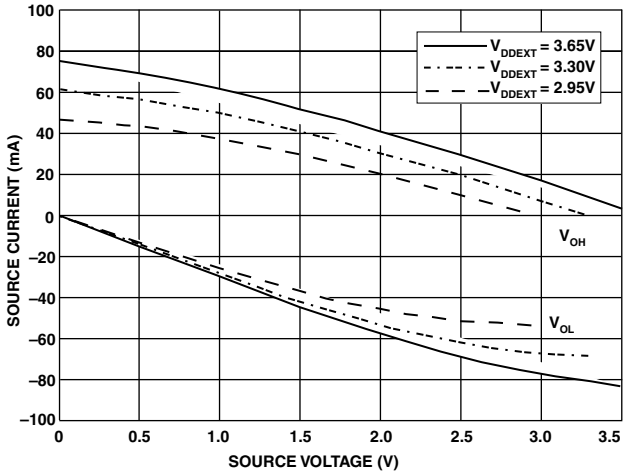


Figure 41. Drive Current C (V_{DDEXT} = 3.3 V)

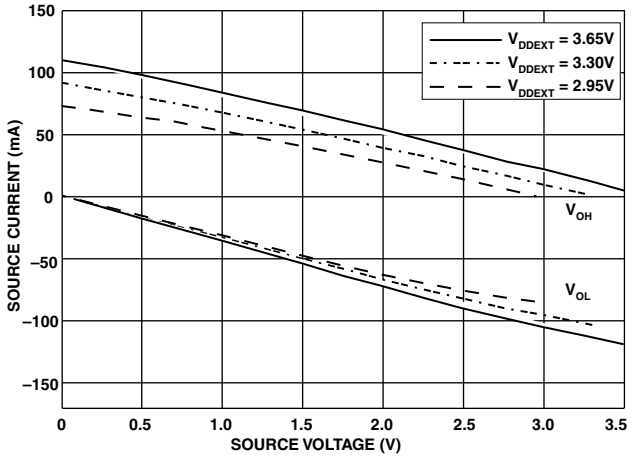
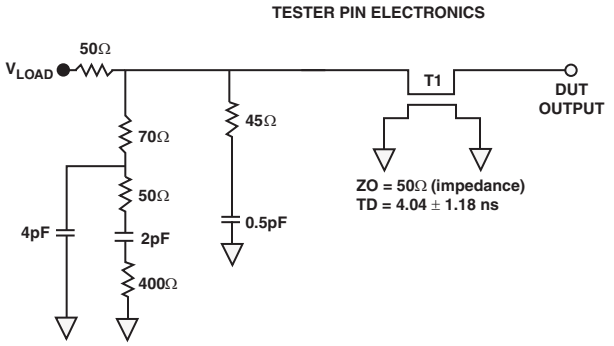


Figure 44. Drive Current D (V_{DDEXT} = 3.3 V)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 47). V_{LOAD} is 0.95 V for V_{DDEXT} (nominal) = 1.8 V or 1.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V. Figure 48 through Figure 59 on Page 48 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 47. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

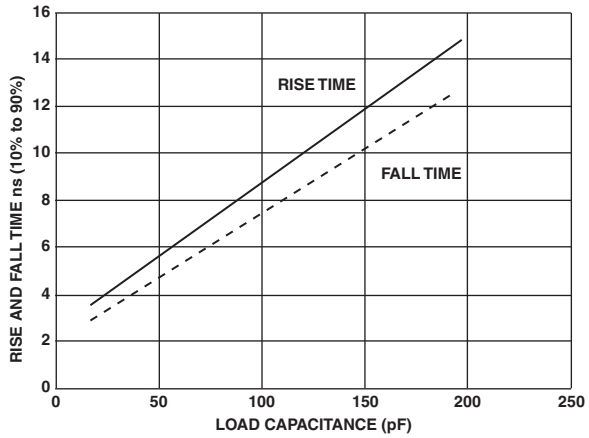


Figure 48. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 1.75 V

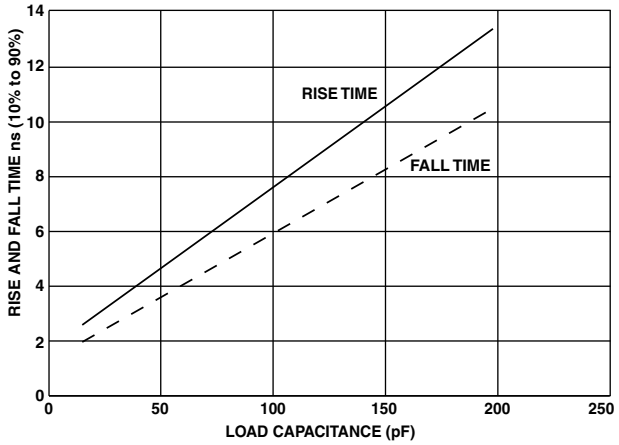


Figure 49. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 2.25 V

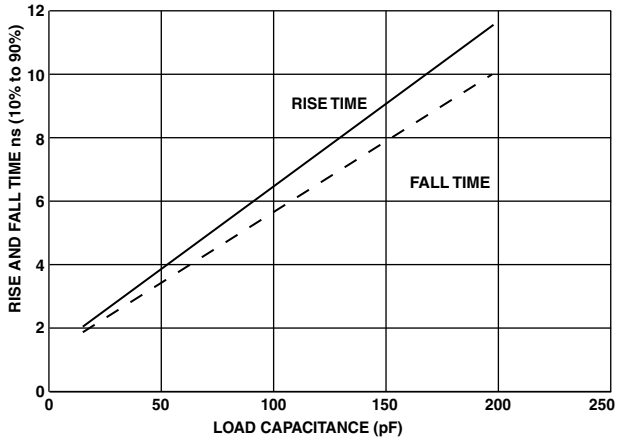


Figure 50. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 3.65 V

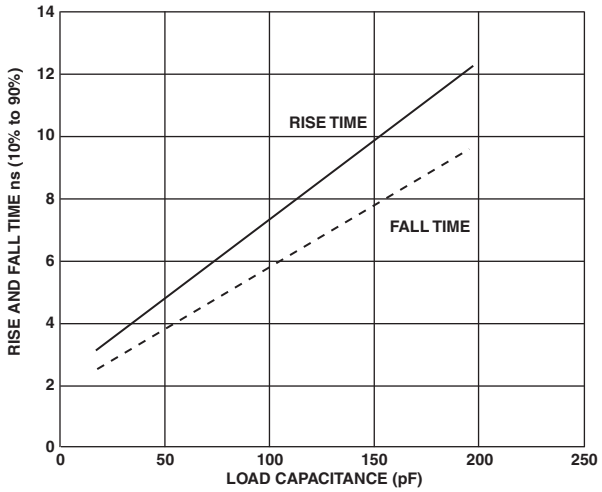


Figure 51. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 1.75 V

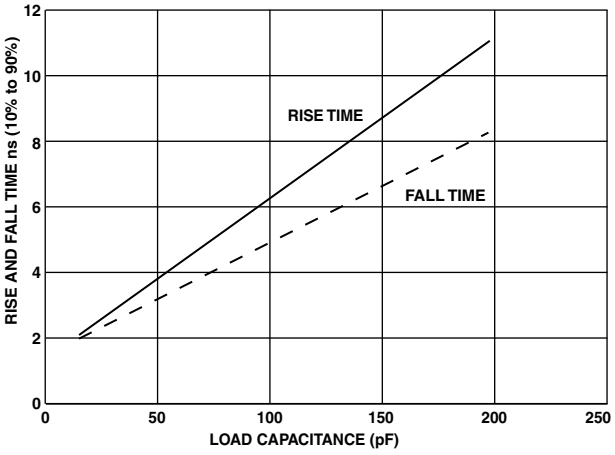


Figure 52. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 2.25 V

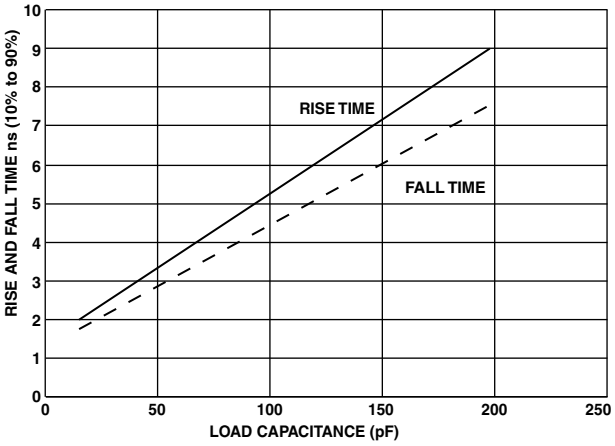


Figure 53. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 3.65 V

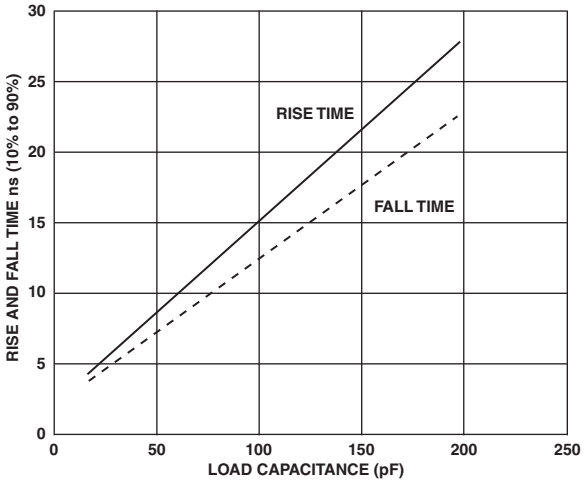


Figure 54. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 1.75 V

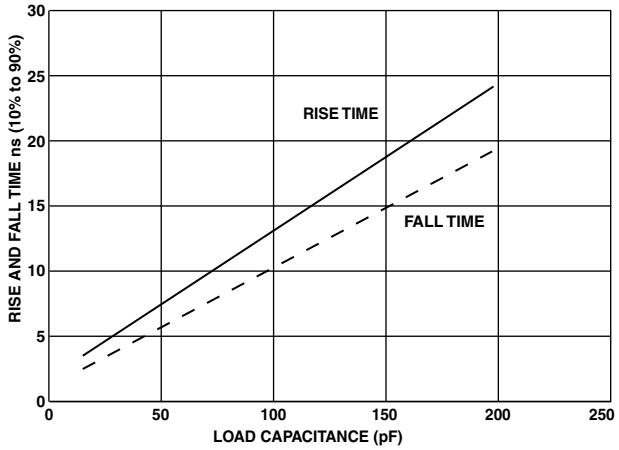


Figure 55. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 2.25 V

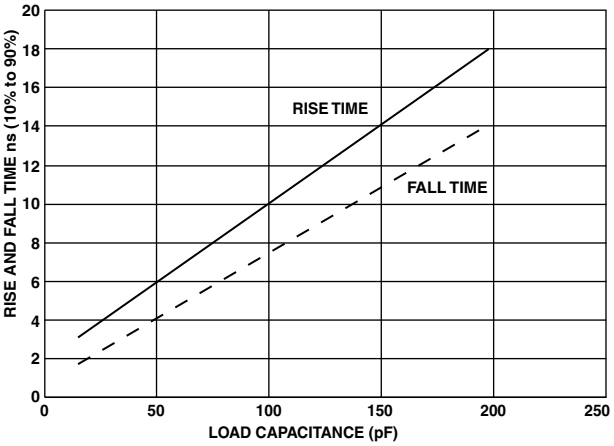


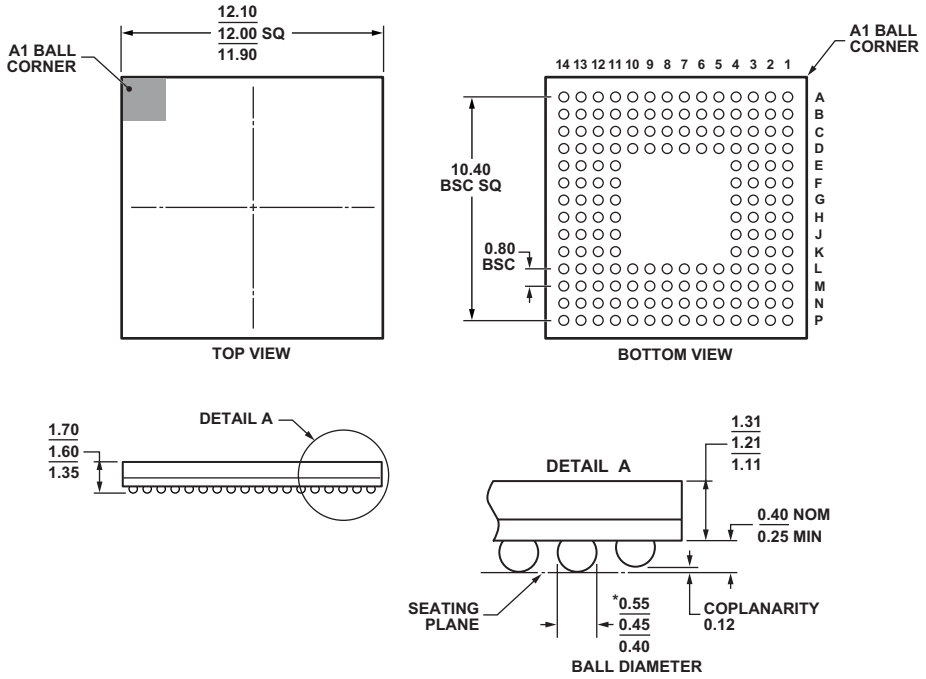
Figure 56. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 3.65 V

169-BALL PBGA BALL ASSIGNMENT

Table 43 lists the PBGA ball assignment by signal. Table 44 on Page 54 lists the PBGA ball assignment by ball number.

Table 43. 169-Ball PBGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{ABE0}$	H16	DATA4	U12	GND	K9	RTXI	A10	V_{DDEXT}	K6
$\overline{ABE1}$	H17	DATA5	U11	GND	K10	RTXO	A11	V_{DDEXT}	L6
ADDR1	J16	DATA6	T10	GND	K11	RX	T1	V_{DDEXT}	M6
ADDR2	J17	DATA7	U10	GND	L7	SA10	B15	V_{DDEXT}	M7
ADDR3	K16	DATA8	T9	GND	L8	$\overline{SCAS}$	A16	V_{DDEXT}	M8
ADDR4	K17	DATA9	U9	GND	L9	SCK	D1	V_{DDEXT}	T2
ADDR5	L16	DATA10	T8	GND	L10	SCKE	B14	VROUT0	B12
ADDR6	L17	DATA11	U8	GND	L11	$\overline{SMS}$	A17	VROUT1	B13
ADDR7	M16	DATA12	U7	GND	M9	$\overline{SRAS}$	A15	XTAL	A13
ADDR8	M17	DATA13	T7	GND	T16	$\overline{SWE}$	B17		
ADDR9	N17	DATA14	U6	MISO	E2	TCK	U4		
ADDR10	N16	DATA15	T6	MOSI	E1	TDI	U3		
ADDR11	P17	DR0PRI	M2	NMI	B11	TDO	T4		
ADDR12	P16	DR0SEC	M1	PF0	D2	TFS0	L1		
ADDR13	R17	DR1PRI	H1	PF1	C1	TFS1	G2		
ADDR14	R16	DR1SEC	H2	PF2	B1	TMR0	R1		
ADDR15	T17	DT0PRI	K2	PF3	C2	TMR1	P2		
ADDR16	U15	DT0SEC	K1	PF4	A1	TMR2	P1		
ADDR17	T15	DT1PRI	F1	PF5	A2	TMS	T3		
ADDR18	U16	DT1SEC	F2	PF6	B3	$\overline{TRST}$	U2		
ADDR19	T14	$\overline{EMU}$	U1	PF7	A3	TSCLK0	L2		
$\overline{AMS0}$	D17	GND	B16	PF8	B4	TSCLK1	G1		
$\overline{AMS1}$	E16	GND	F11	PF9	A4	TX	R2		
$\overline{AMS2}$	E17	GND	G7	PF10	B5	VDD	F12		
$\overline{AMS3}$	F16	GND	G8	PF11	A5	VDD	G12		
$\overline{AOE}$	F17	GND	G9	PF12	A6	VDD	H12		
ARDY	C16	GND	G10	PF13	B6	VDD	J12		
$\overline{ARE}$	G16	GND	G11	PF14	A7	VDD	K12		
$\overline{AWE}$	G17	GND	H7	PF15	B7	VDD	L12		
$\overline{BG}$	T13	GND	H8	PPI_CLK	B10	VDD	M10		
$\overline{BGH}$	U17	GND	H9	PPI0	B9	VDD	M11		
BMODE0	U5	GND	H10	PPI1	A9	VDD	M12		
BMODE1	T5	GND	H11	PPI2	B8	V_{DDEXT}	B2		
$\overline{BR}$	C17	GND	J7	PPI3	A8	V_{DDEXT}	F6		
CLKIN	A14	GND	J8	$\overline{RESET}$	A12	V_{DDEXT}	F7		
CLKOUT	D16	GND	J9	RFS0	N1	V_{DDEXT}	F8		
DATA0	U14	GND	J10	RFS1	J1	V_{DDEXT}	F9		
DATA1	T12	GND	J11	RSCLK0	N2	V_{DDEXT}	G6		
DATA2	U13	GND	K7	RSCLK1	J2	V_{DDEXT}	H6		
DATA3	T11	GND	K8	RTCVDD	F10	V_{DDEXT}	J6		



*COMPLIANT TO JEDEC STANDARDS MO-205-AE WITH THE EXCEPTION TO BALL DIAMETER.

Figure 65. 160-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-160-2)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 47 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 47. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
Chip Scale Package Ball Grid Array (CSP_BGA) BC-160-2	Solder Mask Defined	0.40 mm diameter	0.55 mm diameter
Plastic Ball Grid Array (PBGA) B-169	Solder Mask Defined	0.43 mm diameter	0.56 mm diameter

ORDERING GUIDE

Model [1]	Temperature Range [2]	Speed Grade (Max)	Package Description	Package Option
ADSP-BF531SBB400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF531SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF531SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF531SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF531SBBCZ4RL	–40°C to +85°C	400 MHz	160-Ball CSP_BGA, 13" Tape and Reel	BC-160-2
ADSP-BF531SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF532SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF532SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF532SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF532SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF533SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF533SBB500	–40°C to +85°C	500 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBZ500	–40°C to +85°C	500 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBC500	–40°C to +85°C	500 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ500	–40°C to +85°C	500 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBC-5V	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ-5V	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKBC-6V	0°C to +70°C	600 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKBCZ-6V	0°C to +70°C	600 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKSTZ-5V	0°C to +70°C	533 MHz	176-Lead LQFP	ST-176-1

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 20 for junction temperature (T_J) specification which is the only temperature specification.