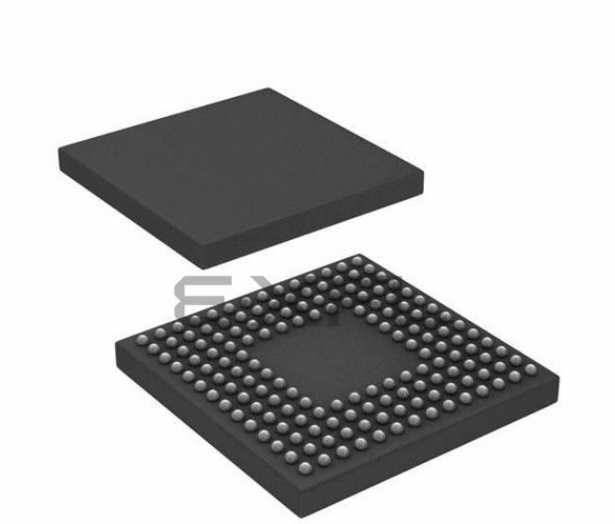

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	400MHz
Non-Volatile Memory	ROM (1kB)
On-Chip RAM	52kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LFBGA, CSPBGA
Supplier Device Package	160-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf531sbbcz4rl

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8/13— Rev. H to Rev. I

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Updated Ordering Guide 63

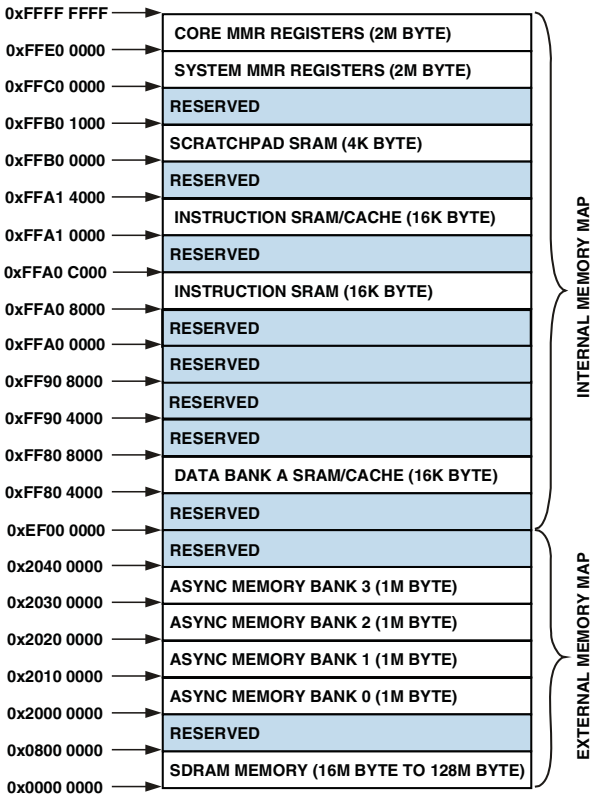


Figure 3. ADSP-BF531 Internal/External Memory Map

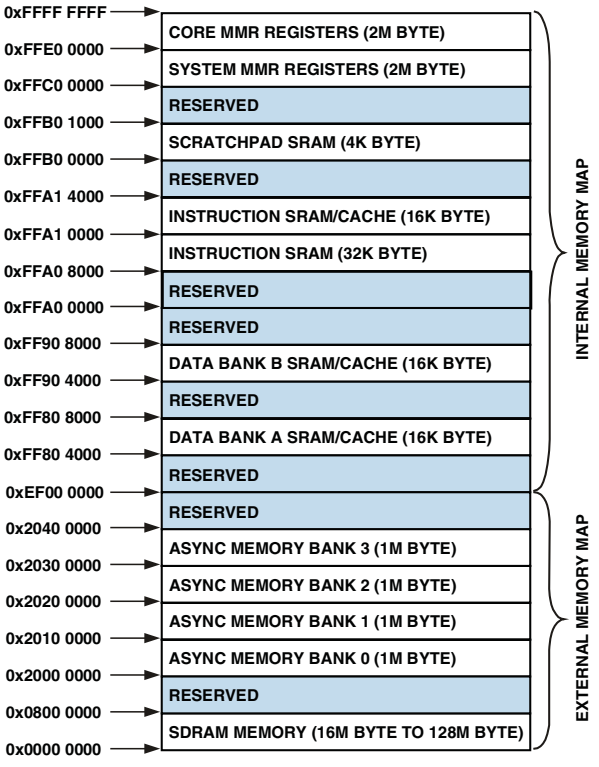


Figure 4. ADSP-BF532 Internal/External Memory Map

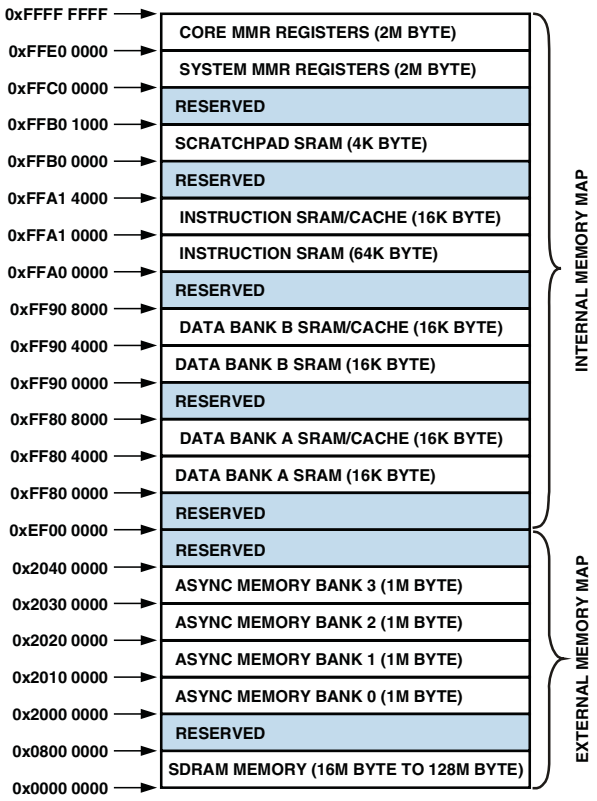


Figure 5. ADSP-BF533 Internal/External Memory Map

Event Handling

The event controller on the processors handle all asynchronous and synchronous events to the processor. The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provide event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher priority event takes precedence over servicing of a lower priority event. The controller provides support for five different types of events:

- Emulation – An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- Reset – This event resets the processor.
- Nonmaskable Interrupt (NMI) – The NMI event can be generated by the software watchdog timer or by the NMI input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- Exceptions – Events that occur synchronously to program flow (i.e., the exception is taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts – Events that occur asynchronously to program flow. They are caused by input pins, timers, and other peripherals, as well as by an explicit software instruction.

- CEC interrupt pending register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but can be read while in supervisor mode.

The SIC allows further control of event processing by providing three 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in Table 3.

- SIC interrupt mask register (SIC_IMASK) – This register controls the masking and unmasking of each peripheral interrupt event. When a bit is set in this register, that peripheral event is unmasked and is processed by the system when asserted. A cleared bit in this register masks the peripheral event, preventing the processor from servicing the event.
- SIC interrupt status register (SIC_ISR) – As multiple peripherals can be mapped to a single event, this register allows the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt, and a cleared bit indicates the peripheral is not asserting the event.
- SIC interrupt wakeup enable register (SIC_IWR) – By enabling the corresponding bit in this register, a peripheral can be configured to wake up the processor, should the core be idled when the event is generated. See Dynamic Power Management on Page 11.

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC recognizes and queues the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

DMA CONTROLLERS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have multiple, independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the SPORTs, SPI port, UART, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The DMA controller supports both 1-dimensional (1-D) and 2-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, autorefreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two pairs of memory DMA channels provided for transfers between the various memories of the processor system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

REAL-TIME CLOCK

The processor real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors. The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60 second counter, a 60 minute counter, a 24 hour counter, and a 32,768 day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. The two alarms are time of day and a day and time of that day.

PFx pins defined as inputs can be configured to generate hardware interrupts, while output PFx pins can be triggered by software interrupts.

- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual PFx pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

PARALLEL PERIPHERAL INTERFACE

The processors provide a parallel peripheral interface (PPI) that can connect directly to parallel ADCs and DACs, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bi-directional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bi-directional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications.

Three distinct sub modes are supported:

- Input mode – Frame syncs and data are inputs into the PPI.
- Frame capture mode – Frame syncs are outputs from the PPI, but data are inputs.
- Output mode – Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (e.g., for frame capture). The processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct sub modes are supported:

- Active video only mode
- Vertical blanking only mode
- Entire field mode

Active Video Only Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that can be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

DYNAMIC POWER MANAGEMENT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provides four operating modes, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

t_{NOM} is the duration running at $f_{CCLKNOM}$

t_{RED} is the duration running at $f_{CCLKRED}$

The percent power savings is calculated as:

$$\%\ power\ savings\ =\ (1 - power\ savings\ factor) \times 100\%$$

VOLTAGE REGULATION

The Blackfin processor provides an on-chip voltage regulator that can generate appropriate V_{DDINT} voltage levels from the V_{DDEXT} supply. See Operating Conditions on Page 20 for regulator tolerances and acceptable V_{DDEXT} ranges for specific models.

Figure 7 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power (V_{DDEXT}) supplied. While in the hibernate state, I/O power is still being applied, eliminating the need for external buffers. The voltage regulator can be activated from this power-down state either through an RTC wakeup or by asserting $\overline{\text{RESET}}$, both of which initiate a boot sequence. The regulator can also be disabled and bypassed at the user's discretion.

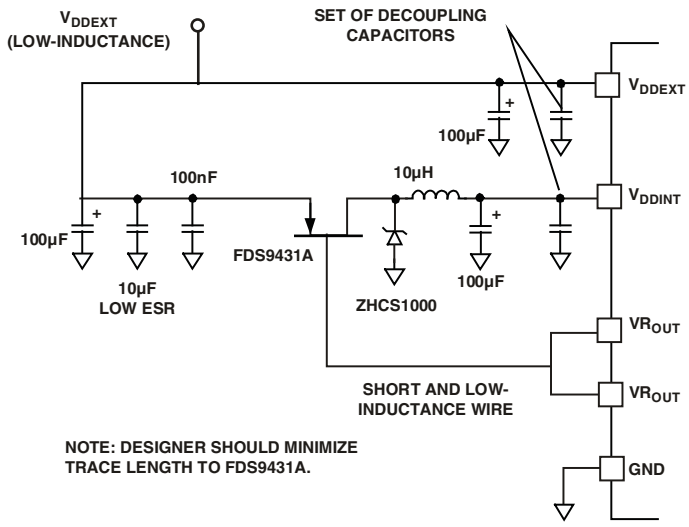


Figure 7. Voltage Regulator Circuit

Voltage Regulator Layout Guidelines

Regulator external component placement, board routing, and bypass capacitors all have a significant effect on noise injected into the other analog circuits on-chip. The VROUT1–0 traces and voltage regulator external components should be considered as noise sources when doing board layout and should not be routed or placed near sensitive circuits or components on the board. All internal and I/O power supplies should be well bypassed with bypass capacitors placed as close to the processors as possible.

For further details on the on-chip voltage regulator and related board design guidelines, see the *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228)* applications note on the Analog Devices web site (www.analog.com)—use site search on "EE-228".

CLOCK SIGNALS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the processors include an on-chip oscillator circuit, an external crystal can be used. For fundamental frequency operation, use the circuit shown in Figure 8.

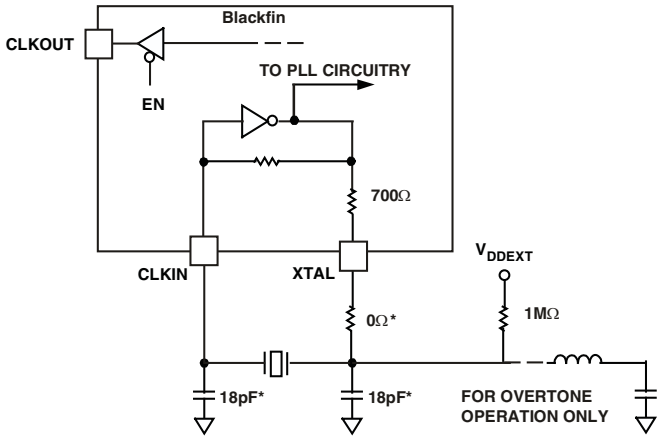


Figure 8. External Crystal Connections

A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor shown in Figure 8 fine tune the phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 8 are typical values only. The capacitor values are dependent upon the crystal manufacturer's load capacitance recommendations and the physical PCB layout. The resistor value depends on the drive level specified by the crystal manufacturer. System designs should verify the customized values based on careful investigation on multiple devices over the allowed temperature range.

A third-overtone crystal can be used at frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 8.

PIN DESCRIPTIONS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors pin definitions are listed in Table 9.

All pins are three-stated during and immediately after reset, except the memory interface, asynchronous memory control, and synchronous memory control pins. These pins are all driven high, with the exception of CLKOUT, which toggles at the system clock rate. During hibernate, all outputs are three-stated unless otherwise noted in Table 9.

If $\overline{BR}$ is active (whether or not $\overline{RESET}$ is asserted), the memory pins are also three-stated. All unused I/O pins have their input buffers disabled with the exception of the pins that need pull-ups or pull-downs as noted in the table.

In order to maintain maximum functionality and reduce package size and pin count, some pins have dual, multiplexed functionality. In cases where pin functionality is reconfigurable, the default state is shown in plain text, while alternate functionality is shown in italics.

Table 9. Pin Descriptions

Pin Name	Type	Function	Driver Type[1]
Memory Interface			
ADDR19–1	O	Address Bus for Async/Sync Access	A
DATA15–0	I/O	Data Bus for Async/Sync Access	A
$\overline{ABE1–0}$/SDQM1–0	O	Byte Enables/Data Masks for Async/Sync Access	A
$\overline{BR}$	I	Bus Request (This pin should be pulled high if not used.)	
$\overline{BG}$	O	Bus Grant	A
$\overline{BGH}$	O	Bus Grant Hang	A
Asynchronous Memory Control			
$\overline{AMS3–0}$	O	Bank Select (Require pull-ups if hibernate is used.)	A
ARDY	I	Hardware Ready Control (This pin should be pulled high if not used.)	
$\overline{AOE}$	O	Output Enable	A
$\overline{ARE}$	O	Read Enable	A
$\overline{AWE}$	O	Write Enable	A
Synchronous Memory Control			
$\overline{SRAS}$	O	Row Address Strobe	A
$\overline{SCAS}$	O	Column Address Strobe	A
$\overline{SWE}$	O	Write Enable	A
SCKE	O	Clock Enable (Requires pull-down if hibernate is used.)	A
CLKOUT	O	Clock Output	B
SA10	O	A10 Pin	A
$\overline{SMS}$	O	Bank Select	A
Timers			
TMR0	I/O	Timer 0	C
TMR1/*PPI_FS1*	I/O	Timer 1/*PPI Frame Sync1*	C
TMR2/*PPI_FS2*	I/O	Timer 2/*PPI Frame Sync2*	C
PPI Port			
PPI3–0	I/O	PPI3–0	C
PPI_CLK/*TMRCLK*	I	PPI Clock/*External Timer Reference*	

Table 9. Pin Descriptions (Continued)

Pin Name	Type	Function	Driver Type[1]
RFS1	I/O	SPORT1 Receive Frame Sync	C
DR1PRI	I	SPORT1 Receive Data Primary	
DR1SEC	I	SPORT1 Receive Data Secondary	
TSCLK1	I/O	SPORT1 Transmit Serial Clock	D
TFS1	I/O	SPORT1 Transmit Frame Sync	C
DT1PRI	O	SPORT1 Transmit Data Primary	C
DT1SEC	O	SPORT1 Transmit Data Secondary	C
UART Port			
RX	I	UART Receive	
TX	O	UART Transmit	C
Real-Time Clock			
RTXI	I	RTC Crystal Input (This pin should be pulled low when not used.)	
RTXO	O	RTC Crystal Output (Does not three-state in hibernate.)	
Clock			
CLKIN	I	Clock/Crystal Input (This pin needs to be at a level or clocking.)	
XTAL	O	Crystal Output	
Mode Controls			
$\overline{\text{RESET}}$	I	Reset (This pin is always active during core power-on.)	
NMI	I	Nonmaskable Interrupt (This pin should be pulled low when not used.)	
BMODE1–0	I	Boot Mode Strap (These pins must be pulled to the state required for the desired boot mode.)	
Voltage Regulator			
VROUT1–0	O	External FET Drive (These pins should be left unconnected when unused and are driven high during hibernate.)	
Supplies			
V_{DDEXT}	P	I/O Power Supply	
V_{DDINT}	P	Core Power Supply	
V_{DDRTC}	P	Real-Time Clock Power Supply (This pin should be connected to V_{DDEXT} when not used and should remain powered at all times.)	
GND	G	External Ground	

[1] Refer to Figure 33 on Page 43 to Figure 44 on Page 44.

The following three tables describe the voltage/frequency requirements for the processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock (Table 10 and Table 11) and system clock (Table 13) specifications. Table 12 describes phase-locked loop operating conditions.

Table 10. Core Clock (CCLK) Requirements—500 MHz, 533 MHz, and 600 MHz Models

Parameter		Internal Regulator Setting	Max	Unit
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.3 V Minimum)[1]	1.30 V	600	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.2 V Minimum)[2]	1.25 V	533	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.14 V Minimum)[3]	1.20 V	500	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	444	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	400	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V	333	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V	250	MHz

[1] Applies to 600 MHz models only. See Ordering Guide on Page 63.
[2] Applies to 533 MHz and 600 MHz models only. See Ordering Guide on Page 63. 533 MHz models cannot support internal regulator levels above 1.25 V.
[3] Applies to 500 MHz, 533 MHz, and 600 MHz models. See Ordering Guide on Page 63. 500 MHz models cannot support internal regulator levels above 1.20 V.

Table 11. Core Clock (CCLK) Requirements—400 MHz Models[1]

Parameter		Internal Regulator Setting	T_J = 125°C Max	All[2] Other T_J Max	Unit
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	400	400	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	333	364	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	295	333	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V		280	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V		250	MHz

[1] See Ordering Guide on Page 63.
[2] See Operating Conditions on Page 20.

Table 12. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	50	Max f_{CCLK}	MHz

Table 13. System Clock (SCLK) Requirements

Parameter[1]		V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
CSP_BGA/PBGA				
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} \geq$ 1.14 V)	100	133	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.14 V)	100	100	MHz
LQFP				
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} \geq$ 1.14 V)	100	133	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.14 V)	83	83	MHz

[1] t_{SCLK} (= $1/f_{SCLK}$) must be greater than or equal to t_{CCLK}.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	400 MHz[1] Min	400 MHz[1] Typical	400 MHz[1] Max	500 MHz/533 MHz/600 MHz[2] Min	500 MHz/533 MHz/600 MHz[2] Typical	500 MHz/533 MHz/600 MHz[2] Max	Unit
V_{OH}	High Level Output Voltage[3]	V_{DDEXT} = 1.75 V, I_{OH} = –0.5 mA V_{DDEXT} = 2.25 V, I_{OH} = –0.5 mA V_{DDEXT} = 3.0 V, I_{OH} = –0.5 mA	1.5 1.9 2.4			1.5 1.9 2.4			V V V
V_{OL}	Low Level Output Voltage[3]	V_{DDEXT} = 1.75 V, I_{OL} = 2.0 mA V_{DDEXT} = 2.25 V/3.0 V, I_{OL} = 2.0 mA			0.2 0.4			0.2 0.4	V V
I_{IH}	High Level Input Current[4]	V_{DDEXT} = Max, V_{IN} = V_{DD} Max			10.0			10.0	µA
I_{IHP}	High Level Input Current JTAG[5]	V_{DDEXT} = Max, V_{IN} = V_{DD} Max			50.0			50.0	µA
I_{IL}[6]	Low Level Input Current[4]	V_{DDEXT} = Max, V_{IN} = 0 V			10.0			10.0	µA
I_{OZH}	Three-State Leakage Current[7]	V_{DDEXT} = Max, V_{IN} = V_{DD} Max			10.0			10.0	µA
I_{OZL}[6]	Three-State Leakage Current[7]	V_{DDEXT} = Max, V_{IN} = 0 V			10.0			10.0	µA
C_{IN}	Input Capacitance[8]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		4	8[9]		4	8[9]	pF
$I_{DDDEEPSLEEP}$[10]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.0 V, f_{CCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		7.5			32.5		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 0.8 V, T_J = 25°C, SCLK = 25 MHz			10			37.5	mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.14 V, f_{CCLK} = 400 MHz, T_J = 25°C		125			152		mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.2 V, f_{CCLK} = 500 MHz, T_J = 25°C					190		mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.2 V, f_{CCLK} = 533 MHz, T_J = 25°C					200		mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.3 V, f_{CCLK} = 600 MHz, T_J = 25°C					245		mA
$I_{DDHIBERNATE}$[10]	V_{DDEXT} Current in Hibernate State	V_{DDEXT} = 3.6 V, CLKIN = 0 MHz, T_J = Max, voltage regulator off (V_{DDINT} = 0 V)		50	100		50	100	µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J = 25°C		20			20		µA
$I_{DDDEEPSLEEP}$[10]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz		6	Table 15		16	Table 14	mA
I_{DD-INT}	V_{DDINT} Current	f_{CCLK} > 0 MHz			$I_{DDDEEPSLEEP}$ + (Table 17 × ASF)			$I_{DDDEEPSLEEP}$ + (Table 17 × ASF)	mA

[1] Applies to all 400 MHz speed grade models. See Ordering Guide on Page 63.
[2] Applies to all 500 MHz, 533 MHz, and 600 MHz speed grade models. See Ordering Guide on Page 63.
[3] Applies to output and bidirectional pins.
[4] Applies to input pins except JTAG inputs.

TIMING SPECIFICATIONS

Clock and Reset Timing

Table 21 and Figure 11 describe clock and reset operations. Per Absolute Maximum Ratings on Page 25, combinations of CLKIN and clock multipliers/divisors must not result in core/system clocks exceeding the maximum limits allowed for the processor, including system clock restrictions related to supply voltage.

Table 21. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN Period[1, 2, 3, 4]	25.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse	10.0		ns
t_{CKINH}	CLKIN High Pulse	10.0		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[5]	11 × t_{CKIN}		ns
t_{NOBOOT}	$\overline{\text{RESET}}$ Deassertion to First External Access Delay[6]	3 × t_{CKIN}	5 × t_{CKIN}	ns

[1] Applies to PLL bypass mode and PLL non bypass mode.
[2] CLKIN frequency must not change on the fly.
[3] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 11 on Page 21 through Table 13 on Page 21. Since the default behavior of the PLL is to multiply the CLKIN frequency by 10, the 400 MHz speed grade parts cannot use the full CLKIN period range.
[4] If the DF bit in the PLL_CTL register is set, then the maximum t_{CKIN} period is 50 ns.
[5] Applies after power-up sequence is complete. See Table 22 and Figure 12 for power-up reset timing.
[6] Applies when processor is configured in No Boot Mode (BMODE1-0 = b#00).

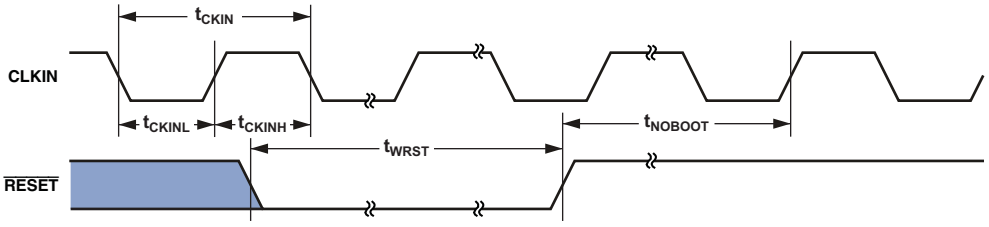
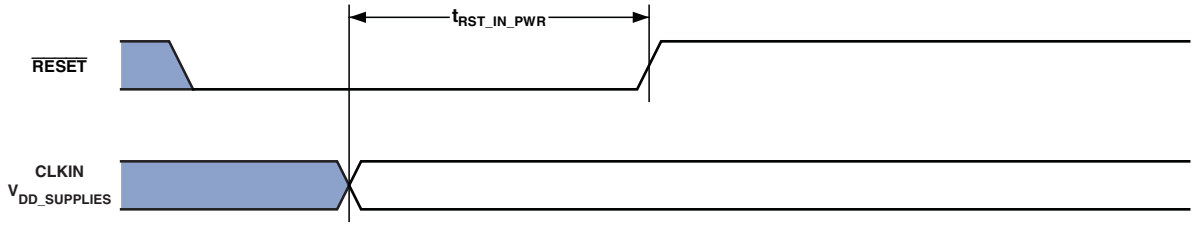


Figure 11. Clock and Reset Timing

Table 22. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted After the V_{DDINT}, V_{DDEXT}, V_{DDRTC}, and CLKIN Pins Are Stable and Within Specification	3500 × t_{CKIN}		ns



In Figure 12, $V_{DD\_SUPPLIES}$ is V_{DDINT}, V_{DDEXT}, V_{DDRTC}

Figure 12. Power-Up Reset Timing

External Port Bus Request and Grant Cycle Timing

Table 26 and Figure 16 describe external port bus request and bus grant operations.

Table 26. External Port Bus Request and Grant Cycle Timing

Parameter	V_{DDEXT} = 1.8 V LQFP/PBGA Packages		V_{DDEXT} = 1.8 V CSP_BGA Package		V_{DDEXT} = 2.5 V/3.3 V All Packages		Unit
	Min	Max	Min	Max	Min	Max	
Timing Requirements							
t_{BS} $\overline{BR}$ Asserted to CLKOUT High Setup	4.6		4.6		4.6		ns
t_{BH} CLKOUT High to $\overline{BR}$ Deasserted Hold Time	1.0		1.0		0.0		ns
Switching Characteristics							
t_{SD} CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Disable		4.5		4.5		4.5	ns
t_{SE} CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Enable		4.5		4.5		4.5	ns
t_{DBG} CLKOUT High to $\overline{BG}$ High Setup		6.0		5.5		3.6	ns
t_{EBG} CLKOUT High to $\overline{BG}$ Deasserted Hold Time		6.0		4.6		3.6	ns
t_{DBH} CLKOUT High to $\overline{BGH}$ High Setup		6.0		5.5		3.6	ns
t_{EBH} CLKOUT High to $\overline{BGH}$ Deasserted Hold Time		6.0		4.6		3.6	ns

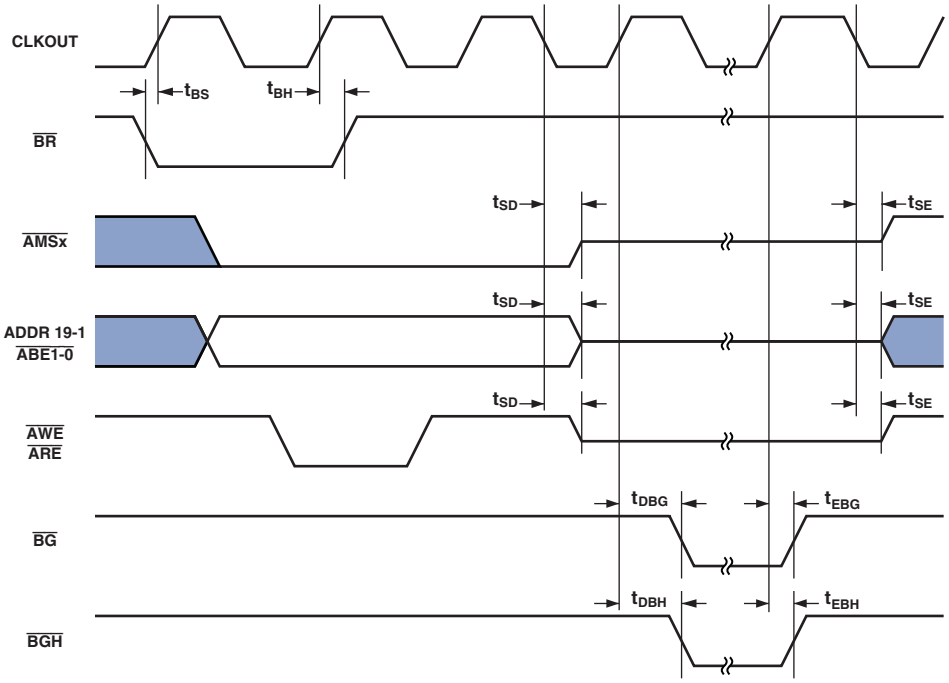


Figure 16. External Port Bus Request and Grant Cycle Timing

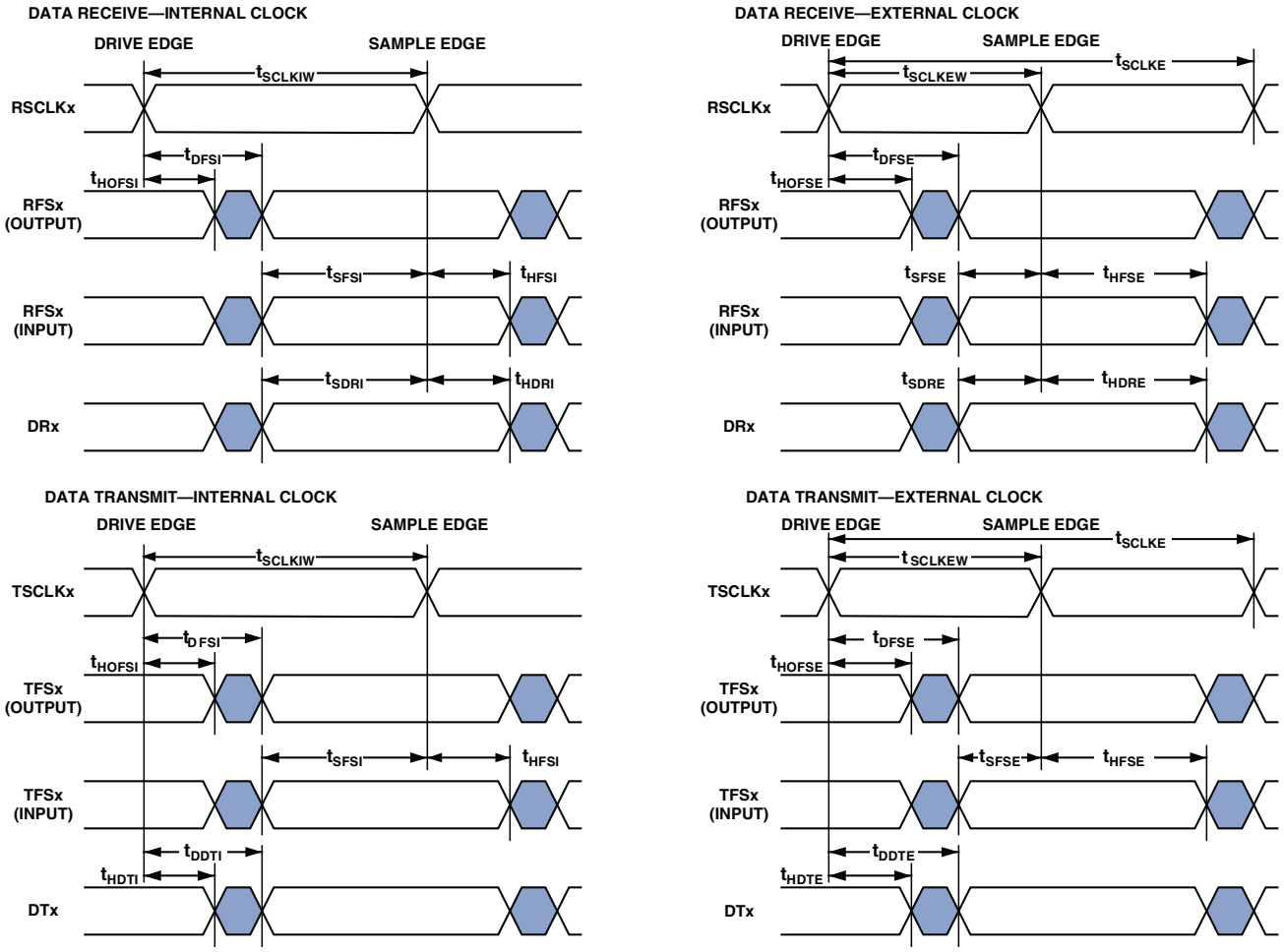


Figure 23. Serial Ports

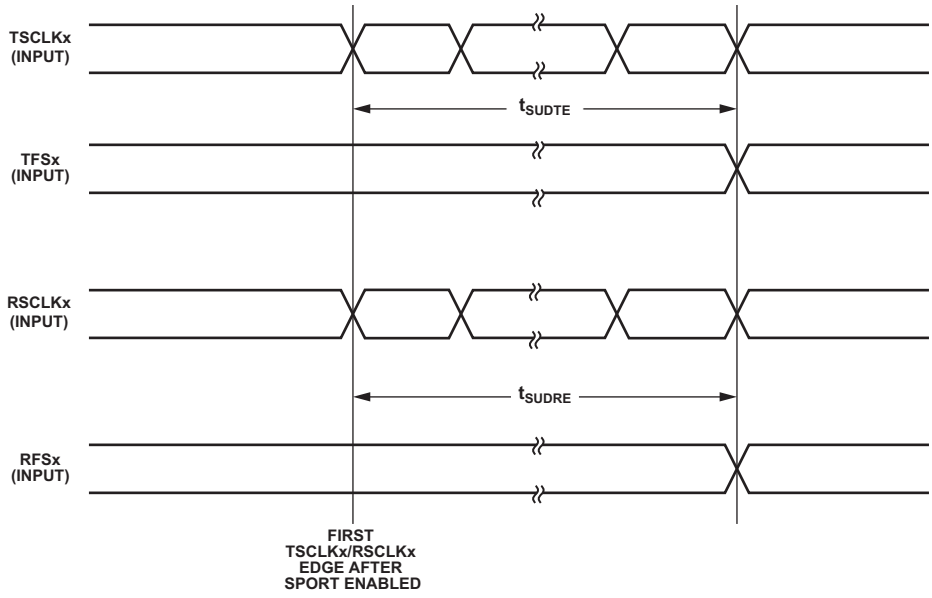


Figure 24. Serial Port Start Up with External Clock and Frame Sync

JTAG Test and Emulation Port Timing

Table 37. JTAG Port Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{TCK}	TCK Period	20		20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		4		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	5		5		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width[2] (Measured in TCK Cycles)	4		4		TCK
Switching Characteristics						
t_{DTDO}	TDO Delay from TCK Low		10		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0	12	0	12	ns

[1] System Inputs = DATA15–0, ARDY, TMR2–0, PF15–0, PPI_CLK, RSCLK0–1, RFS0–1, DR0PRI, DR0SEC, TSCLK0–1, TFS0–1, DR1PRI, DR1SEC, MOSI, MISO, SCK, RX, $\overline{RESET}$, NMI, BMODE1–0, $\overline{BR}$, PPI3–0.

[2] 50 MHz maximum.

[3] System Outputs = DATA15–0, ADDR19–1, $\overline{ABE1–0}$, $\overline{AOE}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AMS3–0}$, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SCKE, CLKOUT, SA10, $\overline{SMS}$, TMR2–0, PF15–0, RSCLK0–1, RFS0–1, TSCLK0–1, TFS0–1, DT0PRI, DT0SEC, DT1PRI, DT1SEC, MOSI, MISO, SCK, TX, $\overline{BG}$, $\overline{BGH}$, PPI3–0.

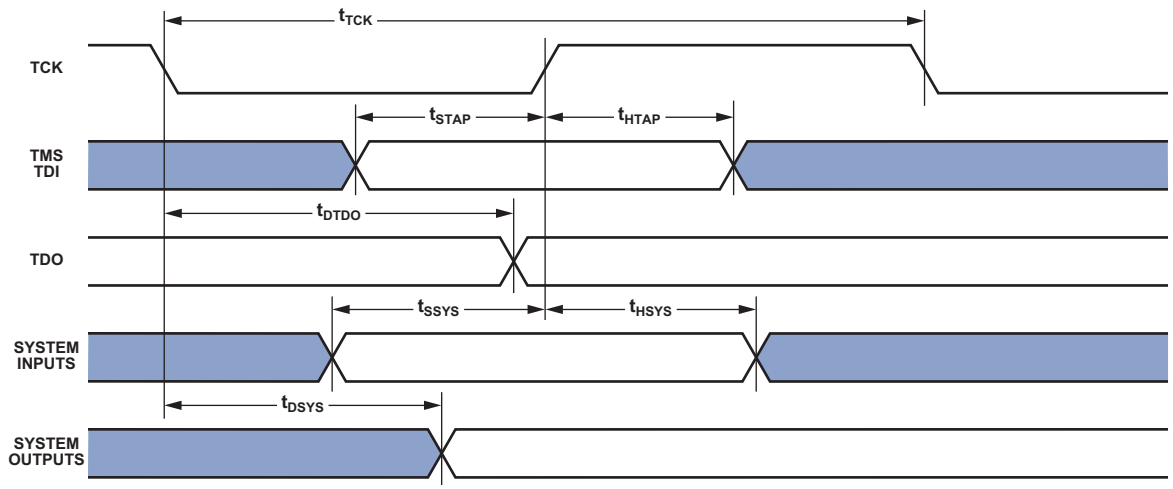


Figure 32. JTAG Port Timing

160-BALL CSP_BGA BALL ASSIGNMENT

Table 41 lists the CSP_BGA ball assignment by signal. Table 42 on Page 51 lists the CSP_BGA ball assignment by ball number.

Table 41. 160-Ball CSP_BGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{ABE0}$	H13	DATA4	N8	GND	L6	SCK	D1
$\overline{ABE1}$	H12	DATA5	P8	GND	L8	SCKE	B13
ADDR1	J14	DATA6	M7	GND	L10	$\overline{SMS}$	C13
ADDR2	K14	DATA7	N7	GND	M4	$\overline{SRAS}$	D13
ADDR3	L14	DATA8	P7	GND	M10	$\overline{SWE}$	D12
ADDR4	J13	DATA9	M6	GND	P14	TCK	P2
ADDR5	K13	DATA10	N6	MISO	E2	TDI	M3
ADDR6	L13	DATA11	P6	MOSI	D3	TDO	N3
ADDR7	K12	DATA12	M5	NMI	B10	TFS0	H3
ADDR8	L12	DATA13	N5	PF0	D2	TFS1	E1
ADDR9	M12	DATA14	P5	PF1	C1	TMR0	L2
ADDR10	M13	DATA15	P4	PF2	C2	TMR1	M1
ADDR11	M14	DR0PRI	K1	PF3	C3	TMR2	K2
ADDR12	N14	DR0SEC	J2	PF4	B1	TMS	N2
ADDR13	N13	DR1PRI	G3	PF5	B2	$\overline{TRST}$	N1
ADDR14	N12	DR1SEC	F3	PF6	B3	TSCLK0	J1
ADDR15	M11	DT0PRI	H1	PF7	B4	TSCLK1	F1
ADDR16	N11	DT0SEC	H2	PF8	A2	TX	K3
ADDR17	P13	DT1PRI	F2	PF9	A3	V_{DDEXT}	A1
ADDR18	P12	DT1SEC	E3	PF10	A4	V_{DDEXT}	C7
ADDR19	P11	$\overline{EMU}$	M2	PF11	A5	V_{DDEXT}	C12
$\overline{AMS0}$	E14	GND	A10	PF12	B5	V_{DDEXT}	D5
$\overline{AMS1}$	F14	GND	A14	PF13	B6	V_{DDEXT}	D9
$\overline{AMS2}$	F13	GND	B11	PF14	A6	V_{DDEXT}	F12
$\overline{AMS3}$	G12	GND	C4	PF15	C6	V_{DDEXT}	G4
$\overline{AOE}$	G13	GND	C5	PPI_CLK	C9	V_{DDEXT}	J4
ARDY	E13	GND	C11	PPI0	C8	V_{DDEXT}	J12
$\overline{ARE}$	G14	GND	D4	PPI1	B8	V_{DDEXT}	L7
$\overline{AWE}$	H14	GND	D7	PPI2	A7	V_{DDEXT}	L11
$\overline{BG}$	P10	GND	D8	PPI3	B7	V_{DDEXT}	P1
$\overline{BGH}$	N10	GND	D10	$\overline{RESET}$	C10	V_{DDINT}	D6
BMODE0	N4	GND	D11	RFS0	J3	V_{DDINT}	E4
BMODE1	P3	GND	F4	RFS1	G2	V_{DDINT}	E11
$\overline{BR}$	D14	GND	F11	RSCLK0	L1	V_{DDINT}	J11
CLKIN	A12	GND	G11	RSCLK1	G1	V_{DDINT}	L4
CLKOUT	B14	GND	H4	RTXI	A9	V_{DDINT}	L9
DATA0	M9	GND	H11	RTXO	A8	V_{DDRTC}	B9
DATA1	N9	GND	K4	RX	L3	VROUT0	A13
DATA2	P9	GND	K11	SA10	E12	VROUT1	B12
DATA3	M8	GND	L5	$\overline{SCAS}$	C14	XTAL	A11

Figure 60 shows the top view of the CSP_BGA ball configuration. Figure 61 shows the bottom view of the CSP_BGA ball configuration.

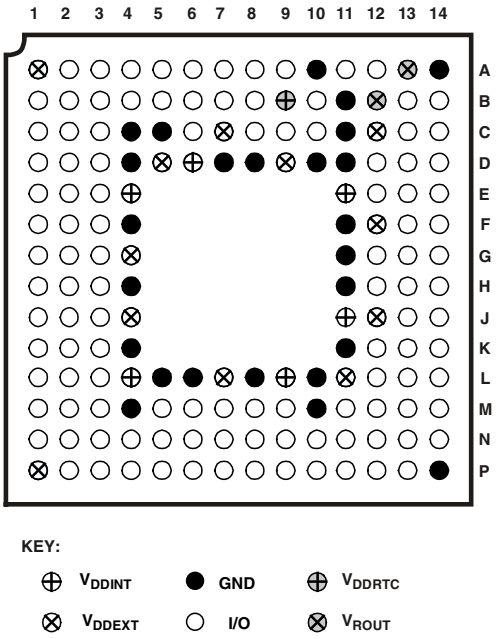


Figure 60. 160-Ball CSP_BGA Ground Configuration (Top View)

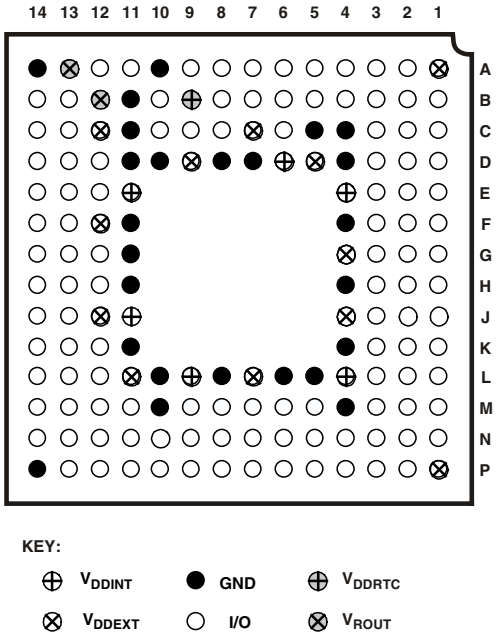


Figure 61. 160-Ball CSP_BGA Ground Configuration (Bottom View)

169-BALL PBGA BALL ASSIGNMENT

Table 43 lists the PBGA ball assignment by signal. Table 44 on Page 54 lists the PBGA ball assignment by ball number.

Table 43. 169-Ball PBGA Ball Assignment (Alphabetical by Signal)

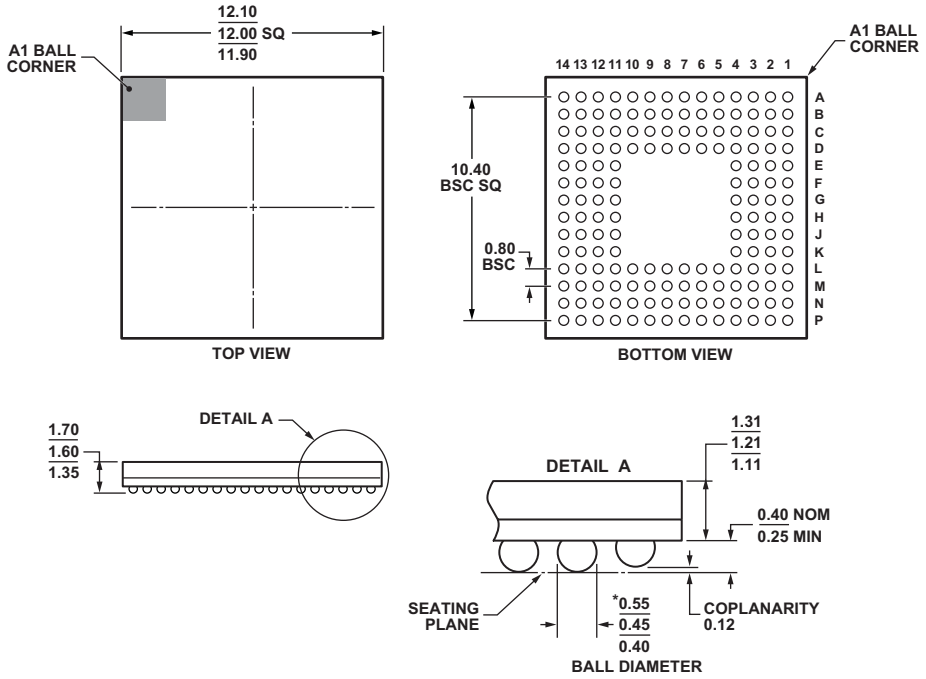
Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{ABE0}$	H16	DATA4	U12	GND	K9	RTXI	A10	V_{DDEXT}	K6
$\overline{ABE1}$	H17	DATA5	U11	GND	K10	RTXO	A11	V_{DDEXT}	L6
ADDR1	J16	DATA6	T10	GND	K11	RX	T1	V_{DDEXT}	M6
ADDR2	J17	DATA7	U10	GND	L7	SA10	B15	V_{DDEXT}	M7
ADDR3	K16	DATA8	T9	GND	L8	$\overline{SCAS}$	A16	V_{DDEXT}	M8
ADDR4	K17	DATA9	U9	GND	L9	SCK	D1	V_{DDEXT}	T2
ADDR5	L16	DATA10	T8	GND	L10	SCKE	B14	VROUT0	B12
ADDR6	L17	DATA11	U8	GND	L11	$\overline{SMS}$	A17	VROUT1	B13
ADDR7	M16	DATA12	U7	GND	M9	$\overline{SRAS}$	A15	XTAL	A13
ADDR8	M17	DATA13	T7	GND	T16	$\overline{SWE}$	B17		
ADDR9	N17	DATA14	U6	MISO	E2	TCK	U4		
ADDR10	N16	DATA15	T6	MOSI	E1	TDI	U3		
ADDR11	P17	DR0PRI	M2	NMI	B11	TDO	T4		
ADDR12	P16	DR0SEC	M1	PF0	D2	TFS0	L1		
ADDR13	R17	DR1PRI	H1	PF1	C1	TFS1	G2		
ADDR14	R16	DR1SEC	H2	PF2	B1	TMR0	R1		
ADDR15	T17	DT0PRI	K2	PF3	C2	TMR1	P2		
ADDR16	U15	DT0SEC	K1	PF4	A1	TMR2	P1		
ADDR17	T15	DT1PRI	F1	PF5	A2	TMS	T3		
ADDR18	U16	DT1SEC	F2	PF6	B3	$\overline{TRST}$	U2		
ADDR19	T14	$\overline{EMU}$	U1	PF7	A3	TSCLK0	L2		
$\overline{AMS0}$	D17	GND	B16	PF8	B4	TSCLK1	G1		
$\overline{AMS1}$	E16	GND	F11	PF9	A4	TX	R2		
$\overline{AMS2}$	E17	GND	G7	PF10	B5	VDD	F12		
$\overline{AMS3}$	F16	GND	G8	PF11	A5	VDD	G12		
$\overline{AOE}$	F17	GND	G9	PF12	A6	VDD	H12		
ARDY	C16	GND	G10	PF13	B6	VDD	J12		
$\overline{ARE}$	G16	GND	G11	PF14	A7	VDD	K12		
$\overline{AWE}$	G17	GND	H7	PF15	B7	VDD	L12		
$\overline{BG}$	T13	GND	H8	PPI_CLK	B10	VDD	M10		
$\overline{BGH}$	U17	GND	H9	PPI0	B9	VDD	M11		
BMODE0	U5	GND	H10	PPI1	A9	VDD	M12		
BMODE1	T5	GND	H11	PPI2	B8	V_{DDEXT}	B2		
$\overline{BR}$	C17	GND	J7	PPI3	A8	V_{DDEXT}	F6		
CLKIN	A14	GND	J8	$\overline{RESET}$	A12	V_{DDEXT}	F7		
CLKOUT	D16	GND	J9	RFS0	N1	V_{DDEXT}	F8		
DATA0	U14	GND	J10	RFS1	J1	V_{DDEXT}	F9		
DATA1	T12	GND	J11	RSCLK0	N2	V_{DDEXT}	G6		
DATA2	U13	GND	K7	RSCLK1	J2	V_{DDEXT}	H6		
DATA3	T11	GND	K8	RTCVDD	F10	V_{DDEXT}	J6		

176-LEAD LQFP PINOUT

Table 45 lists the LQFP pinout by signal. Table 46 on Page 57 lists the LQFP pinout by lead number.

Table 45. 176-Lead LQFP Pin Assignment (Alphabetical by Signal)

Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.
$\overline{ABE0}$	151	DATA3	113	GND	88	PPI_CLK	21	V_{DDEXT}	71
$\overline{ABE1}$	150	DATA4	112	GND	89	PPI0	22	V_{DDEXT}	93
ADDR1	149	DATA5	110	GND	90	PPI1	23	V_{DDEXT}	107
ADDR2	148	DATA6	109	GND	91	PPI2	24	V_{DDEXT}	118
ADDR3	147	DATA7	108	GND	92	PPI3	26	V_{DDEXT}	134
ADDR4	146	DATA8	105	GND	97	$\overline{RESET}$	13	V_{DDEXT}	145
ADDR5	142	DATA9	104	GND	106	RFS0	75	V_{DDEXT}	156
ADDR6	141	DATA10	103	GND	117	RFS1	64	V_{DDEXT}	171
ADDR7	140	DATA11	102	GND	128	RSCLK0	76	V_{DDINT}	25
ADDR8	139	DATA12	101	GND	129	RSCLK1	65	V_{DDINT}	52
ADDR9	138	DATA13	100	GND	130	RTXI	17	V_{DDINT}	66
ADDR10	137	DATA14	99	GND	131	RTXO	16	V_{DDINT}	80
ADDR11	136	DATA15	98	GND	132	RX	82	V_{DDINT}	111
ADDR12	135	DR0PRI	74	GND	133	SA10	164	V_{DDINT}	143
ADDR13	127	DR0SEC	73	GND	144	$\overline{SCAS}$	166	V_{DDINT}	157
ADDR14	126	DR1PRI	63	GND	155	SCK	53	V_{DDINT}	168
ADDR15	125	DR1SEC	62	GND	170	SCKE	173	V_{DDRTC}	18
ADDR16	124	DT0PRI	68	GND	174	$\overline{SMS}$	172	VROUT0	5
ADDR17	123	DT0SEC	67	GND	175	$\overline{SRAS}$	167	VROUT1	4
ADDR18	122	DT1PRI	59	GND	176	$\overline{SWE}$	165	XTAL	11
ADDR19	121	DT1SEC	58	MISO	54	TCK	94		
$\overline{AMS0}$	161	$\overline{EMU}$	83	MOSI	55	TDI	86		
$\overline{AMS1}$	160	GND	1	NMI	14	TDO	87		
$\overline{AMS2}$	159	GND	2	PF0	51	TFS0	69		
$\overline{AMS3}$	158	GND	3	PF1	50	TFS1	60		
$\overline{AOE}$	154	GND	7	PF2	49	TMR0	79		
ARDY	162	GND	8	PF3	48	TMR1	78		
$\overline{ARE}$	153	GND	9	PF4	47	TMR2	77		
$\overline{AWE}$	152	GND	15	PF5	46	TMS	85		
$\overline{BG}$	119	GND	19	PF6	38	$\overline{TRST}$	84		
$\overline{BGH}$	120	GND	30	PF7	37	TSCLK0	72		
BMODE0	96	GND	39	PF8	36	TSCLK1	61		
BMODE1	95	GND	40	PF9	35	TX	81		
$\overline{BR}$	163	GND	41	PF10	34	V_{DDEXT}	6		
CLKIN	10	GND	42	PF11	33	V_{DDEXT}	12		
CLKOUT	169	GND	43	PF12	32	V_{DDEXT}	20		
DATA0	116	GND	44	PF13	29	V_{DDEXT}	31		
DATA1	115	GND	56	PF14	28	V_{DDEXT}	45		
DATA2	114	GND	70	PF15	27	V_{DDEXT}	57		



*COMPLIANT TO JEDEC STANDARDS MO-205-AE WITH THE EXCEPTION TO BALL DIAMETER.

Figure 65. 160-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-160-2)
Dimensions shown in millimeters

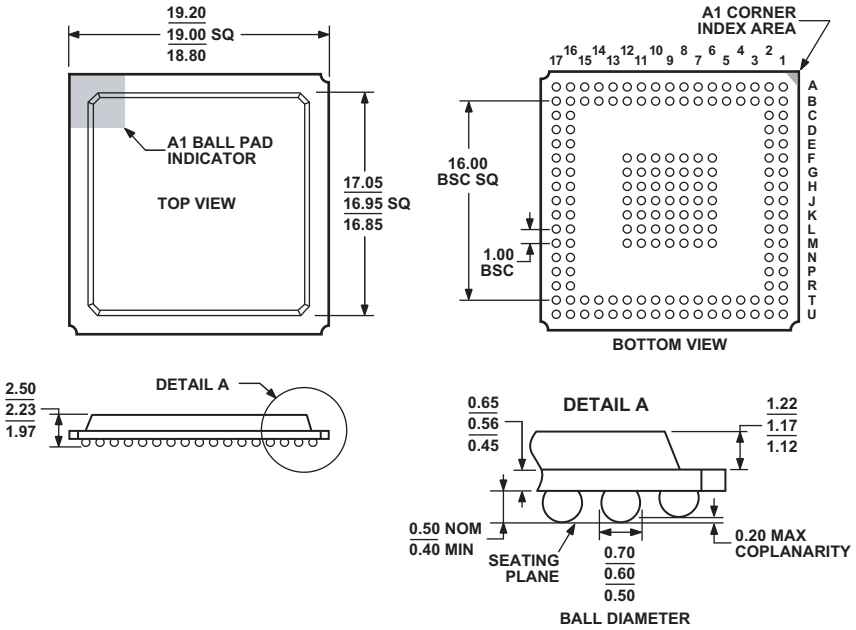


Figure 66. 169-Ball Plastic Ball Grid Array [PBGA]
(B-169)
Dimensions shown in millimeters

ORDERING GUIDE

Model [1]	Temperature Range [2]	Speed Grade (Max)	Package Description	Package Option
ADSP-BF531SBB400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF531SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF531SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF531SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF531SBBCZ4RL	–40°C to +85°C	400 MHz	160-Ball CSP_BGA, 13" Tape and Reel	BC-160-2
ADSP-BF531SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF532SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF532SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF532SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF532SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF533SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF533SBB500	–40°C to +85°C	500 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBZ500	–40°C to +85°C	500 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBC500	–40°C to +85°C	500 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ500	–40°C to +85°C	500 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBC-5V	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ-5V	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKBC-6V	0°C to +70°C	600 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKBCZ-6V	0°C to +70°C	600 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKSTZ-5V	0°C to +70°C	533 MHz	176-Lead LQFP	ST-176-1

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 20 for junction temperature (T_J) specification which is the only temperature specification.