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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	400MHz
Non-Volatile Memory	ROM (1kB)
On-Chip RAM	52kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-BBGA
Supplier Device Package	169-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf531sbbz400

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BLACKFIN PROCESSOR CORE

As shown in Figure 2 on Page 5, the Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-bit, 16-bit, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo 2^{32} multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions includes byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). Quad 16-bit operations are possible using the second ALU.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

MEMORY ARCHITECTURE

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors view memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low latency on-chip memory as cache or SRAM, and larger, lower cost and performance off-chip memory systems. See Figure 3, Figure 4, and Figure 5 on Page 6.

The L1 memory system is the primary highest performance memory available to the Blackfin processor. The off-chip memory system, accessed through the external bus interface unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing up to 132M bytes of physical memory.

The memory DMA controller provides high bandwidth data-movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

Internal (On-Chip) Memory

The processors have three blocks of on-chip memory that provide high bandwidth access to the core.

The first block is the L1 instruction memory, consisting of up to 80K bytes SRAM, of which 16K bytes can be configured as a four way set-associative cache. This memory is accessed at full processor speed.

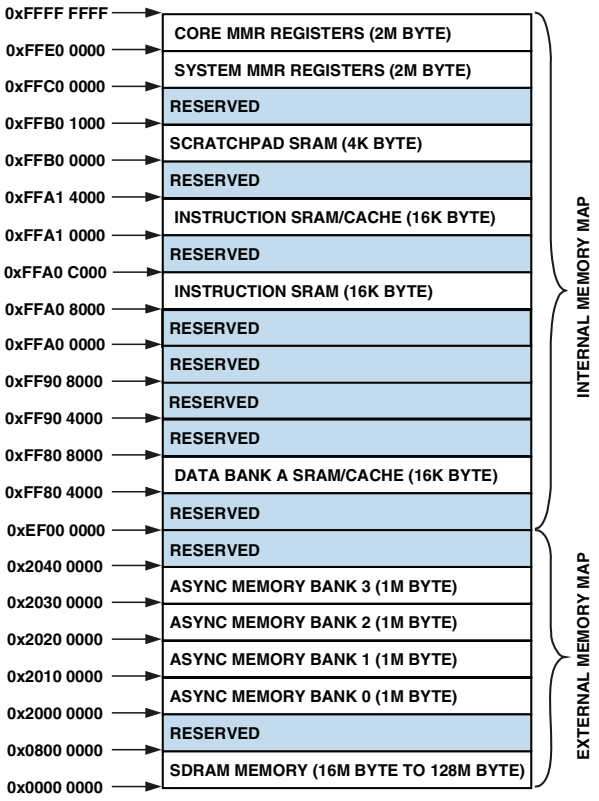


Figure 3. ADSP-BF531 Internal/External Memory Map

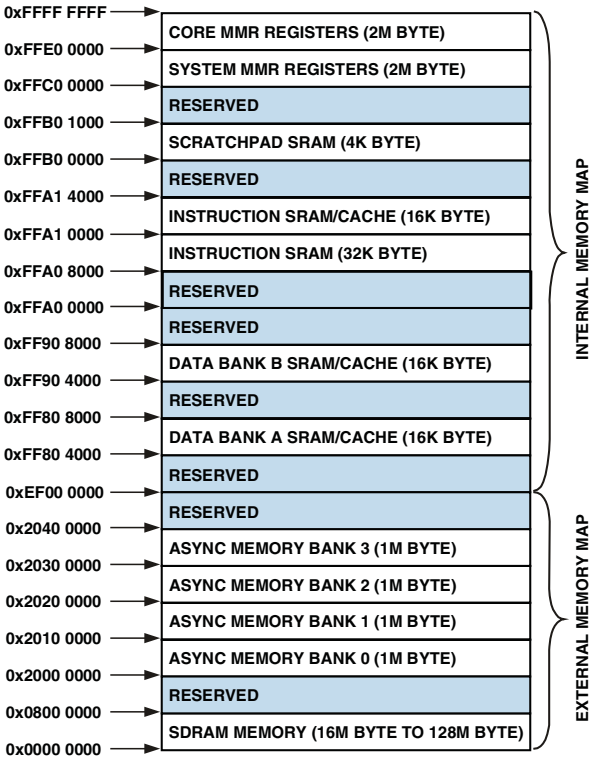


Figure 4. ADSP-BF532 Internal/External Memory Map

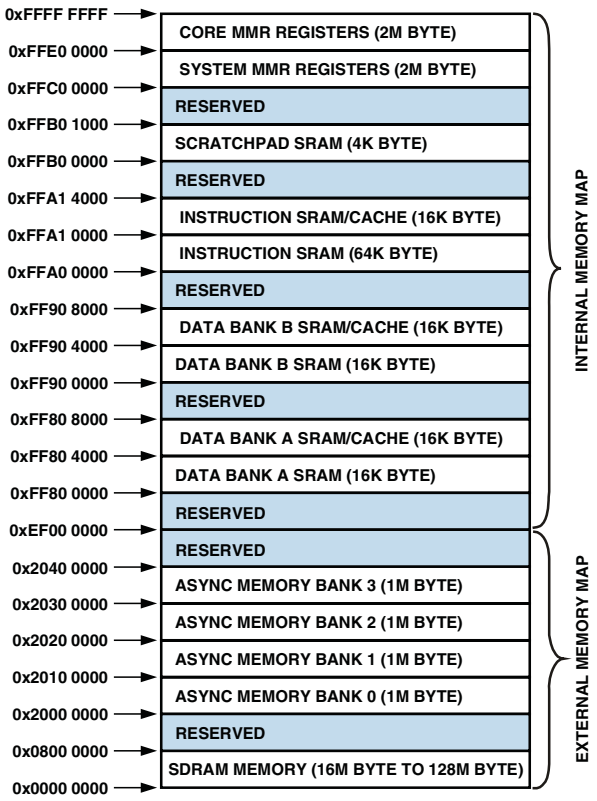


Figure 5. ADSP-BF533 Internal/External Memory Map

Event Handling

The event controller on the processors handle all asynchronous and synchronous events to the processor. The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provide event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher priority event takes precedence over servicing of a lower priority event. The controller provides support for five different types of events:

- Emulation – An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- Reset – This event resets the processor.
- Nonmaskable Interrupt (NMI) – The NMI event can be generated by the software watchdog timer or by the NMI input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- Exceptions – Events that occur synchronously to program flow (i.e., the exception is taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts – Events that occur asynchronously to program flow. They are caused by input pins, timers, and other peripherals, as well as by an explicit software instruction.

Each event type has an associated register to hold the return address and an associated return-from-event instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors' event controller consists of two stages, the core event controller (CEC) and the system interrupt controller (SIC). The core event controller works with the system interrupt controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC, and are then routed directly into the general-purpose interrupts of the CEC.

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the processor. Table 2 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

Table 2. Core Event Controller (CEC)

Priority (0 is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	Reset	RST
2	Nonmaskable Interrupt	NMI
3	Exception	EVX
4	Reserved	
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General Interrupt 7	IVG7
8	General Interrupt 8	IVG8
9	General Interrupt 9	IVG9
10	General Interrupt 10	IVG10
11	General Interrupt 11	IVG11
12	General Interrupt 12	IVG12
13	General Interrupt 13	IVG13
14	General Interrupt 14	IVG14
15	General Interrupt 15	IVG15

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processors provide a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). Table 3 describes the inputs into the SIC and the default mappings into the CEC.

Table 3. System Interrupt Controller (SIC)

Peripheral Interrupt Event	Default Mapping
PLL Wakeup	IVG7
DMA Error	IVG7
PPI Error	IVG7
SPORT 0 Error	IVG7
SPORT 1 Error	IVG7
SPI Error	IVG7
UART Error	IVG7
Real-Time Clock	IVG8
DMA Channel 0 (PPI)	IVG8
DMA Channel 1 (SPORT 0 Receive)	IVG9
DMA Channel 2 (SPORT 0 Transmit)	IVG9
DMA Channel 3 (SPORT 1 Receive)	IVG9
DMA Channel 4 (SPORT 1 Transmit)	IVG9
DMA Channel 5 (SPI)	IVG10
DMA Channel 6 (UART Receive)	IVG10
DMA Channel 7 (UART Transmit)	IVG10
Timer 0	IVG11
Timer 1	IVG11
Timer 2	IVG11
Port F GPIO Interrupt A	IVG12
Port F GPIO Interrupt B	IVG12
Memory DMA Stream 0	IVG13
Memory DMA Stream 1	IVG13
Software Watchdog Timer	IVG13

Event Control

The processors provide a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 32 bits wide:

- CEC interrupt latch register (ILAT) – The ILAT register indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it can also be written to clear (cancel) latched events. This register can be read while in supervisor mode and can only be written while in supervisor mode when the corresponding IMASK bit is cleared.
- CEC interrupt mask register (IMASK) – The IMASK register controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and is processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be latched in the ILAT register. This register can be read or written while in supervisor mode. Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.

- CEC interrupt pending register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but can be read while in supervisor mode.

The SIC allows further control of event processing by providing three 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in Table 3.

- SIC interrupt mask register (SIC_IMASK) – This register controls the masking and unmasking of each peripheral interrupt event. When a bit is set in this register, that peripheral event is unmasked and is processed by the system when asserted. A cleared bit in this register masks the peripheral event, preventing the processor from servicing the event.
- SIC interrupt status register (SIC_ISR) – As multiple peripherals can be mapped to a single event, this register allows the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt, and a cleared bit indicates the peripheral is not asserting the event.
- SIC interrupt wakeup enable register (SIC_IWR) – By enabling the corresponding bit in this register, a peripheral can be configured to wake up the processor, should the core be idled when the event is generated. See Dynamic Power Management on Page 11.

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC recognizes and queues the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

DMA CONTROLLERS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have multiple, independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the SPORTs, SPI port, UART, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The DMA controller supports both 1-dimensional (1-D) and 2-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, autorefreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two pairs of memory DMA channels provided for transfers between the various memories of the processor system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

REAL-TIME CLOCK

The processor real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors. The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60 second counter, a 60 minute counter, a 24 hour counter, and a 32,768 day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. The two alarms are time of day and a day and time of that day.

t_{NOM} is the duration running at $f_{CCLKNOM}$

t_{RED} is the duration running at $f_{CCLKRED}$

The percent power savings is calculated as:

$$\%\ power\ savings\ =\ (1 - power\ savings\ factor) \times 100\%$$

VOLTAGE REGULATION

The Blackfin processor provides an on-chip voltage regulator that can generate appropriate V_{DDINT} voltage levels from the V_{DDEXT} supply. See Operating Conditions on Page 20 for regulator tolerances and acceptable V_{DDEXT} ranges for specific models.

Figure 7 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power (V_{DDEXT}) supplied. While in the hibernate state, I/O power is still being applied, eliminating the need for external buffers. The voltage regulator can be activated from this power-down state either through an RTC wakeup or by asserting $\overline{\text{RESET}}$, both of which initiate a boot sequence. The regulator can also be disabled and bypassed at the user's discretion.

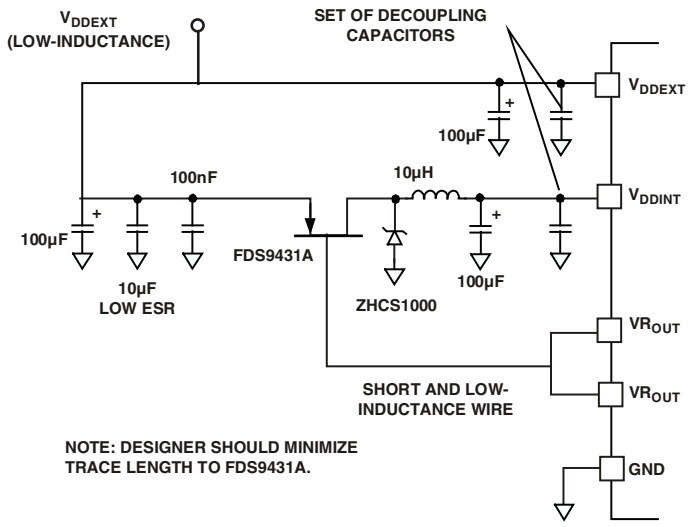


Figure 7. Voltage Regulator Circuit

Voltage Regulator Layout Guidelines

Regulator external component placement, board routing, and bypass capacitors all have a significant effect on noise injected into the other analog circuits on-chip. The VROUT1–0 traces and voltage regulator external components should be considered as noise sources when doing board layout and should not be routed or placed near sensitive circuits or components on the board. All internal and I/O power supplies should be well bypassed with bypass capacitors placed as close to the processors as possible.

For further details on the on-chip voltage regulator and related board design guidelines, see the *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228)* applications note on the Analog Devices web site (www.analog.com)—use site search on "EE-228".

CLOCK SIGNALS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the processors include an on-chip oscillator circuit, an external crystal can be used. For fundamental frequency operation, use the circuit shown in Figure 8.

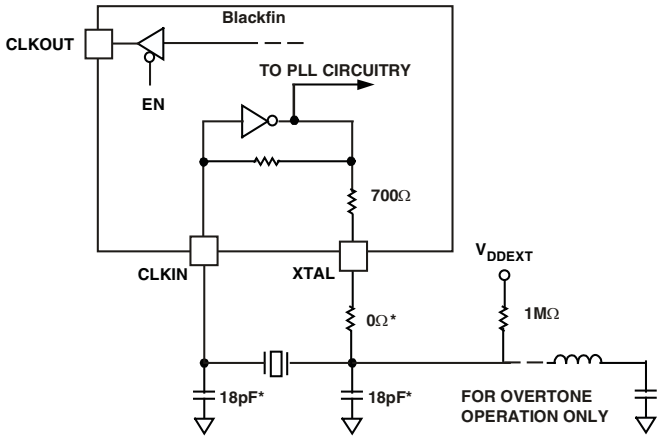


Figure 8. External Crystal Connections

A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor shown in Figure 8 fine tune the phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 8 are typical values only. The capacitor values are dependent upon the crystal manufacturer's load capacitance recommendations and the physical PCB layout. The resistor value depends on the drive level specified by the crystal manufacturer. System designs should verify the customized values based on careful investigation on multiple devices over the allowed temperature range.

A third-overtone crystal can be used at frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 8.

As shown in Figure 9, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a user programmable 0.5× to 64× multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 10×, but it can be modified by a software instruction sequence. On-the-fly frequency changes can be effected by simply writing to the PLL_DIV register.

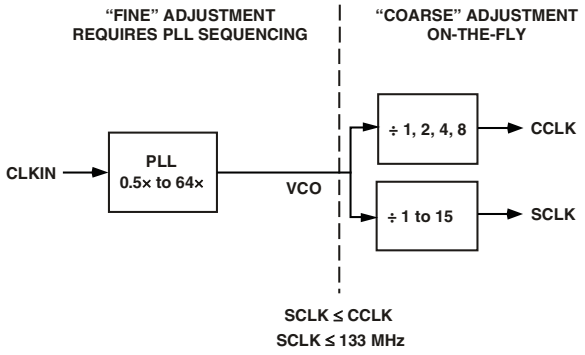


Figure 9. Frequency Modification Methods

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 6 illustrates typical system clock ratios.

Table 6. Example System Clock Ratios

Signal Name SSEL3–0	Divider Ratio VCO/SCLK	Example Frequency Ratios (MHz)	
		VCO	SCLK
0001	1:1	100	100
0101	5:1	400	80
1010	10:1	500	50

The maximum frequency of the system clock is f_{SCLK}. The divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV). When the SSEL value is changed, it affects all of the peripherals that derive their clock signals from the SCLK signal.

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 7. This programmable core clock capability is useful for fast core frequency modifications.

Table 7. Core Clock Ratios

Signal Name CSEL1–0	Divider Ratio VCO/CCLK	Example Frequency Ratios (MHz)	
		VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	400	100
11	8:1	200	25

BOOTING MODES

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have two mechanisms (listed in Table 8) for automatically loading internal L1 instruction memory after a reset. A third mode is provided to execute from external memory, bypassing the boot sequence.

Table 8. Booting Modes

BMODE1–0	Description
00	Execute from 16-bit external memory (bypass boot ROM)
01	Boot from 8-bit or 16-bit FLASH
10	Boot from serial master connected to SPI
11	Boot from serial slave EEPROM/flash (8-,16-, or 24-bit address range, or Atmel AT45DB041, AT45DB081, or AT45DB161serial flash)

The BMODE pins of the reset configuration register, sampled during power-on resets and software-initiated resets, implement the following modes:

- Execute from 16-bit external memory – Execution starts from address 0x2000 0000 with 16-bit packing. The boot ROM is bypassed in this mode. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).
- Boot from 8-bit or 16-bit external flash memory – The flash boot routine located in boot ROM memory space is set up using asynchronous Memory Bank 0. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).
- Boot from SPI serial EEPROM/flash (8-, 16-, or 24-bit addressable, or Atmel AT45DB041, AT45DB081, or AT45DB161) – The SPI uses the PF2 output pin to select a single SPI EEPROM/flash device, submits a read command and successive address bytes (0x00) until a valid 8-, 16-, or 24-bit addressable EEPROM/flash device is detected, and begins clocking data into the processor at the beginning of L1 instruction memory.
- Boot from SPI serial master – The Blackfin processor operates in SPI slave mode and is configured to receive the bytes of the LDR file from an SPI host (master) agent. To hold off the host device from transmitting while the boot ROM is busy, the Blackfin processor asserts a GPIO pin, called host wait (HWAIT), to signal the host device not to send any

[5] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{TRST}$).
[6] Absolute value.
[7] Applies to three-statable pins.
[8] Applies to all signal pins.
[9] Guaranteed, but not tested.
[10] See the *ADSP-BF533 Blackfin Processor Hardware Reference Manual* for definitions of sleep, deep sleep, and hibernate operating modes.
[11] See Table 16 for the list of I_{DDINT} power vectors covered by various Activity Scaling Factors (ASF).

System designers should refer to *Estimating Power for the ADSP-BF531/BF532/BF533 Blackfin Processors (EE-229)*, which provides detailed information for optimizing designs for lowest power. All topics discussed in this section are described in detail in EE-229. Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 22 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 14 or Table 15), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 17).

The dynamic component is also subject to an Activity Scaling Factor (ASF) which represents application code running on the processor (Table 16).

Table 14. Static Current–500 MHz, 533 MHz, and 600 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})[2]														
T_J (°C)[2]	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V	1.45 V
–45	4.3	5.3	5.9	7.0	8.2	9.8	11.2	13.0	15.2	17.7	20.2	21.6	25.5	30.1	32.0
0	18.8	21.3	24.1	27.8	31.6	35.6	40.1	45.3	51.4	58.1	65.0	68.5	78.4	89.8	94.3
25	35.3	39.9	45.0	50.9	57.3	64.4	72.9	80.9	90.3	101.4	112.1	118.0	133.7	151.6	158.7
40	52.3	58.5	65.1	73.3	81.3	90.9	101.2	112.5	125.5	138.7	154.4	160.6	180.6	203.1	212.0
55	73.6	82.5	92.0	102.7	114.4	126.3	141.2	155.7	172.7	191.1	212.1	220.8	247.6	277.7	289.5
70	100.8	112.5	124.5	137.4	152.6	168.4	186.5	205.4	227.0	250.3	276.2	287.1	320.4	357.4	371.9
85	133.3	148.5	164.2	180.5	198.8	219.0	241.0	264.5	290.6	319.7	350.2	364.6	404.9	449.7	467.2
100	178.3	196.3	216.0	237.6	259.9	284.6	311.9	342.0	373.1	408.0	446.1	462.6	511.1	564.7	585.6
115	223.3	245.9	270.2	295.7	323.5	353.3	386.1	421.1	460.1	500.9	545.0	566.5	624.3	688.1	712.8
125	278.5	305.8	334.1	364.3	397.4	432.4	470.6	509.3	553.4	600.6	652.1	676.5	742.1	814.1	841.9

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 20.

Table 15. Static Current–400 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})[2]											
T_J (°C)[2]	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V
–45	0.9	1.1	1.3	1.5	1.8	2.2	2.6	3.1	3.8	4.4	5.0	5.4
0	3.3	3.7	4.2	4.8	5.5	6.3	7.2	8.1	8.9	10.1	11.2	11.9
25	7.5	8.4	9.4	10.0	11.2	12.6	14.1	15.5	17.2	19.0	21.2	21.9
40	12.0	13.1	14.3	15.9	17.4	19.4	21.5	23.5	25.8	28.1	30.8	32.0
55	18.3	20.0	21.9	23.6	26.0	28.2	30.8	33.7	36.8	39.8	43.4	45.0
70	27.7	30.3	32.6	35.3	38.2	41.7	45.2	49.0	52.8	57.6	62.4	64.2
85	38.2	41.7	44.9	48.6	52.7	57.3	61.7	66.7	72.0	77.5	83.9	86.5
100	54.1	58.1	63.2	67.8	73.2	78.8	84.9	91.5	98.4	106.0	113.8	117.2
115	73.9	80.0	86.3	91.9	99.1	106.6	114.1	122.4	131.1	140.9	151.1	155.5
125	98.7	106.3	113.8	122.1	130.8	140.2	149.7	160.4	171.9	183.8	197.0	202.4

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 20.

Table 16. Activity Scaling Factors

I_{DDINT} Power Vector[1]	Activity Scaling Factor (ASF)[2]
$I_{DD-PEAK}$	1.27
$I_{DD-HIGH}$	1.25
I_{DD-TYP}	1.00
I_{DD-APP}	0.86
I_{DD-NOP}	0.72
$I_{DD-IDLE}$	0.41

[1] See EE-229 for power vector definitions.
[2] All ASF values determined using a 10:1 CCLK:SCLK ratio.

Table 17. Dynamic Current (mA, with ASF = 1.0)[1]

	Voltage (V_{DDINT})[2]														
Frequency (MHz)[2]	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V	1.45 V
50	12.7	13.9	15.3	16.8	18.1	19.4	21.0	22.3	24.0	25.4	26.4	27.2	28.7	30.3	30.7
100	22.6	24.2	26.2	28.1	30.1	31.8	34.7	36.2	38.4	40.5	43.0	43.4	45.7	47.9	48.9
200	40.8	44.1	46.9	50.3	53.3	56.9	59.9	63.1	66.7	70.2	73.8	75.0	78.7	82.4	84.6
250	50.1	53.8	57.2	61.4	64.7	68.9	72.9	76.8	81.0	85.1	89.3	90.8	95.2	99.6	102.0
300	N/A	63.5	67.4	72.4	76.2	81.0	85.9	90.6	95.2	100.0	104.8	106.6	111.8	116.9	119.4
375	N/A	N/A	N/A	88.6	93.5	99.0	104.6	110.3	116.0	122.1	128.0	130.0	136.2	142.4	145.5
400	N/A	N/A	N/A	93.9	99.3	105.0	110.8	116.8	123.0	129.4	135.7	137.9	144.6	151.2	154.3
425	N/A	N/A	N/A	N/A	N/A	111.0	117.3	123.5	129.9	136.8	143.2	145.6	152.6	159.7	162.8
475	N/A	N/A	N/A	N/A	N/A	N/A	130.3	136.8	143.8	151.4	158.1	161.1	168.9	176.6	179.7
500	N/A	N/A	N/A	N/A	N/A	N/A	N/A	143.5	150.7	158.7	165.6	168.8	177.0	185.2	188.2
533	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	160.4	168.8	176.5	179.6	188.2	196.8	200.5
600	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	196.2	199.6	209.3	219.0	222.6

[1] The values are not guaranteed as stand-alone maximum specifications, they must be combined with static current per the equations of Electrical Characteristics on Page 22.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 20.

TIMING SPECIFICATIONS

Clock and Reset Timing

Table 21 and Figure 11 describe clock and reset operations. Per Absolute Maximum Ratings on Page 25, combinations of CLKIN and clock multipliers/divisors must not result in core/system clocks exceeding the maximum limits allowed for the processor, including system clock restrictions related to supply voltage.

Table 21. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN Period[1, 2, 3, 4]	25.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse	10.0		ns
t_{CKINH}	CLKIN High Pulse	10.0		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[5]	11 × t_{CKIN}		ns
t_{NOBOOT}	$\overline{\text{RESET}}$ Deassertion to First External Access Delay[6]	3 × t_{CKIN}	5 × t_{CKIN}	ns

[1] Applies to PLL bypass mode and PLL non bypass mode.
[2] CLKIN frequency must not change on the fly.
[3] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 11 on Page 21 through Table 13 on Page 21. Since the default behavior of the PLL is to multiply the CLKIN frequency by 10, the 400 MHz speed grade parts cannot use the full CLKIN period range.
[4] If the DF bit in the PLL_CTL register is set, then the maximum t_{CKIN} period is 50 ns.
[5] Applies after power-up sequence is complete. See Table 22 and Figure 12 for power-up reset timing.
[6] Applies when processor is configured in No Boot Mode (BMODE1-0 = b#00).

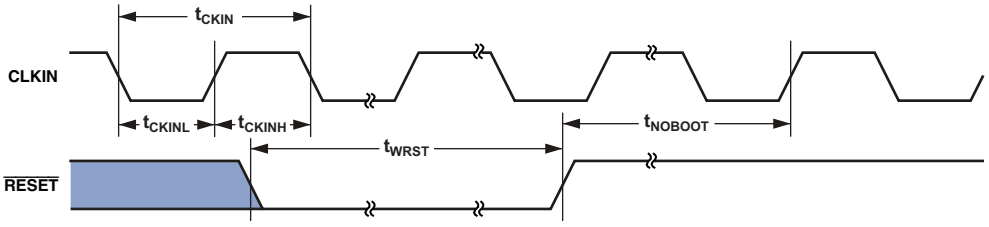
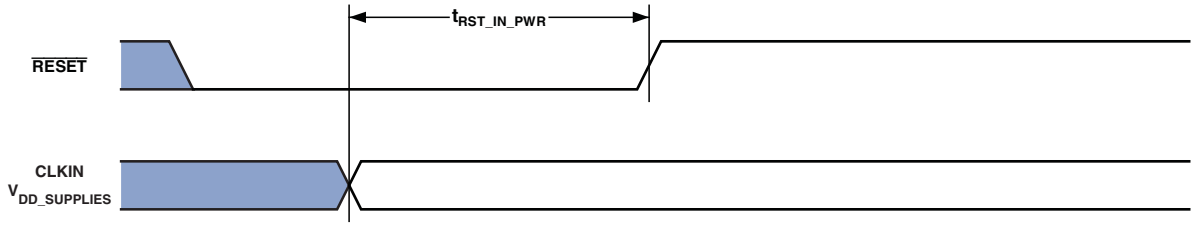


Figure 11. Clock and Reset Timing

Table 22. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted After the V_{DDINT}, V_{DDEXT}, V_{DDRTC}, and CLKIN Pins Are Stable and Within Specification	3500 × t_{CKIN}		ns



In Figure 12, $V_{DD\_SUPPLIES}$ is V_{DDINT}, V_{DDEXT}, V_{DDRTC}

Figure 12. Power-Up Reset Timing

Asynchronous Memory Write Cycle Timing

Table 24. Asynchronous Memory Write Cycle Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	1.0		0.0		ns
Switching Characteristics						
t_{DDAT}	DATA15–0 Disable After CLKOUT		6.0		6.0	ns
t_{ENDAT}	DATA15–0 Enable After CLKOUT	1.0		1.0		ns
t_{DO}	Output Delay After CLKOUT[1]		6.0		6.0	ns
t_{HO}	Output Hold After CLKOUT [1]	1.0		0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, DATA15–0, $\overline{AOE}$, $\overline{AWE}$.

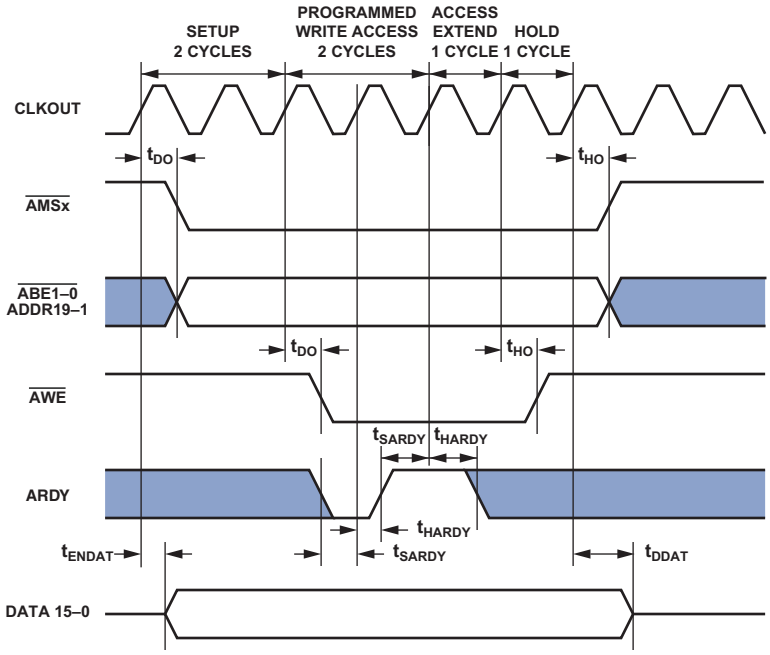


Figure 14. Asynchronous Memory Write Cycle Timing

Parallel Peripheral Interface Timing

Table 27 and Figure 17 through Figure 22 describe parallel peripheral interface operations.

Table 27. Parallel Peripheral Interface Timing

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Timing Requirements								
t_{PCLKW}	PPI_CLK Width	8.0		8.0		6.0		ns
t_{PCLK}	PPI_CLK Period[1]	20.0		20.0		15.0		ns
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK Edge (Nonsampling Edge for Rx, Sampling Edge for Tx)	6.0		6.0		4.0[2]		ns ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.0[2]		1.0[2]		1.0[2]		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	3.5		3.5		3.5		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	1.5		1.5		1.5		ns
Switching Characteristics—GP Output and Frame Capture Modes								
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		11.0		8.0		8.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	1.7		1.7		1.7		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		11.0		9.0		9.0	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	1.8		1.8		1.8		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$.
[2] Applies when PPI_CONTROL Bit 8 is cleared. See Figure 19 and Figure 22.

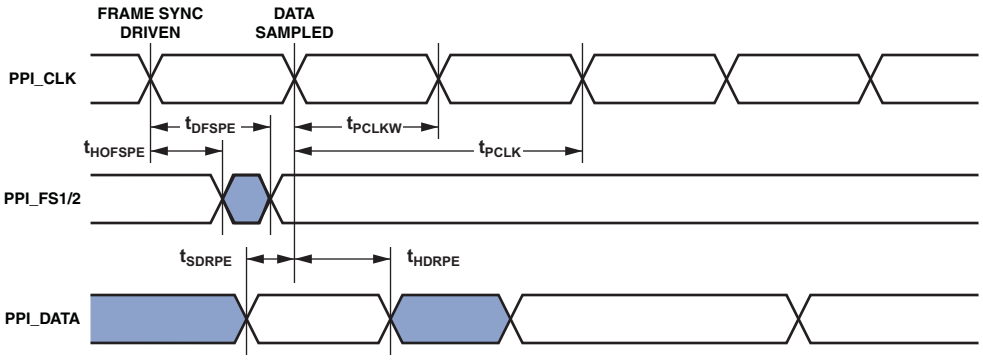


Figure 17. PPI GP Rx Mode with Internal Frame Sync Timing

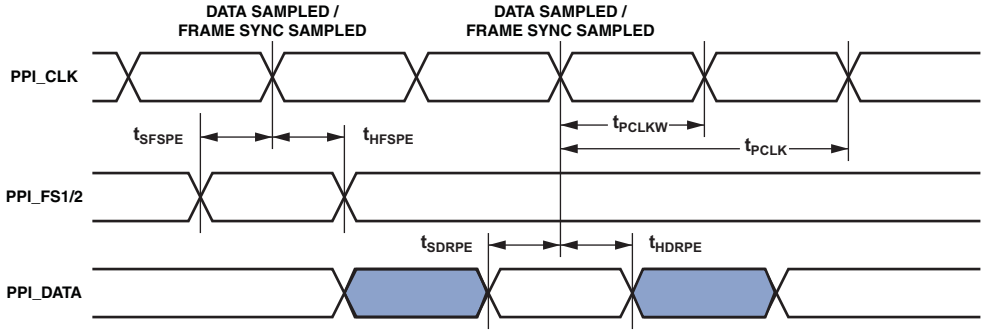


Figure 18. PPI GP Rx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 1)

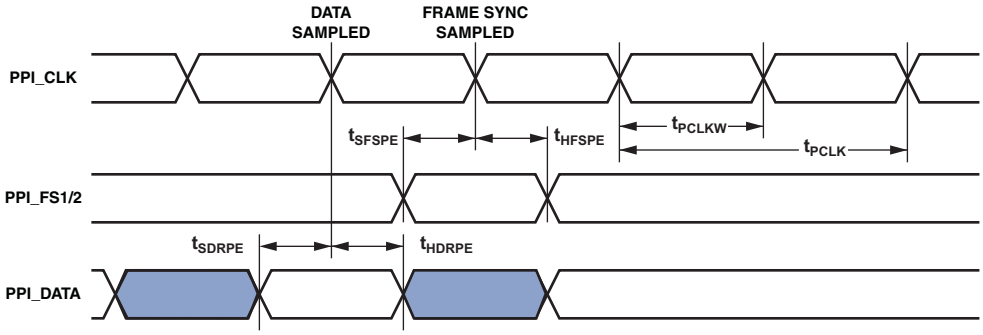


Figure 19. PPI GP Rx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 0)

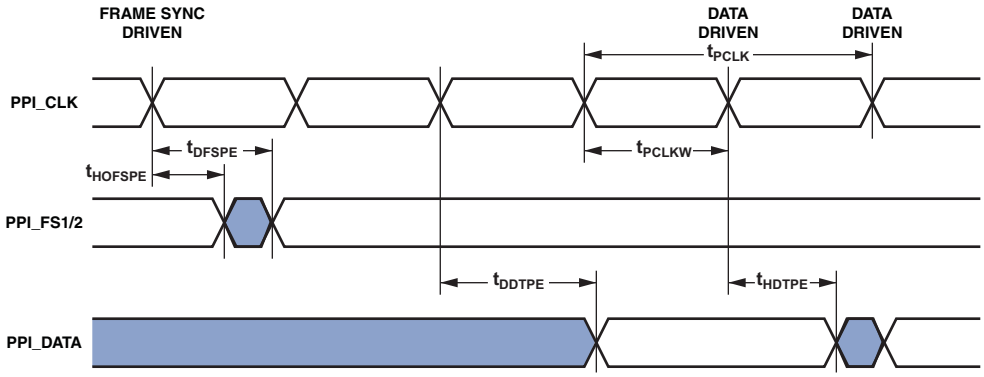


Figure 20. PPI GP Tx Mode with Internal Frame Sync Timing

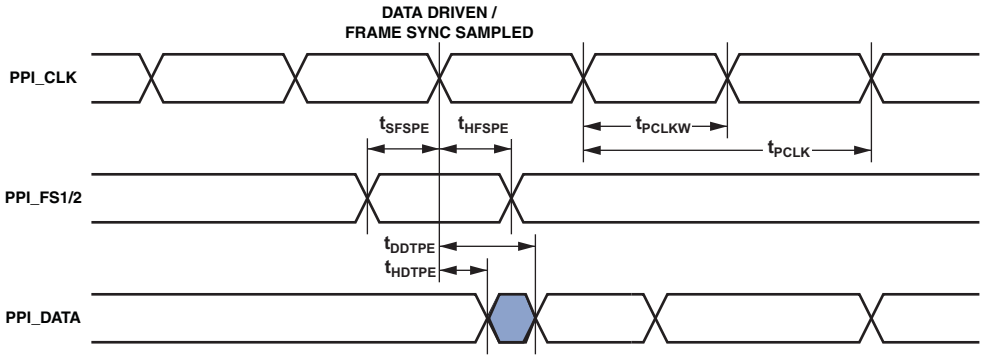


Figure 21. PPI GP Tx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 1)

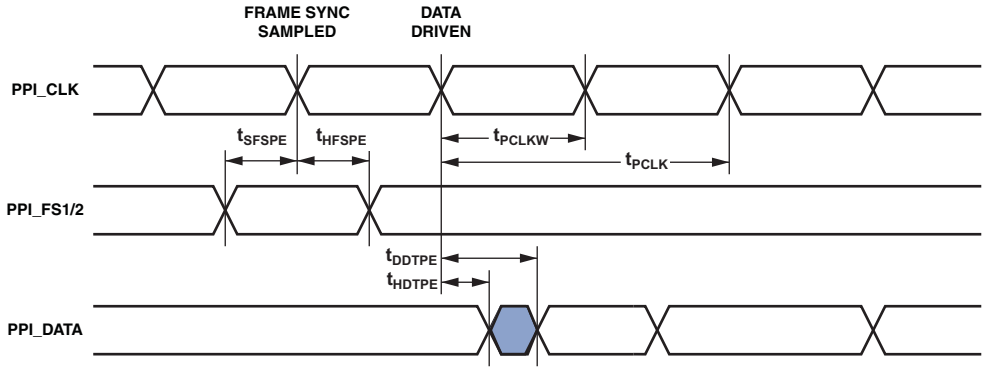


Figure 22. PPI GP Tx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 0)

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 33. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Timing Requirements								
t_{SPICHS}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK}$		$4 \times t_{SCLK}$		$4 \times t_{SCLK}$		ns
t_{HDS}	Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{SPISS}$ Assertion to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		1.6		1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	1.6		1.6		1.6		ns
Switching Characteristics								
t_{DSOE}	$\overline{SPISS}$ Assertion to Data Out Active	0	10	0	9	0	8	ns
t_{DSDHI}	$\overline{SPISS}$ Deassertion to Data High Impedance	0	10	0	9	0	8	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)		10		10		10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0		0		0		ns

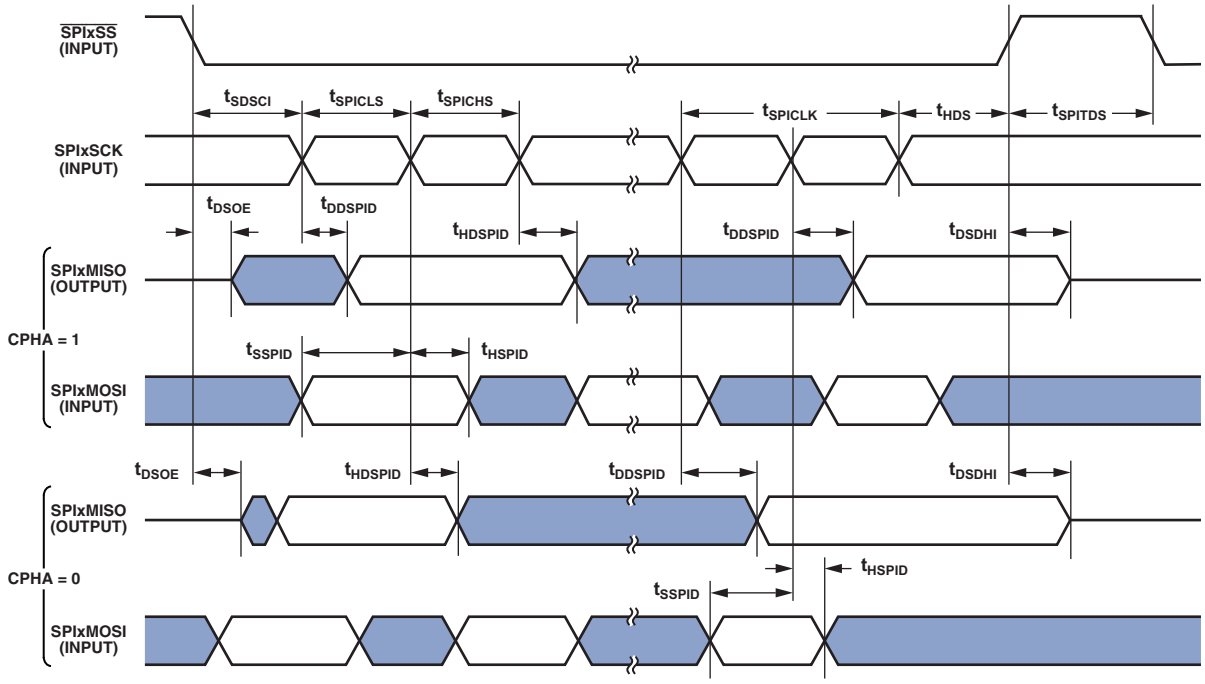


Figure 28. Serial Peripheral Interface (SPI) Port—Slave Timing

OUTPUT DRIVE CURRENTS

Figure 33 through Figure 44 show typical current-voltage characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

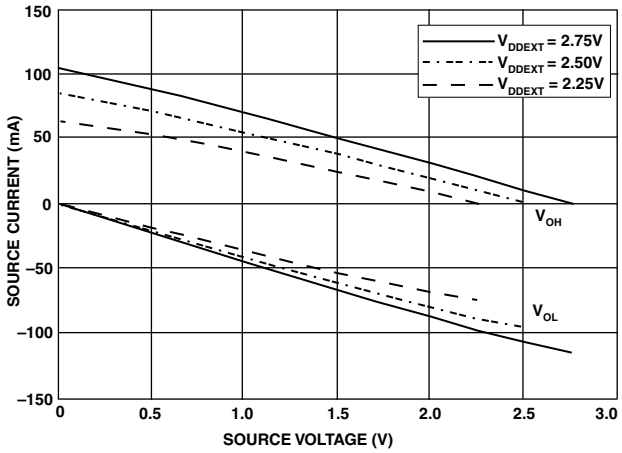


Figure 33. Drive Current A (V_{DDEXT} = 2.5 V)

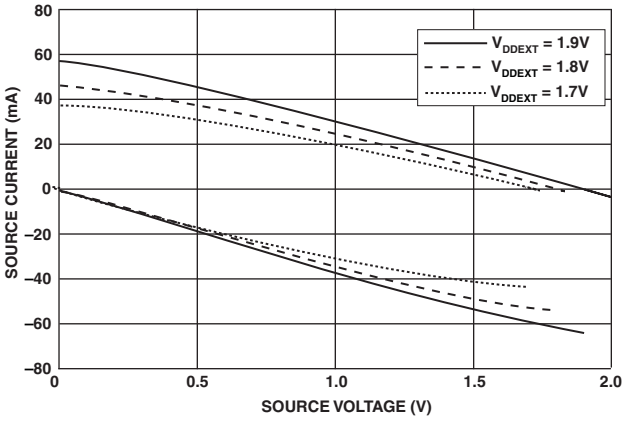


Figure 34. Drive Current A (V_{DDEXT} = 1.8 V)

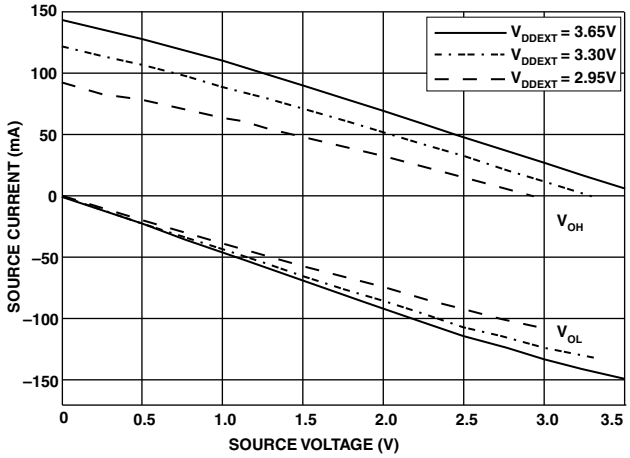


Figure 35. Drive Current A (V_{DDEXT} = 3.3 V)

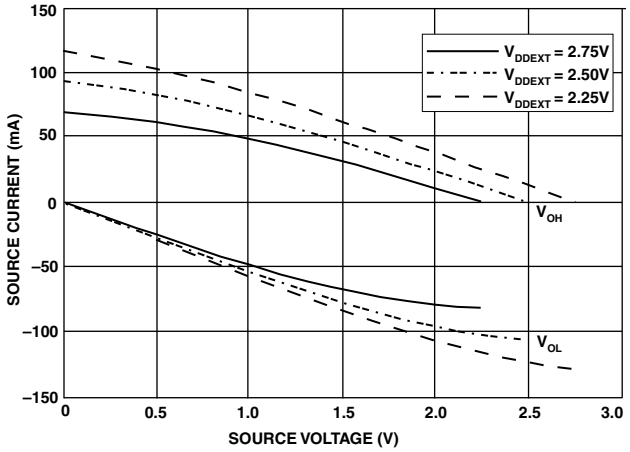


Figure 36. Drive Current B (V_{DDEXT} = 2.5 V)

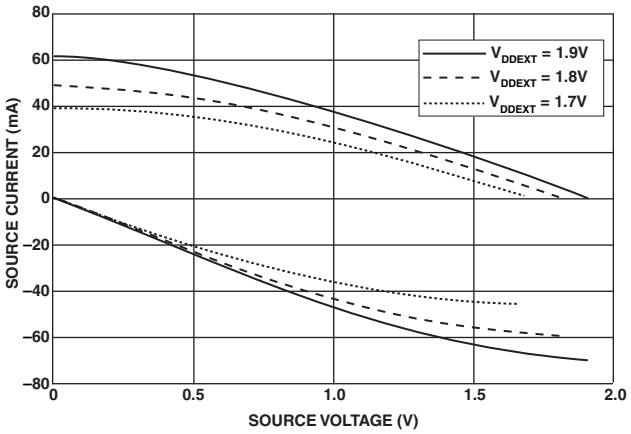


Figure 37. Drive Current B (V_{DDEXT} = 1.8 V)

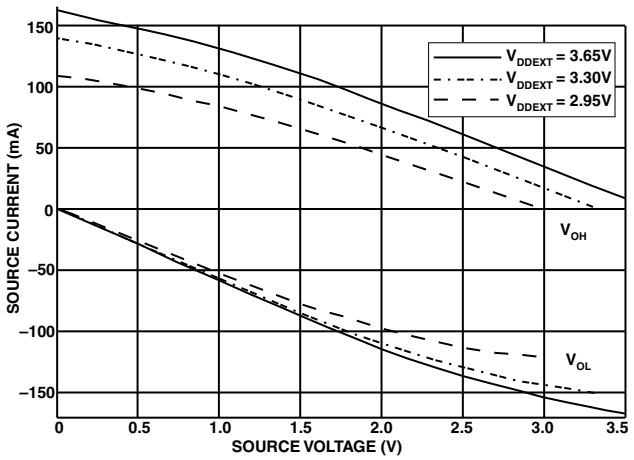


Figure 38. Drive Current B (V_{DDEXT} = 3.3 V)

160-BALL CSP_BGA BALL ASSIGNMENT

Table 41 lists the CSP_BGA ball assignment by signal. Table 42 on Page 51 lists the CSP_BGA ball assignment by ball number.

Table 41. 160-Ball CSP_BGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{ABE0}$	H13	DATA4	N8	GND	L6	SCK	D1
$\overline{ABE1}$	H12	DATA5	P8	GND	L8	SCKE	B13
ADDR1	J14	DATA6	M7	GND	L10	$\overline{SMS}$	C13
ADDR2	K14	DATA7	N7	GND	M4	$\overline{SRAS}$	D13
ADDR3	L14	DATA8	P7	GND	M10	$\overline{SWE}$	D12
ADDR4	J13	DATA9	M6	GND	P14	TCK	P2
ADDR5	K13	DATA10	N6	MISO	E2	TDI	M3
ADDR6	L13	DATA11	P6	MOSI	D3	TDO	N3
ADDR7	K12	DATA12	M5	NMI	B10	TFS0	H3
ADDR8	L12	DATA13	N5	PF0	D2	TFS1	E1
ADDR9	M12	DATA14	P5	PF1	C1	TMR0	L2
ADDR10	M13	DATA15	P4	PF2	C2	TMR1	M1
ADDR11	M14	DR0PRI	K1	PF3	C3	TMR2	K2
ADDR12	N14	DR0SEC	J2	PF4	B1	TMS	N2
ADDR13	N13	DR1PRI	G3	PF5	B2	$\overline{TRST}$	N1
ADDR14	N12	DR1SEC	F3	PF6	B3	TSCLK0	J1
ADDR15	M11	DT0PRI	H1	PF7	B4	TSCLK1	F1
ADDR16	N11	DT0SEC	H2	PF8	A2	TX	K3
ADDR17	P13	DT1PRI	F2	PF9	A3	V_{DDEXT}	A1
ADDR18	P12	DT1SEC	E3	PF10	A4	V_{DDEXT}	C7
ADDR19	P11	$\overline{EMU}$	M2	PF11	A5	V_{DDEXT}	C12
$\overline{AMS0}$	E14	GND	A10	PF12	B5	V_{DDEXT}	D5
$\overline{AMS1}$	F14	GND	A14	PF13	B6	V_{DDEXT}	D9
$\overline{AMS2}$	F13	GND	B11	PF14	A6	V_{DDEXT}	F12
$\overline{AMS3}$	G12	GND	C4	PF15	C6	V_{DDEXT}	G4
$\overline{AOE}$	G13	GND	C5	PPI_CLK	C9	V_{DDEXT}	J4
ARDY	E13	GND	C11	PPI0	C8	V_{DDEXT}	J12
$\overline{ARE}$	G14	GND	D4	PPI1	B8	V_{DDEXT}	L7
$\overline{AWE}$	H14	GND	D7	PPI2	A7	V_{DDEXT}	L11
$\overline{BG}$	P10	GND	D8	PPI3	B7	V_{DDEXT}	P1
$\overline{BGH}$	N10	GND	D10	$\overline{RESET}$	C10	V_{DDINT}	D6
BMODE0	N4	GND	D11	RFS0	J3	V_{DDINT}	E4
BMODE1	P3	GND	F4	RFS1	G2	V_{DDINT}	E11
$\overline{BR}$	D14	GND	F11	RSCLK0	L1	V_{DDINT}	J11
CLKIN	A12	GND	G11	RSCLK1	G1	V_{DDINT}	L4
CLKOUT	B14	GND	H4	RTXI	A9	V_{DDINT}	L9
DATA0	M9	GND	H11	RTXO	A8	V_{DDRTC}	B9
DATA1	N9	GND	K4	RX	L3	VROUT0	A13
DATA2	P9	GND	K11	SA10	E12	VROUT1	B12
DATA3	M8	GND	L5	$\overline{SCAS}$	C14	XTAL	A11

Table 42. 160-Ball CSP_BGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	V_{DDEXT}	C13	$\overline{SMS}$	H1	DT0PRI	M3	TDI
A2	PF8	C14	$\overline{SCAS}$	H2	DT0SEC	M4	GND
A3	PF9	D1	SCK	H3	TFS0	M5	DATA12
A4	PF10	D2	PF0	H4	GND	M6	DATA9
A5	PF11	D3	MOSI	H11	GND	M7	DATA6
A6	PF14	D4	GND	H12	$\overline{ABE1}$	M8	DATA3
A7	PPI2	D5	V_{DDEXT}	H13	$\overline{ABE0}$	M9	DATA0
A8	RTXO	D6	V_{DDINT}	H14	$\overline{AWE}$	M10	GND
A9	RTXI	D7	GND	J1	TSCLK0	M11	ADDR15
A10	GND	D8	GND	J2	DR0SEC	M12	ADDR9
A11	XTAL	D9	V_{DDEXT}	J3	RFS0	M13	ADDR10
A12	CLKIN	D10	GND	J4	V_{DDEXT}	M14	ADDR11
A13	VROUT0	D11	GND	J11	V_{DDINT}	N1	$\overline{TRST}$
A14	GND	D12	$\overline{SWE}$	J12	V_{DDEXT}	N2	TMS
B1	PF4	D13	$\overline{SRAS}$	J13	ADDR4	N3	TDO
B2	PF5	D14	$\overline{BR}$	J14	ADDR1	N4	BMODE0
B3	PF6	E1	TFS1	K1	DR0PRI	N5	DATA13
B4	PF7	E2	MISO	K2	TMR2	N6	DATA10
B5	PF12	E3	DT1SEC	K3	TX	N7	DATA7
B6	PF13	E4	V_{DDINT}	K4	GND	N8	DATA4
B7	PPI3	E11	V_{DDINT}	K11	GND	N9	DATA1
B8	PPI1	E12	SA10	K12	ADDR7	N10	$\overline{BGH}$
B9	V_{DDRTC}	E13	ARDY	K13	ADDR5	N11	ADDR16
B10	NMI	E14	$\overline{AMS0}$	K14	ADDR2	N12	ADDR14
B11	GND	F1	TSCLK1	L1	RSCLK0	N13	ADDR13
B12	VROUT1	F2	DT1PRI	L2	TMR0	N14	ADDR12
B13	SCKE	F3	DR1SEC	L3	RX	P1	V_{DDEXT}
B14	CLKOUT	F4	GND	L4	V_{DDINT}	P2	TCK
C1	PF1	F11	GND	L5	GND	P3	BMODE1
C2	PF2	F12	V_{DDEXT}	L6	GND	P4	DATA15
C3	PF3	F13	$\overline{AMS2}$	L7	V_{DDEXT}	P5	DATA14
C4	GND	F14	$\overline{AMS1}$	L8	GND	P6	DATA11
C5	GND	G1	RSCLK1	L9	V_{DDINT}	P7	DATA8
C6	PF15	G2	RFS1	L10	GND	P8	DATA5
C7	V_{DDEXT}	G3	DR1PRI	L11	V_{DDEXT}	P9	DATA2
C8	PPI0	G4	V_{DDEXT}	L12	ADDR8	P10	$\overline{BG}$
C9	PPI_CLK	G11	GND	L13	ADDR6	P11	ADDR19
C10	$\overline{RESET}$	G12	$\overline{AMS3}$	L14	ADDR3	P12	ADDR18
C11	GND	G13	$\overline{AOE}$	M1	TMR1	P13	ADDR17
C12	V_{DDEXT}	G14	$\overline{ARE}$	M2	$\overline{EMU}$	P14	GND

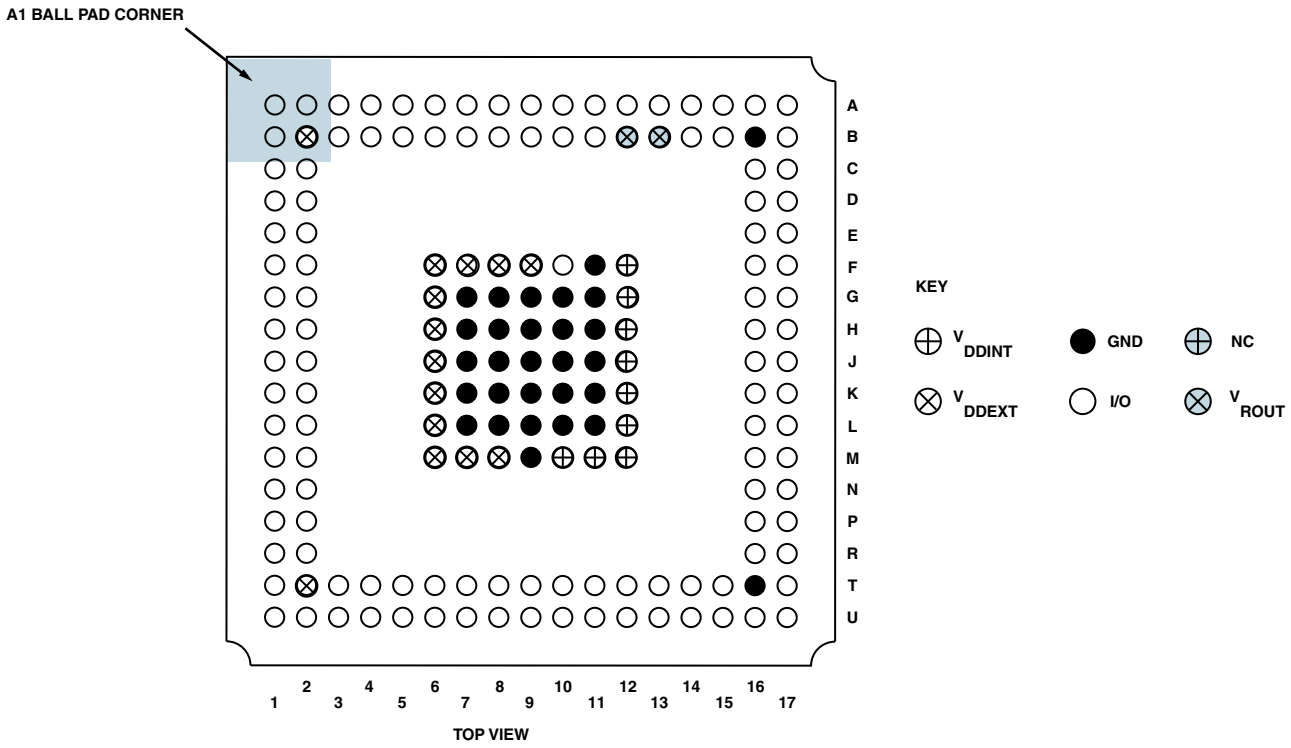


Figure 62. 169-Ball PBGA Ground Configuration (Top View)

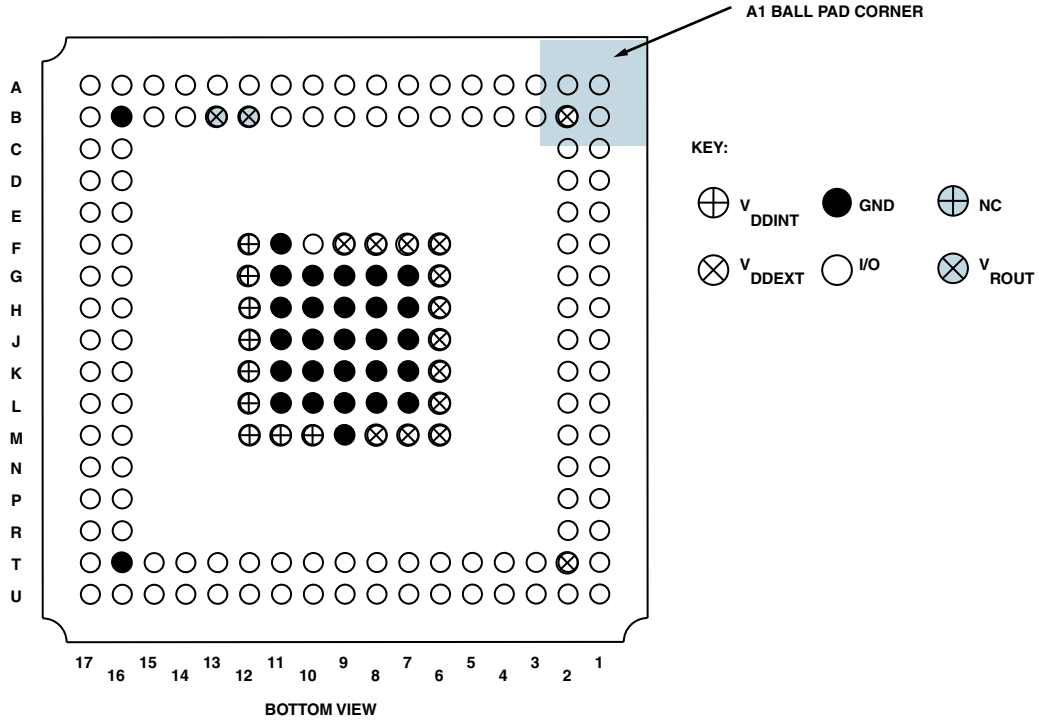


Figure 63. 169-Ball PBGA Ground Configuration (Bottom View)

176-LEAD LQFP PINOUT

Table 45 lists the LQFP pinout by signal. Table 46 on Page 57 lists the LQFP pinout by lead number.

Table 45. 176-Lead LQFP Pin Assignment (Alphabetical by Signal)

Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.
$\overline{ABE0}$	151	DATA3	113	GND	88	PPI_CLK	21	V_{DDEXT}	71
$\overline{ABE1}$	150	DATA4	112	GND	89	PPI0	22	V_{DDEXT}	93
ADDR1	149	DATA5	110	GND	90	PPI1	23	V_{DDEXT}	107
ADDR2	148	DATA6	109	GND	91	PPI2	24	V_{DDEXT}	118
ADDR3	147	DATA7	108	GND	92	PPI3	26	V_{DDEXT}	134
ADDR4	146	DATA8	105	GND	97	$\overline{RESET}$	13	V_{DDEXT}	145
ADDR5	142	DATA9	104	GND	106	RFS0	75	V_{DDEXT}	156
ADDR6	141	DATA10	103	GND	117	RFS1	64	V_{DDEXT}	171
ADDR7	140	DATA11	102	GND	128	RSCLK0	76	V_{DDINT}	25
ADDR8	139	DATA12	101	GND	129	RSCLK1	65	V_{DDINT}	52
ADDR9	138	DATA13	100	GND	130	RTXI	17	V_{DDINT}	66
ADDR10	137	DATA14	99	GND	131	RTXO	16	V_{DDINT}	80
ADDR11	136	DATA15	98	GND	132	RX	82	V_{DDINT}	111
ADDR12	135	DR0PRI	74	GND	133	SA10	164	V_{DDINT}	143
ADDR13	127	DR0SEC	73	GND	144	$\overline{SCAS}$	166	V_{DDINT}	157
ADDR14	126	DR1PRI	63	GND	155	SCK	53	V_{DDINT}	168
ADDR15	125	DR1SEC	62	GND	170	SCKE	173	V_{DDRTC}	18
ADDR16	124	DT0PRI	68	GND	174	$\overline{SMS}$	172	VROUT0	5
ADDR17	123	DT0SEC	67	GND	175	$\overline{SRAS}$	167	VROUT1	4
ADDR18	122	DT1PRI	59	GND	176	$\overline{SWE}$	165	XTAL	11
ADDR19	121	DT1SEC	58	MISO	54	TCK	94		
$\overline{AMS0}$	161	$\overline{EMU}$	83	MOSI	55	TDI	86		
$\overline{AMS1}$	160	GND	1	NMI	14	TDO	87		
$\overline{AMS2}$	159	GND	2	PF0	51	TFS0	69		
$\overline{AMS3}$	158	GND	3	PF1	50	TFS1	60		
$\overline{AOE}$	154	GND	7	PF2	49	TMR0	79		
ARDY	162	GND	8	PF3	48	TMR1	78		
$\overline{ARE}$	153	GND	9	PF4	47	TMR2	77		
$\overline{AWE}$	152	GND	15	PF5	46	TMS	85		
$\overline{BG}$	119	GND	19	PF6	38	$\overline{TRST}$	84		
$\overline{BGH}$	120	GND	30	PF7	37	TSCLK0	72		
BMODE0	96	GND	39	PF8	36	TSCLK1	61		
BMODE1	95	GND	40	PF9	35	TX	81		
$\overline{BR}$	163	GND	41	PF10	34	V_{DDEXT}	6		
CLKIN	10	GND	42	PF11	33	V_{DDEXT}	12		
CLKOUT	169	GND	43	PF12	32	V_{DDEXT}	20		
DATA0	116	GND	44	PF13	29	V_{DDEXT}	31		
DATA1	115	GND	56	PF14	28	V_{DDEXT}	45		
DATA2	114	GND	70	PF15	27	V_{DDEXT}	57		

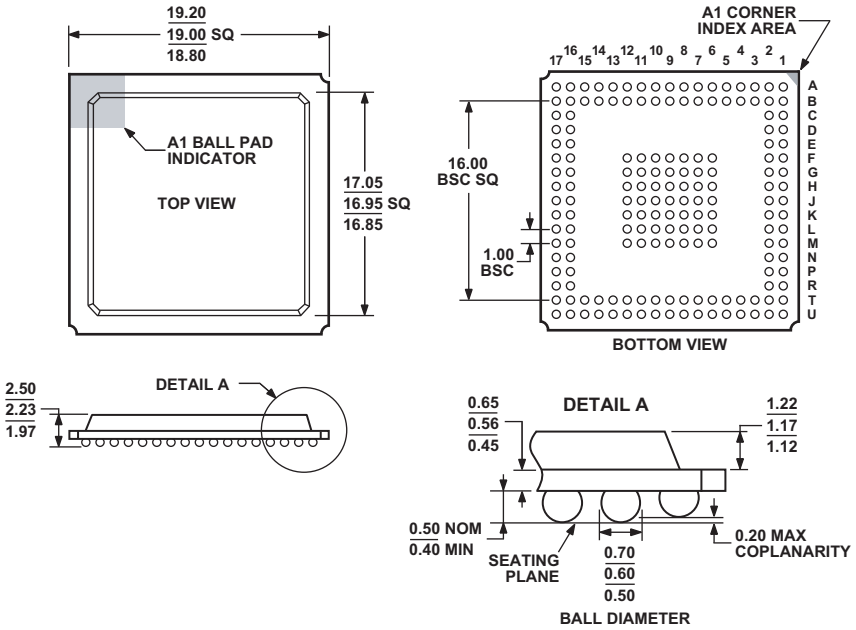


Figure 66. 169-Ball Plastic Ball Grid Array [PBGA]
(B-169)
Dimensions shown in millimeters