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Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

Details

Product Status	Active
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	400MHz
Non-Volatile Memory	ROM (1kB)
On-Chip RAM	52kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf531sbstz400

ADSP-BF531/ADSP-BF532/ADSP-BF533

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REVISION HISTORY

8/13— Rev. H to Rev. I

Updated Development Tools	15
Corrected Conditions value of the V_{IL} specification in Operating Conditions	20
Added notes to Table 30 in Serial Ports—Enable and Three-State	36
Added Timer Clock Timing	41
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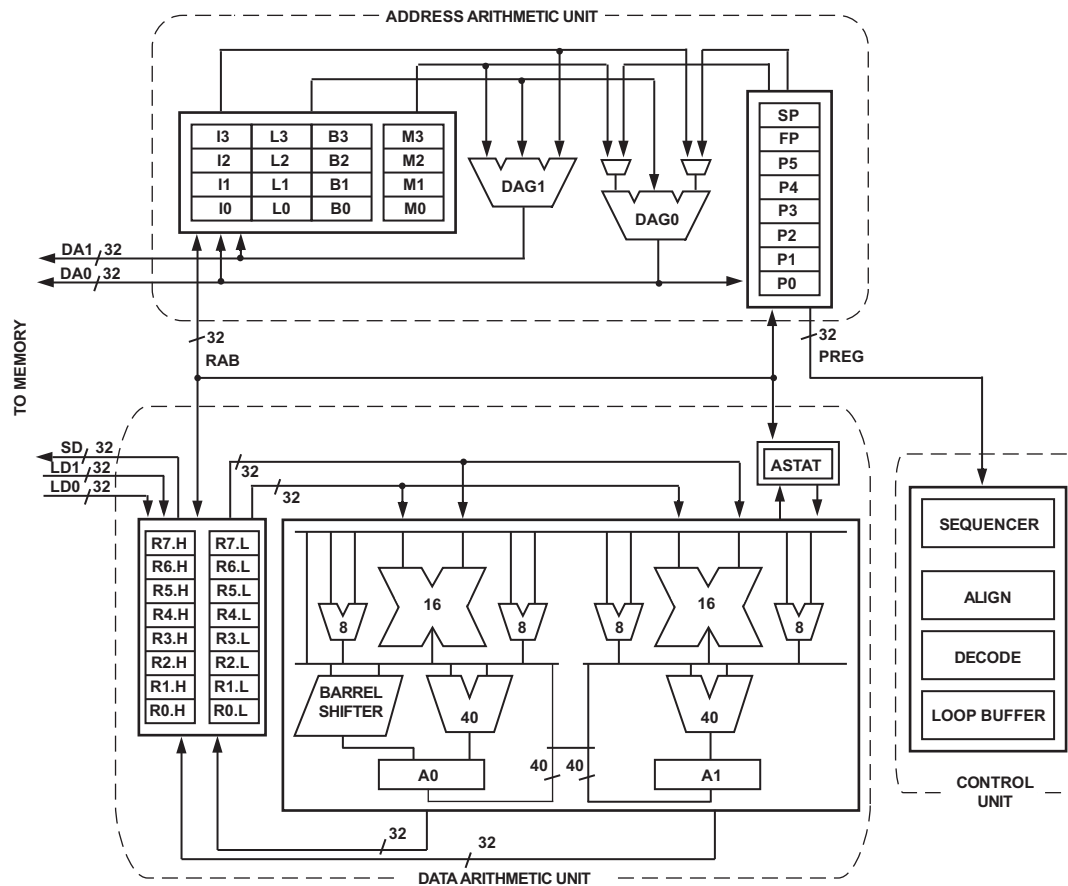


Figure 2. Blackfin Processor Core

The second on-chip memory block is the L1 data memory, consisting of one or two banks of up to 32K bytes. The memory banks are configurable, offering both cache and SRAM functionality. This memory block is accessed at full processor speed.

The third memory block is a 4K byte scratchpad SRAM, which runs at the same speed as the L1 memories, but is only accessible as data SRAM and cannot be configured as cache memory.

External (Off-Chip) Memory

External memory is accessed via the external bus interface unit (EBIU). This 16-bit interface provides a glueless connection to a bank of synchronous DRAM (SDRAM) as well as up to four banks of asynchronous memory devices including flash, EPROM, ROM, SRAM, and memory mapped I/O devices.

The PC133-compliant SDRAM controller can be programmed to interface to up to 128M bytes of SDRAM. The SDRAM controller allows one row to be open for each internal SDRAM bank, for up to four internal SDRAM banks, improving overall system performance.

The asynchronous memory controller can be programmed to control up to four banks of devices with very flexible timing parameters for a wide variety of devices. Each bank occupies a

1M byte segment regardless of the size of the devices used, so that these banks are only contiguous if each is fully populated with 1M byte of memory.

I/O Memory Space

Blackfin processors do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one containing the control MMRs for all core functions, and the other containing the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors contain a small boot kernel, which configures the appropriate peripheral for booting. If the processors are configured to boot from boot ROM memory space, the processor starts executing from the on-chip boot ROM. For more information, see [Boot-ing Modes on Page 14](#).

Each event type has an associated register to hold the return address and an associated return-from-event instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors' event controller consists of two stages, the core event controller (CEC) and the system interrupt controller (SIC). The core event controller works with the system interrupt controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC, and are then routed directly into the general-purpose interrupts of the CEC.

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the processor. Table 2 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

Table 2. Core Event Controller (CEC)

Priority (0 is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	Reset	RST
2	Nonmaskable Interrupt	NMI
3	Exception	EVX
4	Reserved	
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General Interrupt 7	IVG7
8	General Interrupt 8	IVG8
9	General Interrupt 9	IVG9
10	General Interrupt 10	IVG10
11	General Interrupt 11	IVG11
12	General Interrupt 12	IVG12
13	General Interrupt 13	IVG13
14	General Interrupt 14	IVG14
15	General Interrupt 15	IVG15

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processors provide a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). Table 3 describes the inputs into the SIC and the default mappings into the CEC.

Table 3. System Interrupt Controller (SIC)

Peripheral Interrupt Event	Default Mapping
PLL Wakeup	IVG7
DMA Error	IVG7
PPI Error	IVG7
SPORT 0 Error	IVG7
SPORT 1 Error	IVG7
SPI Error	IVG7
UART Error	IVG7
Real-Time Clock	IVG8
DMA Channel 0 (PPI)	IVG8
DMA Channel 1 (SPORT 0 Receive)	IVG9
DMA Channel 2 (SPORT 0 Transmit)	IVG9
DMA Channel 3 (SPORT 1 Receive)	IVG9
DMA Channel 4 (SPORT 1 Transmit)	IVG9
DMA Channel 5 (SPI)	IVG10
DMA Channel 6 (UART Receive)	IVG10
DMA Channel 7 (UART Transmit)	IVG10
Timer 0	IVG11
Timer 1	IVG11
Timer 2	IVG11
Port F GPIO Interrupt A	IVG12
Port F GPIO Interrupt B	IVG12
Memory DMA Stream 0	IVG13
Memory DMA Stream 1	IVG13
Software Watchdog Timer	IVG13

Event Control

The processors provide a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 32 bits wide:

- CEC interrupt latch register (ILAT) – The ILAT register indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it can also be written to clear (cancel) latched events. This register can be read while in supervisor mode and can only be written while in supervisor mode when the corresponding IMASK bit is cleared.
- CEC interrupt mask register (IMASK) – The IMASK register controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and is processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be latched in the ILAT register. This register can be read or written while in supervisor mode. Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.

The stopwatch function counts down from a programmed value, with one second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like other peripherals, the RTC can wake up the processor from sleep mode upon generation of any RTC wakeup event. Additionally, an RTC wakeup event can wake up the processor from deep sleep mode, and wake up the on-chip internal voltage regulator from a powered-down state.

Connect RTC pins RTXI and RTXO with external components as shown in Figure 6.

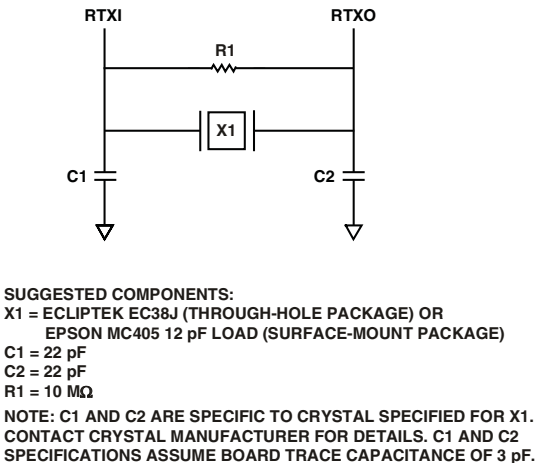


Figure 6. External Components for RTC

WATCHDOG TIMER

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors include a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK), at a maximum frequency of f_{SCLK} .

TIMERS

There are four general-purpose programmable timer units in the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors. Three timers have an external pin that can be configured either as a pulse-width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the PF1 pin (TACLK), an external clock input to the PPI_CLK pin (TMRCLK), or to the internal SCLK.

The timer units can be used in conjunction with the UART to measure the width of the pulses in the data stream to provide an autobaud detect function for a serial channel.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the three general-purpose programmable timers, a fourth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

SERIAL PORTS (SPORTs)

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- I²S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I²S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from $(f_{SCLK}/131,070)$ Hz to $(f_{SCLK}/2)$ Hz.
- Word length – Each SPORT supports serial data words from 3 bits to 32 bits in length, transferred most-significant-bit first or least-significant-bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ -law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.

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- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data-word or after transferring an entire data buffer or buffers through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1,024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

An additional 250 mV of SPORT input hysteresis can be enabled by setting Bit 15 of the PLL_CTL register. When this bit is set, all SPORT input pins have the increased hysteresis.

SERIAL PERIPHERAL INTERFACE (SPI) PORT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have an SPI-compatible port that enables the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins (master output-slave input, MOSI, and master input-slave output, MISO) and a clock pin (serial clock, SCK). An SPI chip select input pin ($\overline{\text{SPISS}}$) lets other SPI devices select the processor, and seven SPI chip select output pins ($\overline{\text{SPISEL7-1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface which supports both master/slave modes and multimaster environments.

The baud rate and clock phase/polarities for the SPI port are programmable, and it has an integrated DMA controller, configurable to support transmit or receive data streams. The SPI DMA controller can only service unidirectional accesses at any given time.

The SPI port clock rate is calculated as:

$$\text{SPI Clock Rate} = \frac{f_{\text{SCLK}}}{2 \times \text{SPI_BAUD}}$$

where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provide a full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART port includes support for 5 data bits to 8 data bits, 1 stop bit or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.

- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The baud rate, serial data format, error code generation and status, and interrupts for the UART port are programmable.

The UART programmable features include:

- Supporting bit rates ranging from ($f_{\text{SCLK}}/1,048,576$) bits per second to ($f_{\text{SCLK}}/16$) bits per second.
- Supporting data formats from seven bits to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as:

$$\text{UART Clock Rate} = \frac{f_{\text{SCLK}}}{16 \times \text{UART_Divisor}}$$

where the 16-bit UART_Divisor comes from the UART_DLH register (most significant 8 bits) and UART_DLL register (least significant 8 bits).

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The capabilities of the UART are further extended with support for the Infrared Data Association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

GENERAL-PURPOSE I/O PORT F

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have 16 bidirectional, general-purpose I/O pins on Port F (PF15–0). Each general-purpose I/O pin can be individually controlled by manipulation of the GPIO control, status and interrupt registers:

- GPIO direction control register – Specifies the direction of each individual PFx pin as input or output.
- GPIO control and status registers – The processor employs a “write one to modify” mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins. Four control registers are provided. One register is written in order to set GPIO pin values, one register is written in order to clear GPIO pin values, one register is written in order to toggle GPIO pin values, and one register is written in order to specify GPIO pin values. Reading the GPIO status register allows software to interrogate the sense of the GPIO pin.
- GPIO interrupt mask registers – The two GPIO interrupt mask registers allow each individual PFx pin to function as an interrupt to the processor. Similar to the two GPIO control registers that are used to set and clear individual GPIO pin values, one GPIO interrupt mask register sets bits to enable interrupt function, and the other GPIO interrupt mask register clears bits to disable interrupt function.

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ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	400 MHz ¹			500 MHz/533 MHz/600 MHz ²			Unit
			Min	Typical	Max	Min	Typical	Max	
V _{OH}	High Level Output Voltage ³	V _{DDEXT} = 1.75 V, I _{OH} = -0.5 mA V _{DDEXT} = 2.25 V, I _{OH} = -0.5 mA V _{DDEXT} = 3.0 V, I _{OH} = -0.5 mA	1.5 1.9 2.4			1.5 1.9 2.4			V V V
V _{OL}	Low Level Output Voltage ³	V _{DDEXT} = 1.75 V, I _{OL} = 2.0 mA V _{DDEXT} = 2.25 V/3.0 V, I _{OL} = 2.0 mA			0.2 0.4			0.2 0.4	V V
I _{IH}	High Level Input Current ⁴	V _{DDEXT} = Max, V _{IN} = V _{DD} Max			10.0			10.0	μA
I _{IHP}	High Level Input Current JTAG ⁵	V _{DDEXT} = Max, V _{IN} = V _{DD} Max			50.0			50.0	μA
I _{IL} ⁶	Low Level Input Current ⁴	V _{DDEXT} = Max, V _{IN} = 0 V			10.0			10.0	μA
I _{OZH}	Three-State Leakage Current ⁷	V _{DDEXT} = Max, V _{IN} = V _{DD} Max			10.0			10.0	μA
I _{OZL} ⁶	Three-State Leakage Current ⁷	V _{DDEXT} = Max, V _{IN} = 0 V			10.0			10.0	μA
C _{IN}	Input Capacitance ⁸	f _{IN} = 1 MHz, T _{AMBIENT} = 25°C, V _{IN} = 2.5 V		4	8 ⁹		4	8 ⁹	pF
I _{DDDEEPSLEEP} ¹⁰	V _{DDINT} Current in Deep Sleep Mode	V _{DDINT} = 1.0 V, f _{CCLK} = 0 MHz, T _J = 25°C, ASF = 0.00		7.5			32.5		mA
I _{DDSLEEP}	V _{DDINT} Current in Sleep Mode	V _{DDINT} = 0.8 V, T _J = 25°C, SCLK = 25 MHz			10			37.5	mA
I _{DD-TYP} ¹¹	V _{DDINT} Current	V _{DDINT} = 1.14 V, f _{CCLK} = 400 MHz, T _J = 25°C		125			152		mA
I _{DD-TYP} ¹¹	V _{DDINT} Current	V _{DDINT} = 1.2 V, f _{CCLK} = 500 MHz, T _J = 25°C					190		mA
I _{DD-TYP} ¹¹	V _{DDINT} Current	V _{DDINT} = 1.2 V, f _{CCLK} = 533 MHz, T _J = 25°C					200		mA
I _{DD-TYP} ¹¹	V _{DDINT} Current	V _{DDINT} = 1.3 V, f _{CCLK} = 600 MHz, T _J = 25°C					245		mA
I _{DDHIBERNATE} ¹⁰	V _{DDEXT} Current in Hibernate State	V _{DDEXT} = 3.6 V, CLKIN = 0 MHz, T _J = Max, voltage regulator off (V _{DDINT} = 0 V)		50	100		50	100	μA
I _{DDRTC}	V _{DDRTC} Current	V _{DDRTC} = 3.3 V, T _J = 25°C		20			20		μA
I _{DDDEEPSLEEP} ¹⁰	V _{DDINT} Current in Deep Sleep Mode	f _{CCLK} = 0 MHz		6	Table 15		16	Table 14	mA
I _{DD-INT}	V _{DDINT} Current	f _{CCLK} > 0 MHz			I _{DDDEEPSLEEP} + (Table 17 × ASF)			I _{DDDEEPSLEEP} + (Table 17 × ASF)	mA

¹ Applies to all 400 MHz speed grade models. See [Ordering Guide on Page 63](#).

² Applies to all 500 MHz, 533 MHz, and 600 MHz speed grade models. See [Ordering Guide on Page 63](#).

³ Applies to output and bidirectional pins.

⁴ Applies to input pins except JTAG inputs.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 18 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Table 18. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.45 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.5 V to +3.8 V
Input Voltage ^{1, 2}	–0.5 V to +3.8 V
Output Voltage Swing	–0.5 V to $V_{DDEXT} + 0.5$ V
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	125°C

¹ Applies to 100% transient duty cycle. For other duty cycles see Table 19.

² Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is $V_{DDEXT} \pm 0.2$ V.

Table 19. Maximum Duty Cycle for Input Transient Voltage¹

V_{IN} Min (V) ²	V_{IN} Max (V) ²	Maximum Duty Cycle ³
–0.50	+3.80	100%
–0.70	+4.00	40%
–0.80	+4.10	25%
–0.90	+4.20	15%
–1.00	+4.30	10%

¹ Applies to all signal pins with the exception of CLKIN, XTAL, VROUT1–0.

² The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.

³ Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

ESD SENSITIVITY



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

Clock and Reset Timing

Table 21 and Figure 11 describe clock and reset operations. Per Absolute Maximum Ratings on Page 25, combinations of CLKIN and clock multipliers/divisors must not result in core/

system clocks exceeding the maximum limits allowed for the processor, including system clock restrictions related to supply voltage.

Table 21. Clock and Reset Timing

Parameter	Min	Max	Unit
Timing Requirements			
t_{CKIN} CLKIN Period ^{1, 2, 3, 4}	25.0	100.0	ns
t_{CKINL} CLKIN Low Pulse	10.0		ns
t_{CKINH} CLKIN High Pulse	10.0		ns
t_{WRST} $\overline{RESET}$ Asserted Pulse Width Low ⁵	$11 \times t_{CKIN}$		ns
t_{NOBOOT} $\overline{RESET}$ Deassertion to First External Access Delay ⁶	$3 \times t_{CKIN}$	$5 \times t_{CKIN}$	ns

¹ Applies to PLL bypass mode and PLL non bypass mode.

² CLKIN frequency must not change on the fly.

³ Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO} , f_{CLK} , and f_{SCLK} settings discussed in Table 11 on Page 21 through Table 13 on Page 21. Since the default behavior of the PLL is to multiply the CLKIN frequency by 10, the 400 MHz speed grade parts cannot use the full CLKIN period range.

⁴ If the DF bit in the PLL_CTL register is set, then the maximum t_{CKIN} period is 50 ns.

⁵ Applies after power-up sequence is complete. See Table 22 and Figure 12 for power-up reset timing.

⁶ Applies when processor is configured in No Boot Mode (BMODE1-0 = b#00).

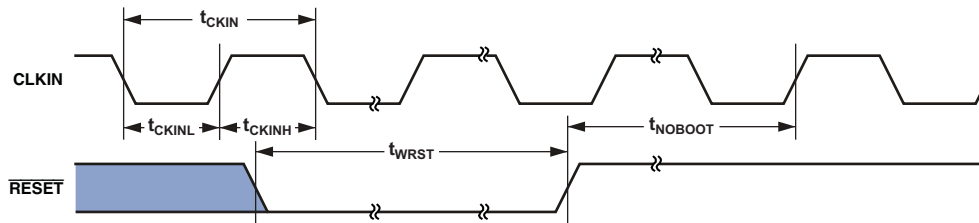
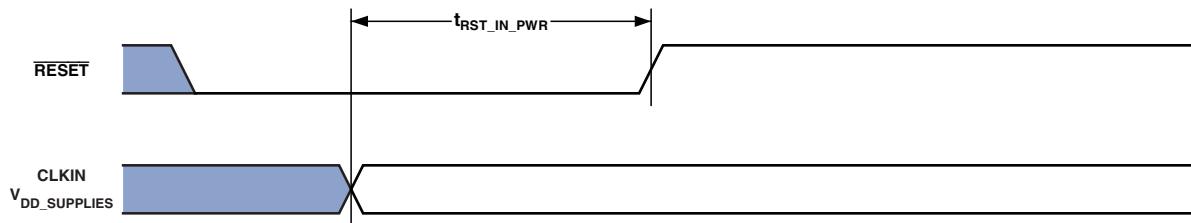


Figure 11. Clock and Reset Timing

Table 22. Power-Up Reset Timing

Parameter	Min	Max	Unit
Timing Requirement			
$t_{RST_IN_PWR}$ $\overline{RESET}$ Deasserted After the V_{DDINT} , V_{DDEXT} , V_{DDRTC} , and CLKIN Pins Are Stable and Within Specification	$3500 \times t_{CKIN}$		ns



In Figure 12, $V_{DD_SUPPLIES}$ is V_{DDINT} , V_{DDEXT} , V_{DDRTC}

Figure 12. Power-Up Reset Timing

Asynchronous Memory Write Cycle Timing

Table 24. Asynchronous Memory Write Cycle Timing

Parameter	$V_{DDEXT} = 1.8\text{ V}$		$V_{DDEXT} = 2.5\text{ V}/3.3\text{ V}$		Unit
	Min	Max	Min	Max	
Timing Requirements					
t_{SARDY}	ARDY Setup Before CLKOUT		4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT		1.0	0.0	ns
Switching Characteristics					
t_{DDAT}	DATA15–0 Disable After CLKOUT			6.0	ns
t_{ENDAT}	DATA15–0 Enable After CLKOUT		1.0	1.0	ns
t_{DO}	Output Delay After CLKOUT ¹			6.0	ns
t_{HO}	Output Hold After CLKOUT ¹		1.0	0.8	ns

¹ Output pins include $\overline{\text{AMS3}}\text{--}0$, $\overline{\text{ABE1}}\text{--}0$, $\text{ADDR19--}1$, $\text{DATA15--}0$, AOE , AWE .

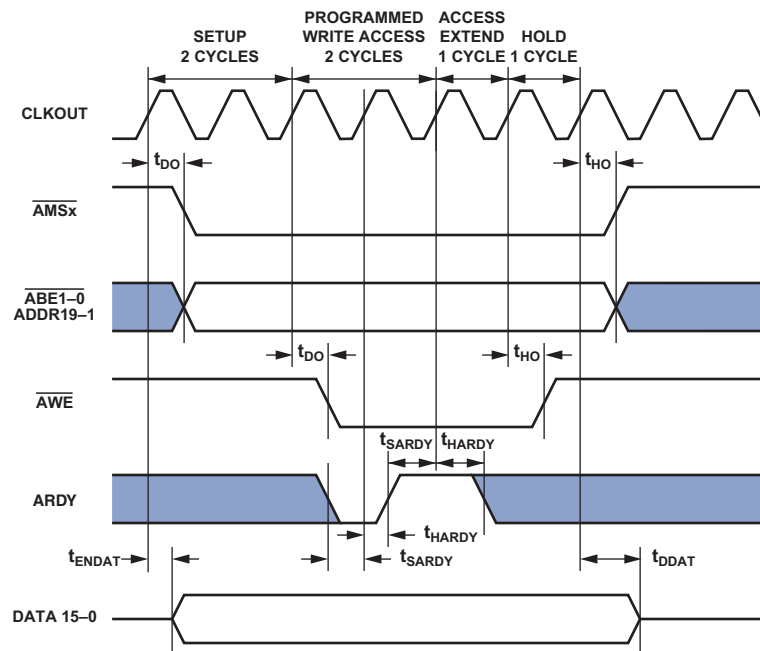


Figure 14. Asynchronous Memory Write Cycle Timing

ADSP-BF531/ADSP-BF532/ADSP-BF533

Serial Port Timing

Table 28 through Table 31 on Page 37 and Figure 23 on Page 35 through Figure 26 on Page 37 describe Serial Port operations.

Table 28. Serial Ports—External Clock

Parameter	V _{DDEXT} = 1.8 V		V _{DDEXT} = 2.5 V/3.3 V		Unit
	Min	Max	Min	Max	
Timing Requirements					
t _{SFSE} TFSx/RFSx Setup Before TSCLKx/RSCLKx ¹	3.0		3.0		ns
t _{HFSE} TFSx/RFSx Hold After TSCLKx/RSCLKx ¹	3.0		3.0		ns
t _{SDRE} Receive Data Setup Before RSCLKx ¹	3.0		3.0		ns
t _{HDRE} Receive Data Hold After RSCLKx ¹	3.0		3.0		ns
t _{SCLKEW} TSCLKx/RSCLKx Width	8.0		4.5		ns
t _{SCLKE} TSCLKx/RSCLKx Period	20.0		15.0 ²		ns
t _{SUDTE} Start-Up Delay From SPORT Enable To First External TFSx ³	4.0 × t _{SCLKE}		4.0 × t _{SCLKE}		ns
t _{SUDRE} Start-Up Delay From SPORT Enable To First External RFSx ³	4.0 × t _{SCLKE}		4.0 × t _{SCLKE}		ns
Switching Characteristics					
t _{DFSE} TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx) ⁴		10.0		10.0	ns
t _{HOFSE} TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx) ¹	0.0		0.0		ns
t _{DDTE} Transmit Data Delay After TSCLKx ¹		10.0		10.0	ns
t _{HDTE} Transmit Data Hold After TSCLKx ¹	0.0		0.0		ns

¹ Referenced to sample edge.

² For receive mode with external RSCLKx and external RFSx only, the maximum specification is 11.11 ns (90 MHz).

³ Verified in design but untested. After being enabled, the serial port requires external clock pulses—before the first external frame sync edge—to initialize the serial port.

⁴ Referenced to drive edge.

Table 29. Serial Ports—Internal Clock

Parameter	V _{DDEXT} = 1.8 V		V _{DDEXT} = 2.5 V/3.3 V		Unit
	Min	Max	Min	Max	
Timing Requirements					
t _{SFSI} TFSx/RFSx Setup Before TSCLKx/RSCLKx ¹	11.0		9.0		ns
t _{HFSI} TFSx/RFSx Hold After TSCLKx/RSCLKx ¹	−2.0		−2.0		ns
t _{SDRI} Receive Data Setup Before RSCLKx ¹	9.5		9.0		ns
t _{HDRI} Receive Data Hold After RSCLKx ¹	0.0		0.0		ns
Switching Characteristics					
t _{DFSI} TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx) ²		3.0		3.0	ns
t _{HOFSI} TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx) ¹	−1.0		−1.0		ns
t _{DDTI} Transmit Data Delay After TSCLKx ¹		3.0		3.0	ns
t _{HDTI} Transmit Data Hold After TSCLKx ¹	−2.5		−2.0		ns
t _{SCLKIW} TSCLKx/RSCLKx Width	6.0		4.5		ns

¹ Referenced to sample edge.

² Referenced to drive edge.

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Table 30. Serial Ports—Enable and Three-State

Parameter		V _{DDEXT} = 1.8 V		V _{DDEXT} = 2.5 V/3.3 V		Unit
		Min	Max	Min	Max	
Switching Characteristics						
t _{D_TENE}	Data Enable Delay from External TSCLKx ¹	0		0		ns
t _{D_DTTE}	Data Disable Delay from External TSCLKx ^{1, 2, 3}		10.0		10.0	ns
t _{D_TENI}	Data Enable Delay from Internal TSCLKx ¹	−2.0		−2.0		ns
t _{D_DTTI}	Data Disable Delay from Internal TSCLKx ^{1, 2, 3}		3.0		3.0	ns

¹ Referenced to drive edge.

² Applicable to multichannel mode only.

³ TSCLKx is tied to RSCLKx.

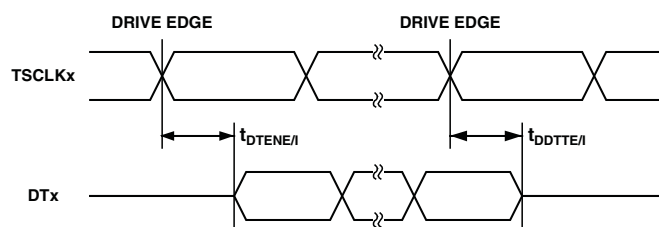


Figure 25. Enable and Three-State

ADSP-BF531/ADSP-BF532/ADSP-BF533

General-Purpose I/O Port F Pin Cycle Timing

Table 34. General-Purpose I/O Port F Pin Cycle Timing

Parameter	V _{DDEXT} = 1.8 V		V _{DDEXT} = 2.5 V/3.3 V		Unit
	Min	Max	Min	Max	
Timing Requirement					
t _{WFI} GPIO Input Pulse Width	t _{SCLK} + 1		t _{SCLK} + 1		ns
Switching Characteristic					
t _{GPOD} GPIO Output Delay from CLKOUT Low	6		6		ns

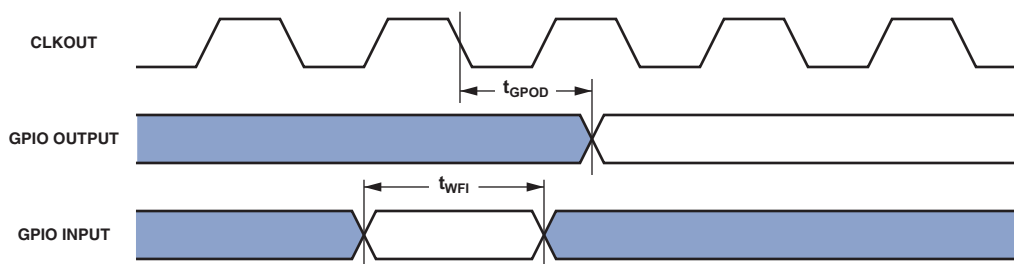


Figure 29. GPIO Cycle Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

For information on the UART port receive and transmit operations, see the *ADSP-BF533 Blackfin Processor Hardware Reference*.

OUTPUT DRIVE CURRENTS

Figure 33 through Figure 44 show typical current-voltage characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

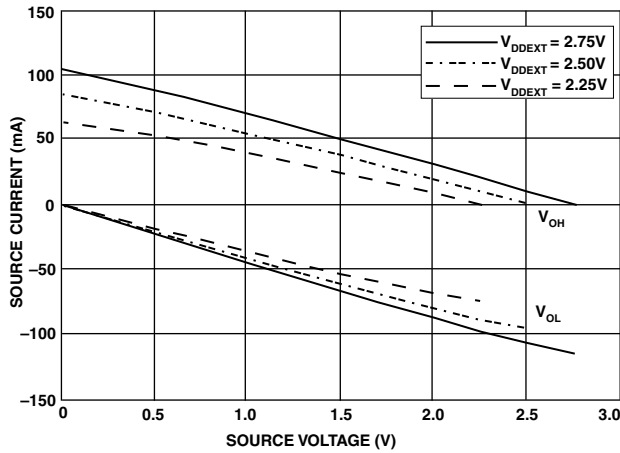


Figure 33. Drive Current A ($V_{DDEXT} = 2.5 \text{ V}$)

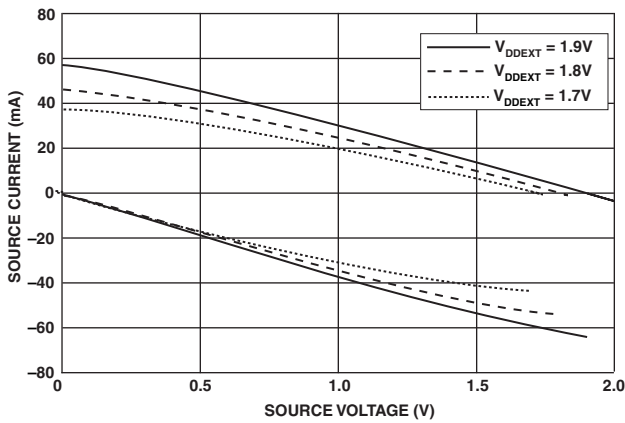


Figure 34. Drive Current A ($V_{DDEXT} = 1.8 \text{ V}$)

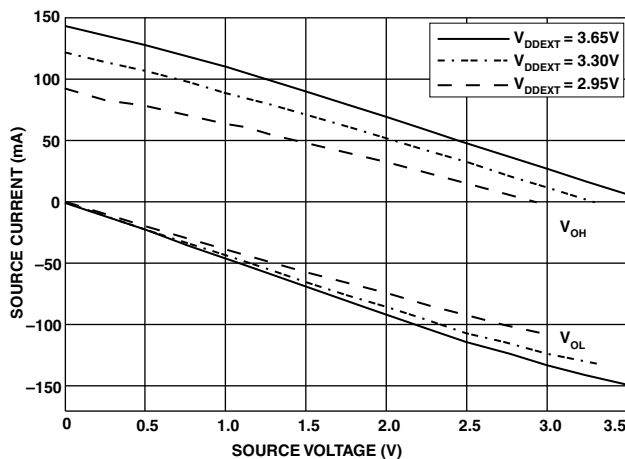


Figure 35. Drive Current A ($V_{DDEXT} = 3.3 \text{ V}$)

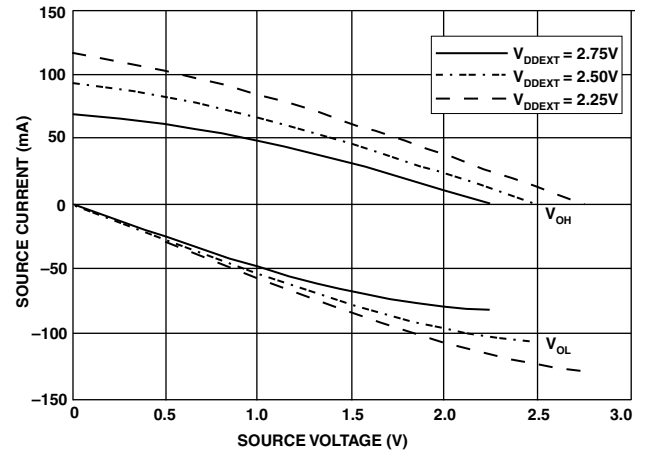


Figure 36. Drive Current B ($V_{DDEXT} = 2.5 \text{ V}$)

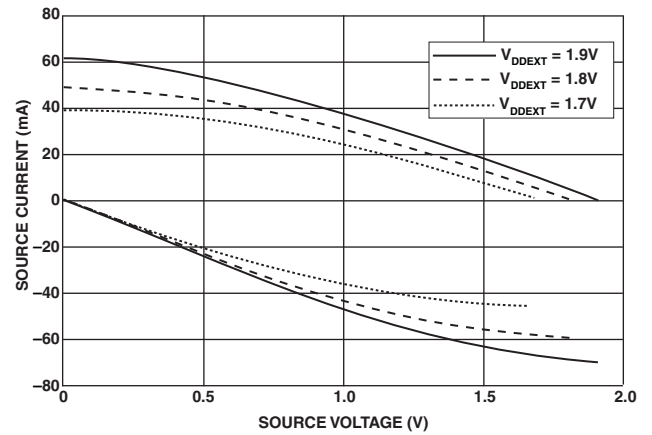


Figure 37. Drive Current B ($V_{DDEXT} = 1.8 \text{ V}$)

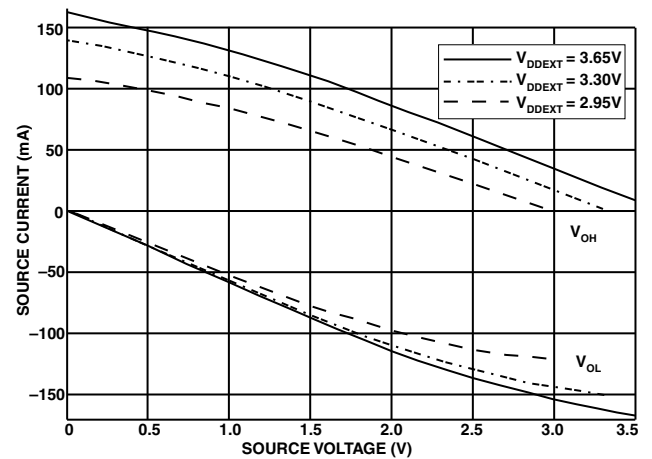


Figure 38. Drive Current B ($V_{DDEXT} = 3.3 \text{ V}$)

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 45 shows the measurement point for ac measurements (except output enable/disable). The measurement point V_{MEAS} is 0.95 V for V_{DDEXT} (nominal) = 1.8 V or 1.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V.



Figure 45. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 46.

The time $t_{ENA_MEASURED}$ is the interval, from when the reference signal switches, to when the output voltage reaches $V_{TRIP(HIGH)}$ or $V_{TRIP(LOW)}$.

For V_{DDEXT} (nominal) = 1.8 V— V_{TRIP} (high) is 1.3 V and V_{TRIP} (low) is 0.7 V.

For V_{DDEXT} (nominal) = 2.5 V/3.3 V— V_{TRIP} (high) is 2.0 V and V_{TRIP} (low) is 1.0 V.

Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the V_{TRIP} (high) or V_{TRIP} (low) trip voltage.

Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA_MEASURED} - t_{TRIP}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 45.

$$t_{DIS} = t_{DIS_MEASURED} - t_{DECAY}$$

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load C_L and the load current I_L . This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V) / I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L , and with ΔV equal to 0.1 V for V_{DDEXT} (nominal) = 1.8 V or 0.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V.

The time $t_{DIS_MEASURED}$ is the interval from when the reference signal switches, to when the output voltage decays ΔV from the measured output high or output low voltage.

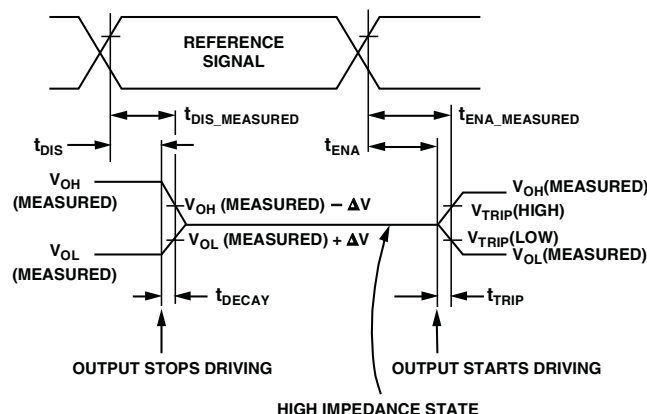


Figure 46. Output Enable/Disable

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the processor's output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time is t_{DECAY} plus the various output disable times as specified in the [Timing Specifications on Page 27](#) (for example t_{SDAT} for an SDRAM write cycle as shown in [SDRAM Interface Timing on Page 30](#)).

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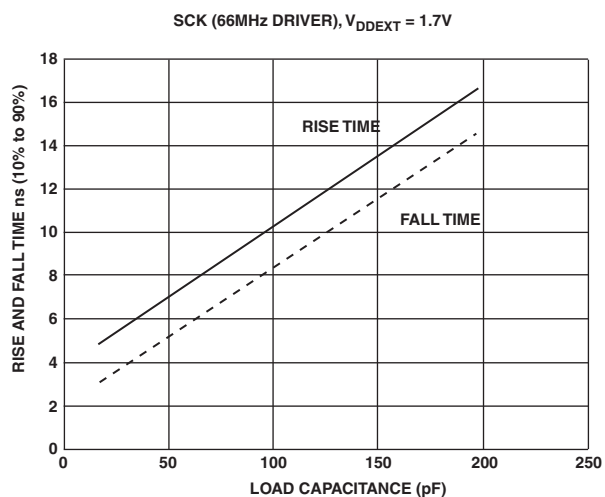


Figure 57. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at $V_{DDEXT} = 1.75V$

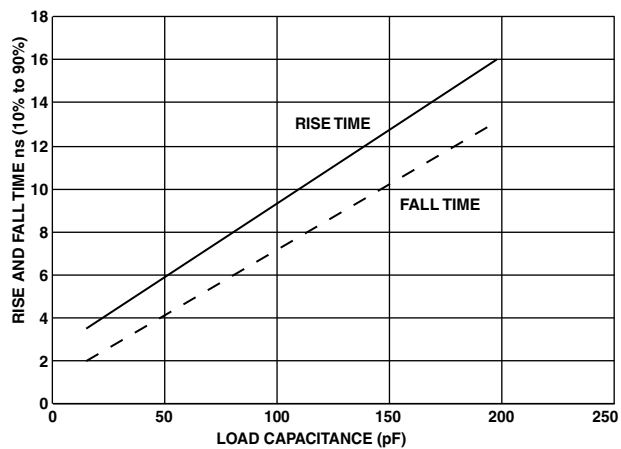


Figure 58. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at $V_{DDEXT} = 2.25V$

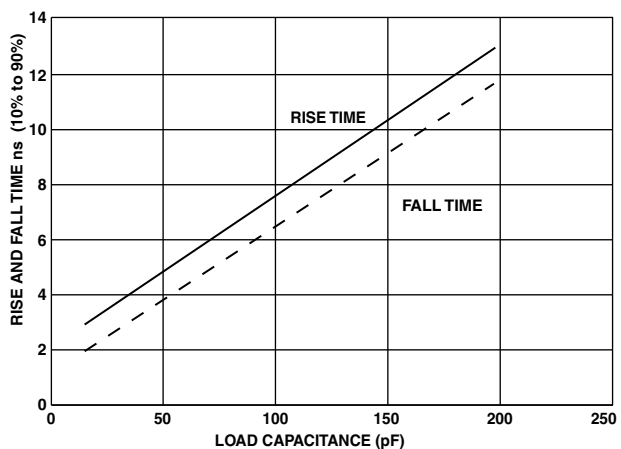


Figure 59. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at $V_{DDEXT} = 3.65V$

169-BALL PBGA BALL ASSIGNMENT

Table 43 lists the PBGA ball assignment by signal. Table 44 on Page 54 lists the PBGA ball assignment by ball number.

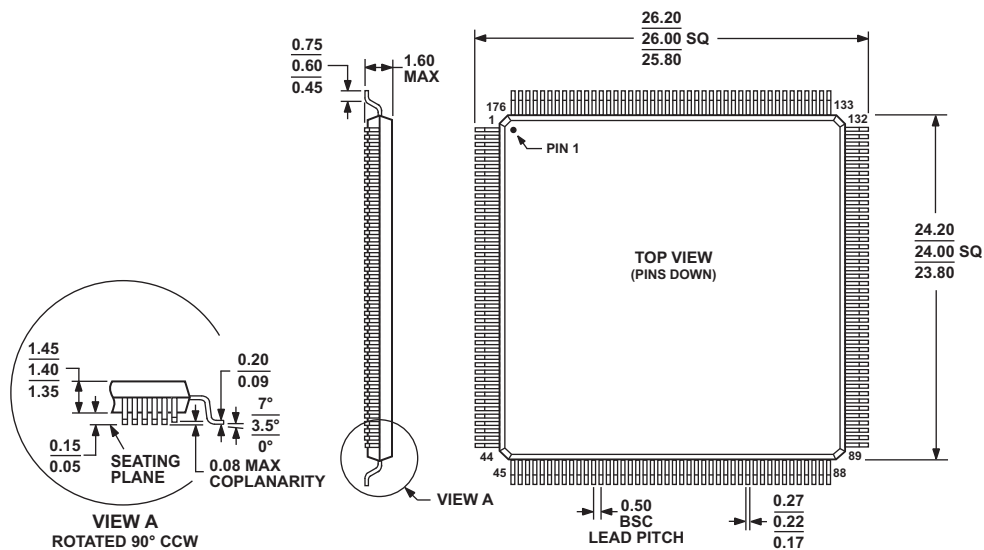
Table 43. 169-Ball PBGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
ABE0	H16	DATA4	U12	GND	K9	RTXI	A10	V _{DDEXT}	K6
ABE1	H17	DATA5	U11	GND	K10	RTXO	A11	V _{DDEXT}	L6
ADDR1	J16	DATA6	T10	GND	K11	RX	T1	V _{DDEXT}	M6
ADDR2	J17	DATA7	U10	GND	L7	SA10	B15	V _{DDEXT}	M7
ADDR3	K16	DATA8	T9	GND	L8	SCAS	A16	V _{DDEXT}	M8
ADDR4	K17	DATA9	U9	GND	L9	SCK	D1	V _{DDEXT}	T2
ADDR5	L16	DATA10	T8	GND	L10	SCKE	B14	VRROUT0	B12
ADDR6	L17	DATA11	U8	GND	L11	SMS	A17	VRROUT1	B13
ADDR7	M16	DATA12	U7	GND	M9	SRAS	A15	XTAL	A13
ADDR8	M17	DATA13	T7	GND	T16	SWE	B17		
ADDR9	N17	DATA14	U6	MISO	E2	TCK	U4		
ADDR10	N16	DATA15	T6	MOSI	E1	TDI	U3		
ADDR11	P17	DR0PRI	M2	NMI	B11	TDO	T4		
ADDR12	P16	DR0SEC	M1	PF0	D2	TFS0	L1		
ADDR13	R17	DR1PRI	H1	PF1	C1	TFS1	G2		
ADDR14	R16	DR1SEC	H2	PF2	B1	TMR0	R1		
ADDR15	T17	DT0PRI	K2	PF3	C2	TMR1	P2		
ADDR16	U15	DT0SEC	K1	PF4	A1	TMR2	P1		
ADDR17	T15	DT1PRI	F1	PF5	A2	TMS	T3		
ADDR18	U16	DT1SEC	F2	PF6	B3	TRST	U2		
ADDR19	T14	EMU	U1	PF7	A3	TSCLK0	L2		
AMS0	D17	GND	B16	PF8	B4	TSCLK1	G1		
AMS1	E16	GND	F11	PF9	A4	TX	R2		
AMS2	E17	GND	G7	PF10	B5	VDD	F12		
AMS3	F16	GND	G8	PF11	A5	VDD	G12		
AOE	F17	GND	G9	PF12	A6	VDD	H12		
ARDY	C16	GND	G10	PF13	B6	VDD	J12		
ARE	G16	GND	G11	PF14	A7	VDD	K12		
AWE	G17	GND	H7	PF15	B7	VDD	L12		
BG	T13	GND	H8	PPI_CLK	B10	VDD	M10		
BGH	U17	GND	H9	PPI0	B9	VDD	M11		
BMODE0	U5	GND	H10	PPI1	A9	VDD	M12		
BMODE1	T5	GND	H11	PPI2	B8	V _{DDEXT}	B2		
BR	C17	GND	J7	PPI3	A8	V _{DDEXT}	F6		
CLKIN	A14	GND	J8	RESET	A12	V _{DDEXT}	F7		
CLKOUT	D16	GND	J9	RFS0	N1	V _{DDEXT}	F8		
DATA0	U14	GND	J10	RFS1	J1	V _{DDEXT}	F9		
DATA1	T12	GND	J11	RSCLK0	N2	V _{DDEXT}	G6		
DATA2	U13	GND	K7	RSCLK1	J2	V _{DDEXT}	H6		
DATA3	T11	GND	K8	RTCVDD	F10	V _{DDEXT}	J6		

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OUTLINE DIMENSIONS

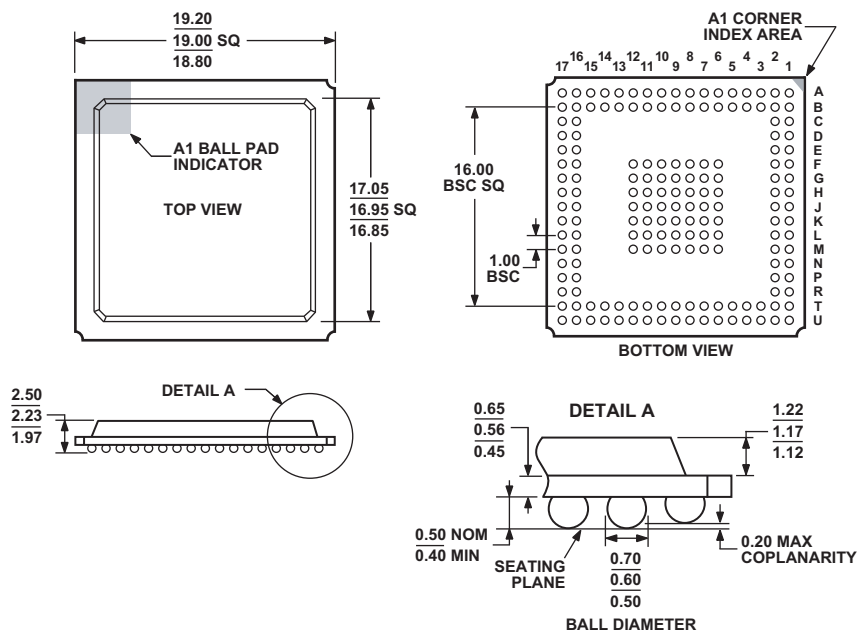
Dimensions in the outline dimension figures are shown in millimeters.



COMPLIANT TO JEDEC STANDARDS MS-026-BGA

Figure 64. 176-Lead Low Profile Quad Flat Package [LQFP]
(ST-176-1)
Dimensions shown in millimeters

ADSP-BF531/ADSP-BF532/ADSP-BF533



COMPLIANT TO JEDEC STANDARDS MS-034-AAG-2

Figure 66. 169-Ball Plastic Ball Grid Array [PBGA]
(B-169)

Dimensions shown in millimeters

ADSP-BF531/ADSP-BF532/ADSP-BF533

ORDERING GUIDE

Model ¹	Temperature Range ²	Speed Grade (Max)	Package Description	Package Option
ADSP-BF531SBB400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF531SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF531SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF531SBBZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF531SBBZ4RL	–40°C to +85°C	400 MHz	160-Ball CSP_BGA, 13" Tape and Reel	BC-160-2
ADSP-BF531SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF532SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF532SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF532SBBZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF532SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF533SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF533SBB500	–40°C to +85°C	500 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBZ500	–40°C to +85°C	500 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBC500	–40°C to +85°C	500 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBZ500	–40°C to +85°C	500 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBC-5V	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBZ-5V	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKBC-6V	0°C to +70°C	600 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKBCZ-6V	0°C to +70°C	600 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKSTZ-5V	0°C to +70°C	533 MHz	176-Lead LQFP	ST-176-1

¹ Z = RoHS compliant part.

² Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see [Operating Conditions on Page 20](#) for junction temperature (T_J) specification which is the only temperature specification.

