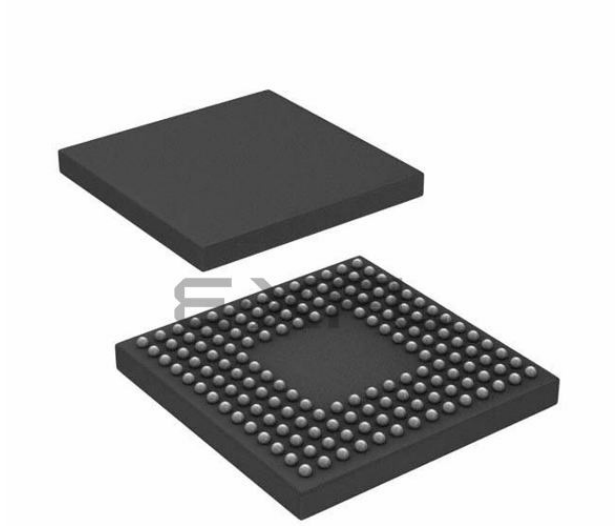

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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Active |
| Type | Fixed Point |
| Interface | SPI, SSP, UART |
| Clock Rate | 400MHz |
| Non-Volatile Memory | ROM (1kB) |
| On-Chip RAM | 84kB |
| Voltage - I/O | 3.30V |
| Voltage - Core | 1.20V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 160-LFBGA, CSPBGA |
| Supplier Device Package | 160-CSPBGA (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/adsp-bf532sbbcz400 |

Each event type has an associated register to hold the return address and an associated return-from-event instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors' event controller consists of two stages, the core event controller (CEC) and the system interrupt controller (SIC). The core event controller works with the system interrupt controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC, and are then routed directly into the general-purpose interrupts of the CEC.

### *Core Event Controller (CEC)*

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the processor. Table 2 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

**Table 2. Core Event Controller (CEC)**

| Priority (0 is Highest) | Event Class | EVT Entry |
|---|---|---|
| 0 | Emulation/Test Control | EMU |
| 1 | Reset | RST |
| 2 | Nonmaskable Interrupt | NMI |
| 3 | Exception | EVX |
| 4 | Reserved | |
| 5 | Hardware Error | IVHW |
| 6 | Core Timer | IVTMR |
| 7 | General Interrupt 7 | IVG7 |
| 8 | General Interrupt 8 | IVG8 |
| 9 | General Interrupt 9 | IVG9 |
| 10 | General Interrupt 10 | IVG10 |
| 11 | General Interrupt 11 | IVG11 |
| 12 | General Interrupt 12 | IVG12 |
| 13 | General Interrupt 13 | IVG13 |
| 14 | General Interrupt 14 | IVG14 |
| 15 | General Interrupt 15 | IVG15 |

### *System Interrupt Controller (SIC)*

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processors provide a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). Table 3 describes the inputs into the SIC and the default mappings into the CEC.

**Table 3. System Interrupt Controller (SIC)**

| Peripheral Interrupt Event | Default Mapping |
|---|---|
| PLL Wakeup | IVG7 |
| DMA Error | IVG7 |
| PPI Error | IVG7 |
| SPORT 0 Error | IVG7 |
| SPORT 1 Error | IVG7 |
| SPI Error | IVG7 |
| UART Error | IVG7 |
| Real-Time Clock | IVG8 |
| DMA Channel 0 (PPI) | IVG8 |
| DMA Channel 1 (SPORT 0 Receive) | IVG9 |
| DMA Channel 2 (SPORT 0 Transmit) | IVG9 |
| DMA Channel 3 (SPORT 1 Receive) | IVG9 |
| DMA Channel 4 (SPORT 1 Transmit) | IVG9 |
| DMA Channel 5 (SPI) | IVG10 |
| DMA Channel 6 (UART Receive) | IVG10 |
| DMA Channel 7 (UART Transmit) | IVG10 |
| Timer 0 | IVG11 |
| Timer 1 | IVG11 |
| Timer 2 | IVG11 |
| Port F GPIO Interrupt A | IVG12 |
| Port F GPIO Interrupt B | IVG12 |
| Memory DMA Stream 0 | IVG13 |
| Memory DMA Stream 1 | IVG13 |
| Software Watchdog Timer | IVG13 |

### *Event Control*

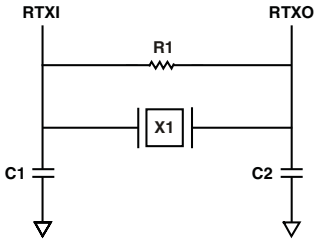
The processors provide a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 32 bits wide:

- CEC interrupt latch register (ILAT) – The ILAT register indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it can also be written to clear (cancel) latched events. This register can be read while in supervisor mode and can only be written while in supervisor mode when the corresponding IMASK bit is cleared.
- CEC interrupt mask register (IMASK) – The IMASK register controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and is processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be latched in the ILAT register. This register can be read or written while in supervisor mode. Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.

The stopwatch function counts down from a programmed value, with one second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like other peripherals, the RTC can wake up the processor from sleep mode upon generation of any RTC wakeup event. Additionally, an RTC wakeup event can wake up the processor from deep sleep mode, and wake up the on-chip internal voltage regulator from a powered-down state.

Connect RTC pins RTXI and RTXO with external components as shown in Figure 6.




SUGGESTED COMPONENTS:
X1 = ECLIPTEK EC38J (THROUGH-HOLE PACKAGE) OR
EPSON MC405 12 pF LOAD (SURFACE-MOUNT PACKAGE)
C1 = 22 pF
C2 = 22 pF
R1 = 10 MΩ

NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

*Figure 6. External Components for RTC*

## WATCHDOG TIMER

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors include a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK), at a maximum frequency of $f_{SCLK}$.

## TIMERS

There are four general-purpose programmable timer units in the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors. Three timers have an external pin that can be configured either as a pulse-width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the PF1 pin (TACLK), an external clock input to the PPI_CLK pin (TMRCLK), or to the internal SCLK.

The timer units can be used in conjunction with the UART to measure the width of the pulses in the data stream to provide an autobaud detect function for a serial channel.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the three general-purpose programmable timers, a fourth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

## SERIAL PORTS (SPORTs)

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- $I^2S$ capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of $I^2S$ stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from ($f_{SCLK}$/131,070) Hz to ($f_{SCLK}$/2) Hz.
- Word length – Each SPORT supports serial data words from 3 bits to 32 bits in length, transferred most-significant-bit first or least-significant-bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.

- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data-word or after transferring an entire data buffer or buffers through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1,024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

An additional 250 mV of SPORT input hysteresis can be enabled by setting Bit 15 of the PLL_CTL register. When this bit is set, all SPORT input pins have the increased hysteresis.

## SERIAL PERIPHERAL INTERFACE (SPI) PORT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have an SPI-compatible port that enables the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins (master output-slave input, MOSI, and master input-slave output, MISO) and a clock pin (serial clock, SCK). An SPI chip select input pin ($\overline{\text{SPISS}}$) lets other SPI devices select the processor, and seven SPI chip select output pins ($\overline{\text{SPISEL7–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface which supports both master/slave modes and multimaster environments.

The baud rate and clock phase/polarities for the SPI port are programmable, and it has an integrated DMA controller, configurable to support transmit or receive data streams. The SPI DMA controller can only service unidirectional accesses at any given time.

The SPI port clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

## UART PORT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provide a full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART port includes support for 5 data bits to 8 data bits, 1 stop bit or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The baud rate, serial data format, error code generation and status, and interrupts for the UART port are programmable.

The UART programmable features include:

- Supporting bit rates ranging from ($f_{SCLK}$/1,048,576) bits per second to ($f_{SCLK}$/16) bits per second.
- Supporting data formats from seven bits to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as:

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16 \times UART\_Divisor}$$

where the 16-bit UART_Divisor comes from the UART_DLH register (most significant 8 bits) and UART_DLL register (least significant 8 bits).

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The capabilities of the UART are further extended with support for the Infrared Data Association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

## GENERAL-PURPOSE I/O PORT F

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have 16 bidirectional, general-purpose I/O pins on Port F (PF15–0). Each general-purpose I/O pin can be individually controlled by manipulation of the GPIO control, status and interrupt registers:

- GPIO direction control register – Specifies the direction of each individual PFx pin as input or output.
- GPIO control and status registers – The processor employs a "write one to modify" mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins. Four control registers are provided. One register is written in order to set GPIO pin values, one register is written in order to clear GPIO pin values, one register is written in order to toggle GPIO pin values, and one register is written in order to specify GPIO pin values. Reading the GPIO status register allows software to interrogate the sense of the GPIO pin.
- GPIO interrupt mask registers – The two GPIO interrupt mask registers allow each individual PFx pin to function as an interrupt to the processor. Similar to the two GPIO control registers that are used to set and clear individual GPIO pin values, one GPIO interrupt mask register sets bits to enable interrupt function, and the other GPIO interrupt mask register clears bits to disable interrupt function.

$t_{NOM}$ is the duration running at $f_{CCLKNOM}$

$t_{RED}$ is the duration running at $f_{CCLKRED}$

The percent power savings is calculated as:

$$\%\ power\ savings\ =\ (1 - power\ savings\ factor) \times 100\%$$

## VOLTAGE REGULATION

The Blackfin processor provides an on-chip voltage regulator that can generate appropriate $V_{DDINT}$ voltage levels from the $V_{DDEXT}$ supply. See Operating Conditions on Page 20 for regulator tolerances and acceptable $V_{DDEXT}$ ranges for specific models.

Figure 7 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power ($V_{DDEXT}$) supplied. While in the hibernate state, I/O power is still being applied, eliminating the need for external buffers. The voltage regulator can be activated from this power-down state either through an RTC wakeup or by asserting $\overline{\text{RESET}}$, both of which initiate a boot sequence. The regulator can also be disabled and bypassed at the user's discretion.

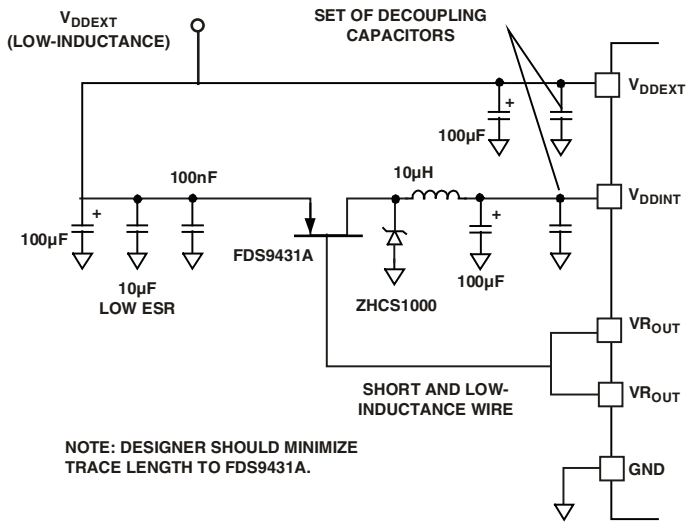



*Figure 7. Voltage Regulator Circuit*

### *Voltage Regulator Layout Guidelines*

Regulator external component placement, board routing, and bypass capacitors all have a significant effect on noise injected into the other analog circuits on-chip. The VROUT1–0 traces and voltage regulator external components should be considered as noise sources when doing board layout and should not be routed or placed near sensitive circuits or components on the board. All internal and I/O power supplies should be well bypassed with bypass capacitors placed as close to the processors as possible.

For further details on the on-chip voltage regulator and related board design guidelines, see the *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228)* applications note on the Analog Devices web site (www.analog.com)—use site search on "EE-228".

## CLOCK SIGNALS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the processors include an on-chip oscillator circuit, an external crystal can be used. For fundamental frequency operation, use the circuit shown in Figure 8.

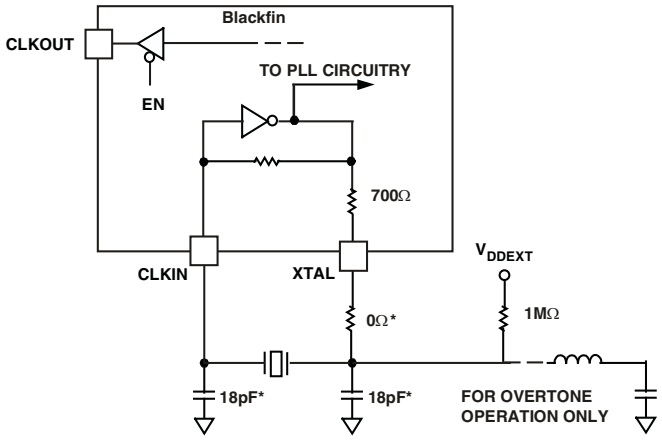



*Figure 8. External Crystal Connections*

A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor shown in Figure 8 fine tune the phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 8 are typical values only. The capacitor values are dependent upon the crystal manufacturer's load capacitance recommendations and the physical PCB layout. The resistor value depends on the drive level specified by the crystal manufacturer. System designs should verify the customized values based on careful investigation on multiple devices over the allowed temperature range.

A third-overtone crystal can be used at frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 8.

more bytes until the flag is deasserted. The GPIO pin is chosen by the user and this information is transferred to the Blackfin processor via bits[10:5] of the FLAG header in the LDR image.

For each of the boot modes, a 10-byte header is first read from an external memory device. The header specifies the number of bytes to be transferred and the memory destination address. Multiple memory blocks can be loaded by any boot sequence. Once all blocks are loaded, program execution commences from the start of L1 instruction SRAM.

In addition, Bit 4 of the reset configuration register can be set by application code to bypass the normal boot sequence during a software reset. For this case, the processor jumps directly to the beginning of L1 instruction memory.

## INSTRUCTION SET DESCRIPTION

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both user (algorithm/application code) and supervisor (O/S kernel, device drivers, debuggers, ISRs) modes of operation, allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/CPU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU + two load/store + two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4G byte memory space, providing a simplified programming model.
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data types; and separate user and supervisor stack pointers.
- Code density enhancements, which include intermixing of 16-bit and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded in 16 bits.

## DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

### *Integrated Development Environments (IDEs)*

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

### *EZ-KIT Lite Evaluation Board*

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

### *EZ-KIT Lite Evaluation Kits*

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

### *Software Add-Ins for CrossCore Embedded Studio*

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

# PIN DESCRIPTIONS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors pin definitions are listed in Table 9.

All pins are three-stated during and immediately after reset, except the memory interface, asynchronous memory control, and synchronous memory control pins. These pins are all driven high, with the exception of CLKOUT, which toggles at the system clock rate. During hibernate, all outputs are three-stated unless otherwise noted in Table 9.

If $\overline{BR}$ is active (whether or not $\overline{RESET}$ is asserted), the memory pins are also three-stated. All unused I/O pins have their input buffers disabled with the exception of the pins that need pull-ups or pull-downs as noted in the table.

In order to maintain maximum functionality and reduce package size and pin count, some pins have dual, multiplexed functionality. In cases where pin functionality is reconfigurable, the default state is shown in plain text, while alternate functionality is shown in italics.

**Table 9. Pin Descriptions**

| Pin Name | Type | Function | Driver Type[1] |
|---|---|---|---|
| *Memory Interface* | | | |
| ADDR19–1 | O | Address Bus for Async/Sync Access | A |
| DATA15–0 | I/O | Data Bus for Async/Sync Access | A |
| $\overline{ABE1–0}$/SDQM1–0 | O | Byte Enables/Data Masks for Async/Sync Access | A |
| $\overline{BR}$ | I | Bus Request (This pin should be pulled high if not used.) | |
| $\overline{BG}$ | O | Bus Grant | A |
| $\overline{BGH}$ | O | Bus Grant Hang | A |
| *Asynchronous Memory Control* | | | |
| $\overline{AMS3–0}$ | O | Bank Select (Require pull-ups if hibernate is used.) | A |
| ARDY | I | Hardware Ready Control (This pin should be pulled high if not used.) | |
| $\overline{AOE}$ | O | Output Enable | A |
| $\overline{ARE}$ | O | Read Enable | A |
| $\overline{AWE}$ | O | Write Enable | A |
| *Synchronous Memory Control* | | | |
| $\overline{SRAS}$ | O | Row Address Strobe | A |
| $\overline{SCAS}$ | O | Column Address Strobe | A |
| $\overline{SWE}$ | O | Write Enable | A |
| SCKE | O | Clock Enable (Requires pull-down if hibernate is used.) | A |
| CLKOUT | O | Clock Output | B |
| SA10 | O | A10 Pin | A |
| $\overline{SMS}$ | O | Bank Select | A |
| *Timers* | | | |
| TMR0 | I/O | Timer 0 | C |
| TMR1/*PPI_FS1* | I/O | Timer 1/*PPI Frame Sync1* | C |
| TMR2/*PPI_FS2* | I/O | Timer 2/*PPI Frame Sync2* | C |
| *PPI Port* | | | |
| PPI3–0 | I/O | PPI3–0 | C |
| PPI_CLK/*TMRCLK* | I | PPI Clock/*External Timer Reference* | |

**Table 9. Pin Descriptions (Continued)**

| Pin Name | Type | Function | Driver Type[1] |
|---|---|---|---|
| *Port F: GPIO/Parallel Peripheral Interface Port/SPI/Timers* | | | |
| PF0/*SPISS* | I/O | GPIO/*SPI Slave Select Input* | C |
| PF1/*SPISEL1*/*TACLK* | I/O | GPIO/*SPI Slave Select Enable 1/Timer Alternate Clock Input* | C |
| PF2/*SPISEL2* | I/O | GPIO/*SPI Slave Select Enable 2* | C |
| PF3/*SPISEL3*/*PPI_FS3* | I/O | GPIO/*SPI Slave Select Enable 3/PPI Frame Sync 3* | C |
| PF4/*SPISEL4*/*PPI15* | I/O | GPIO/*SPI Slave Select Enable 4/PPI 15* | C |
| PF5/*SPISEL5*/*PPI14* | I/O | GPIO/*SPI Slave Select Enable 5/PPI 14* | C |
| PF6/*SPISEL6*/*PPI13* | I/O | GPIO/*SPI Slave Select Enable 6/PPI 13* | C |
| PF7/*SPISEL7*/*PPI12* | I/O | GPIO/*SPI Slave Select Enable 7/PPI 12* | C |
| PF8/*PPI11* | I/O | GPIO/*PPI 11* | C |
| PF9/*PPI10* | I/O | GPIO/*PPI 10* | C |
| PF10/*PPI9* | I/O | GPIO/*PPI 9* | C |
| PF11/*PPI8* | I/O | GPIO/*PPI 8* | C |
| PF12/*PPI7* | I/O | GPIO/*PPI 7* | C |
| PF13/*PPI6* | I/O | GPIO/*PPI 6* | C |
| PF14/*PPI5* | I/O | GPIO/*PPI 5* | C |
| PF15/*PPI4* | I/O | GPIO/*PPI 4* | C |
| *JTAG Port* | | | |
| TCK | I | JTAG Clock | |
| TDO | O | JTAG Serial Data Out | C |
| TDI | I | JTAG Serial Data In | |
| TMS | I | JTAG Mode Select | |
| $\overline{\text{TRST}}$ | I | JTAG Reset (This pin should be pulled low if JTAG is not used.) | |
| $\overline{\text{EMU}}$ | O | Emulation Output | C |
| *SPI Port* | | | |
| MOSI | I/O | Master Out Slave In | C |
| MISO | I/O | Master In Slave Out (This pin should be pulled high through a 4.7 kΩ resistor if booting via the SPI port.) | C |
| SCK | I/O | SPI Clock | D |
| *Serial Ports* | | | |
| RSCLK0 | I/O | SPORT0 Receive Serial Clock | D |
| RFS0 | I/O | SPORT0 Receive Frame Sync | C |
| DR0PRI | I | SPORT0 Receive Data Primary | |
| DR0SEC | I | SPORT0 Receive Data Secondary | |
| TSCLK0 | I/O | SPORT0 Transmit Serial Clock | D |
| TFS0 | I/O | SPORT0 Transmit Frame Sync | C |
| DT0PRI | O | SPORT0 Transmit Data Primary | C |
| DT0SEC | O | SPORT0 Transmit Data Secondary | C |
| RSCLK1 | I/O | SPORT1 Receive Serial Clock | D |

# SPECIFICATIONS

Component specifications are subject to change without notice.

## OPERATING CONDITIONS

| Parameter | | Conditions | Min | Nominal | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDINT}$ | Internal Supply Voltage[1] | Nonautomotive 400 MHz and 500 MHz speed grade models[2] | 0.8 | 1.2 | 1.45 | V |
| $V_{DDINT}$ | Internal Supply Voltage[1] | Nonautomotive 533 MHz speed grade models[2] | 0.8 | 1.25 | 1.45 | V |
| $V_{DDINT}$ | Internal Supply Voltage[1] | 600 MHz speed grade models[2] | 0.8 | 1.30 | 1.45 | V |
| $V_{DDINT}$ | Internal Supply Voltage[1] | Automotive 400 MHz speed grade models[2] | 0.95 | 1.2 | 1.45 | V |
| $V_{DDINT}$ | Internal Supply Voltage[1] | Automotive 533 MHz speed grade models[2] | 0.95 | 1.25 | 1.45 | V |
| $V_{DDEXT}$ | External Supply Voltage[3] | Nonautomotive grade models[2] | 1.75 | 1.8/3.3 | 3.6 | V |
| $V_{DDEXT}$ | External Supply Voltage | Automotive grade models[2] | 2.7 | 3.3 | 3.6 | V |
| $V_{DDRTC}$ | Real-Time Clock Power Supply Voltage | Nonautomotive grade models[2] | 1.75 | 1.8/3.3 | 3.6 | V |
| $V_{DDRTC}$ | Real-Time Clock Power Supply Voltage | Automotive grade models[2] | 2.7 | 3.3 | 3.6 | V |
| $V_{IH}$ | High Level Input Voltage[4, 5] | $V_{DDEXT}$ = 1.85 V | 1.3 | | | V |
| $V_{IH}$ | High Level Input Voltage[4, 5] | $V_{DDEXT}$ = Maximum | 2.0 | | | V |
| $V_{IHCLKIN}$ | High Level Input Voltage[6] | $V_{DDEXT}$ = Maximum | 2.2 | | | V |
| $V_{IL}$ | Low Level Input Voltage[7] | $V_{DDEXT}$ = 1.75 V | | | +0.3 | V |
| $V_{IL}$ | Low Level Input Voltage[7] | $V_{DDEXT}$ = 2.7 V | | | +0.6 | V |
| $T_J$ | Junction Temperature | 160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = 0°C to +70°C | 0 | | +95 | °C |
| $T_J$ | Junction Temperature | 160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +85°C | –40 | | +105 | °C |
| $T_J$ | Junction Temperature | 160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +105°C | –40 | | +125 | °C |
| $T_J$ | Junction Temperature | 169-Ball Plastic Ball Grid Array (PBGA) @ $T_{AMBIENT}$ = –40°C to +105°C | –40 | | +125 | °C |
| $T_J$ | Junction Temperature | 169-Ball Plastic Ball Grid Array (PBGA) @ $T_{AMBIENT}$ = –40°C to +85°C | –40 | | +105 | °C |
| $T_J$ | Junction Temperature | 176-Lead Quad Flatpack (LQFP) @ $T_{AMBIENT}$ = –40°C to +85°C | –40 | | +100 | °C |

[1] The regulator can generate $V_{DDINT}$ at levels of 0.85 V to 1.2 V with –5% to +10% tolerance, 1.25 V with –4% to +10% tolerance, and 1.3 V with –0% to +10% tolerance.

[2] See Ordering Guide on Page 63.

[3] When $V_{DDEXT}$ < 2.25 V, on-chip voltage regulation is not supported.

[4] Applies to all input and bidirectional pins except CLKIN.

[5] The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are 3.3 V tolerant (always accepts up to 3.6 V maximum $V_{IH}$), but voltage compliance (on outputs, $V_{OH}$) depends on the input $V_{DDEXT}$, because $V_{OH}$ (maximum) approximately equals $V_{DDEXT}$ (maximum). This 3.3 V tolerance applies to bidirectional pins (DATA15–0, TMR2–0, PF15–0, PPI3–0, RSCLK1–0, TSCLK1–0, RFS1–0, TFS1–0, MOSI, MISO, SCK) and input only pins ($\overline{BR}$, ARDY, PPI_CLK, DR0PRI, DR0SEC, DR1PRI, DR1SEC, RX, RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, NMI, and BMODE1–0).

[6] Applies to CLKIN pin only.

[7] Applies to all input and bidirectional pins.

## ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 18 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

**Table 18. Absolute Maximum Ratings**

| Parameter | Rating |
|---|---|
| Internal (Core) Supply Voltage ($V_{DDINT}$) | –0.3 V to +1.45 V |
| External (I/O) Supply Voltage ($V_{DDEXT}$) | –0.5 V to +3.8 V |
| Input Voltage[1, 2] | –0.5 V to +3.8 V |
| Output Voltage Swing | –0.5 V to $V_{DDEXT}$ + 0.5 V |
| Storage Temperature Range | –65°C to +150°C |
| Junction Temperature While Biased | 125°C |

[1] Applies to 100% transient duty cycle. For other duty cycles see Table 19.
[2] Applies only when $V_{DDEXT}$ is within specifications. When $V_{DDEXT}$ is outside specifications, the range is $V_{DDEXT}$ ± 0.2 V.

**Table 19. Maximum Duty Cycle for Input Transient Voltage[1]**

| $V_{IN}$ Min (V)[2] | $V_{IN}$ Max (V)[2] | Maximum Duty Cycle[3] |
|---|---|---|
| –0.50 | +3.80 | 100% |
| –0.70 | +4.00 | 40% |
| –0.80 | +4.10 | 25% |
| –0.90 | +4.20 | 15% |
| –1.00 | +4.30 | 10% |

[1] Applies to all signal pins with the exception of CLKIN, XTAL, VROUT1–0.
[2] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.
[3] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

## ESD SENSITIVITY

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

### *Parallel Peripheral Interface Timing*

Table 27 and Figure 17 through Figure 22 describe parallel peripheral interface operations.

**Table 27. Parallel Peripheral Interface Timing**

| Parameter | | $V_{DDEXT}$ = 1.8 V LQFP/PBGA Packages Min | Max | $V_{DDEXT}$ = 1.8 V CSP_BGA Package Min | Max | $V_{DDEXT}$ = 2.5 V/3.3 V All Packages Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | | | |
| $t_{PCLKW}$ | PPI_CLK Width | 8.0 | | 8.0 | | 6.0 | | ns |
| $t_{PCLK}$ | PPI_CLK Period[1] | 20.0 | | 20.0 | | 15.0 | | ns |
| $t_{SFSPE}$ | External Frame Sync Setup Before PPI_CLK Edge (Nonsampling Edge for Rx, Sampling Edge for Tx) | 6.0 | | 6.0 | | 4.0[2] | | ns<br>ns |
| $t_{HFSPE}$ | External Frame Sync Hold After PPI_CLK | 1.0[2] | | 1.0[2] | | 1.0[2] | | ns |
| $t_{SDRPE}$ | Receive Data Setup Before PPI_CLK | 3.5 | | 3.5 | | 3.5 | | ns |
| $t_{HDRPE}$ | Receive Data Hold After PPI_CLK | 1.5 | | 1.5 | | 1.5 | | ns |
| *Switching Characteristics—GP Output and Frame Capture Modes* | | | | | | | | |
| $t_{DFSPE}$ | Internal Frame Sync Delay After PPI_CLK | | 11.0 | | 8.0 | | 8.0 | ns |
| $t_{HOFSPE}$ | Internal Frame Sync Hold After PPI_CLK | 1.7 | | 1.7 | | 1.7 | | ns |
| $t_{DDTPE}$ | Transmit Data Delay After PPI_CLK | | 11.0 | | 9.0 | | 9.0 | ns |
| $t_{HDTPE}$ | Transmit Data Hold After PPI_CLK | 1.8 | | 1.8 | | 1.8 | | ns |

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$.
[2] Applies when PPI_CONTROL Bit 8 is cleared. See Figure 19 and Figure 22.

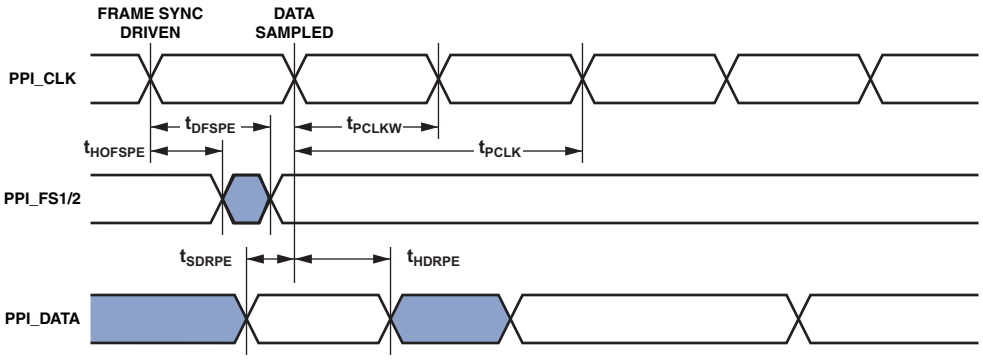



*Figure 17. PPI GP Rx Mode with Internal Frame Sync Timing*

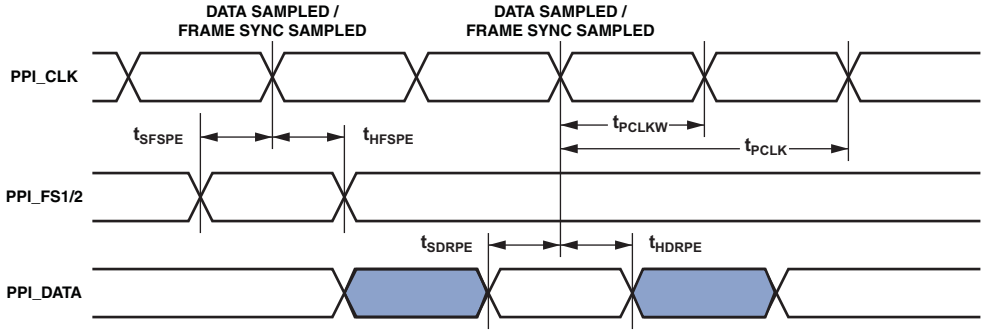



*Figure 18. PPI GP Rx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 1)*

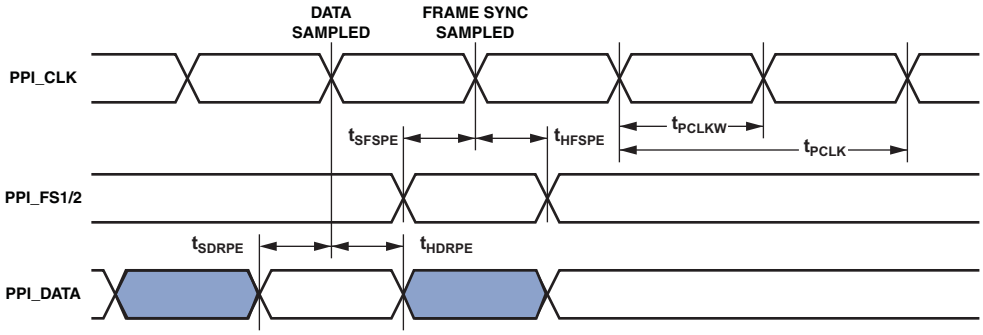



*Figure 19. PPI GP Rx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 0)*

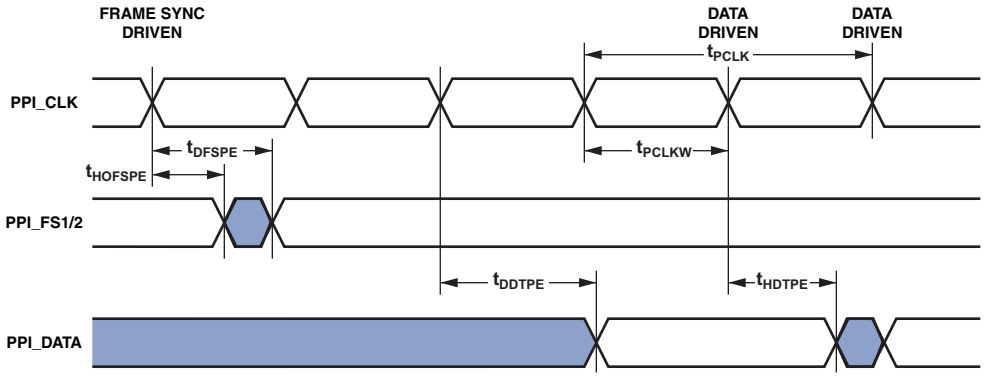



*Figure 20. PPI GP Tx Mode with Internal Frame Sync Timing*

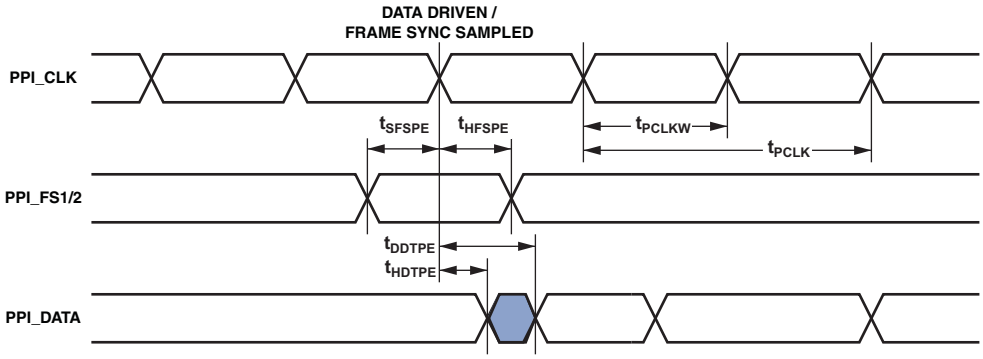



*Figure 21. PPI GP Tx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 1)*

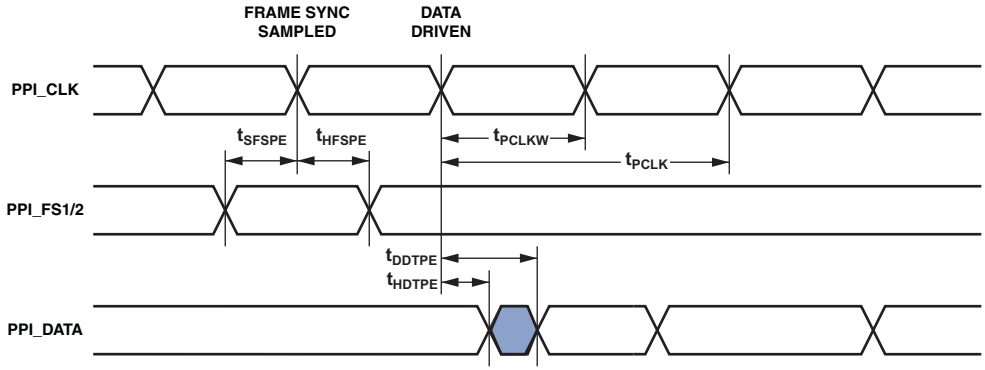



*Figure 22. PPI GP Tx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 0)*

### *Serial Peripheral Interface (SPI) Port—Slave Timing*

**Table 33. Serial Peripheral Interface (SPI) Port—Slave Timing**

| Parameter | | $V_{DDEXT}$ = 1.8 V LQFP/PBGA Packages Min | Max | $V_{DDEXT}$ = 1.8 V CSP_BGA Package Min | Max | $V_{DDEXT}$ = 2.5 V/3.3 V All Packages Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | | | |
| $t_{SPICHS}$ | Serial Clock High Period | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPICLS}$ | Serial Clock Low Period | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPICLK}$ | Serial Clock Period | $4 \times t_{SCLK}$ | | $4 \times t_{SCLK}$ | | $4 \times t_{SCLK}$ | | ns |
| $t_{HDS}$ | Last SCK Edge to $\overline{SPISS}$ Not Asserted | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPITDS}$ | Sequential Transfer Delay | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SDSCI}$ | $\overline{SPISS}$ Assertion to First SCK Edge | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SSPID}$ | Data Input Valid to SCK Edge (Data Input Setup) | 1.6 | | 1.6 | | 1.6 | | ns |
| $t_{HSPID}$ | SCK Sampling Edge to Data Input Invalid | 1.6 | | 1.6 | | 1.6 | | ns |
| *Switching Characteristics* | | | | | | | | |
| $t_{DSOE}$ | $\overline{SPISS}$ Assertion to Data Out Active | 0 | 10 | 0 | 9 | 0 | 8 | ns |
| $t_{DSDHI}$ | $\overline{SPISS}$ Deassertion to Data High Impedance | 0 | 10 | 0 | 9 | 0 | 8 | ns |
| $t_{DDSPID}$ | SCK Edge to Data Out Valid (Data Out Delay) | | 10 | | 10 | | 10 | ns |
| $t_{HDSPID}$ | SCK Edge to Data Out Invalid (Data Out Hold) | 0 | | 0 | | 0 | | ns |

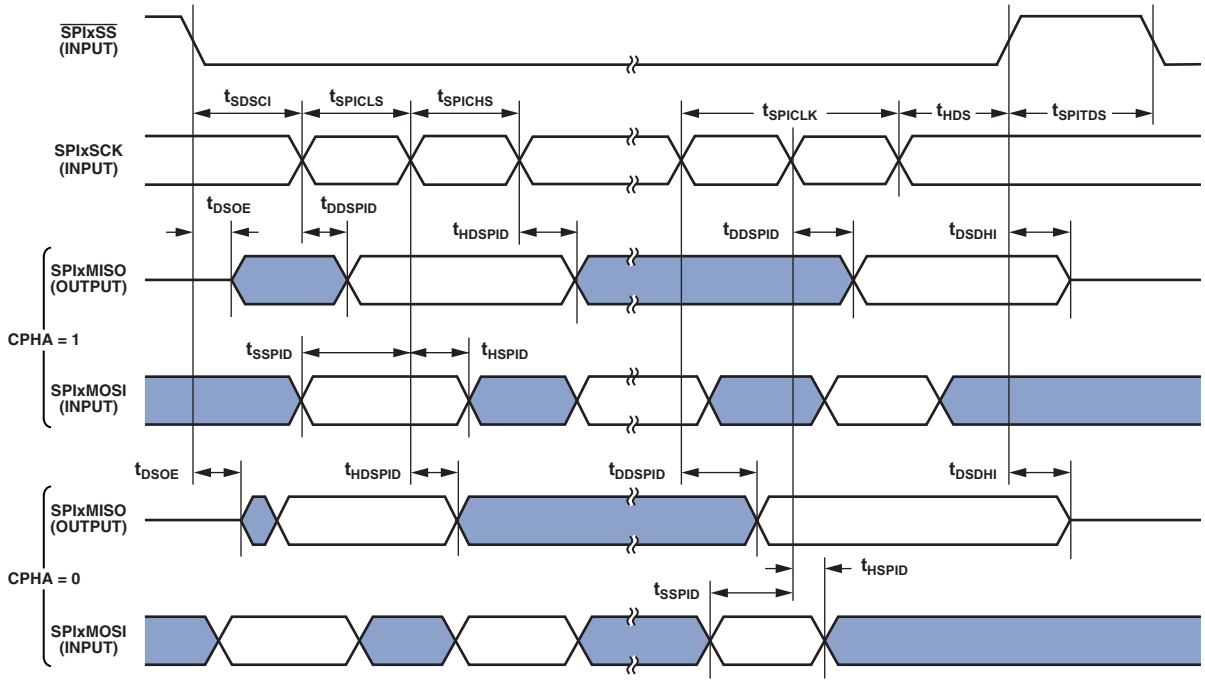
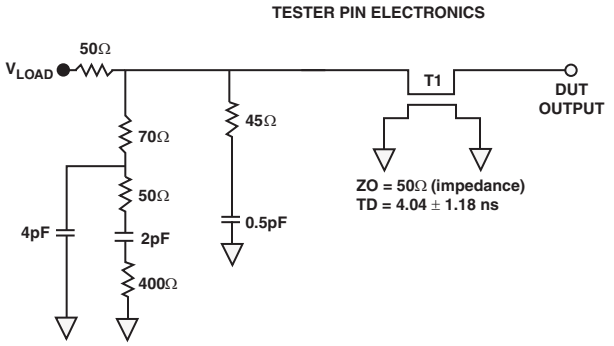



*Figure 28. Serial Peripheral Interface (SPI) Port—Slave Timing*

### *Capacitive Loading*

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 47). $V_{LOAD}$ is 0.95 V for $V_{DDEXT}$ (nominal) = 1.8 V or 1.5 V for $V_{DDEXT}$ (nominal) = 2.5 V/3.3 V. Figure 48 through Figure 59 on Page 48 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.




NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

*Figure 47. Equivalent Device Loading for AC Measurements (Includes All Fixtures)*

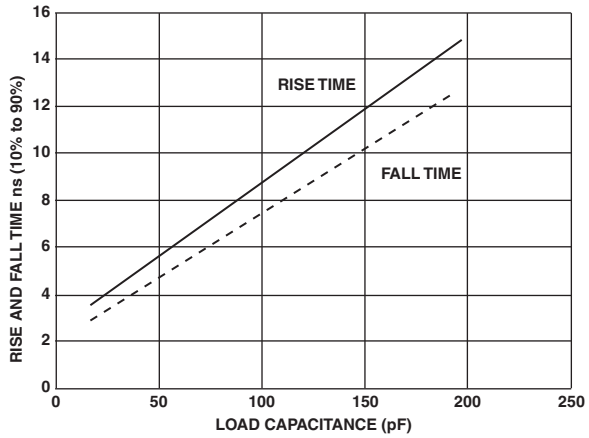



*Figure 48. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at $V_{DDEXT}$ = 1.75 V*

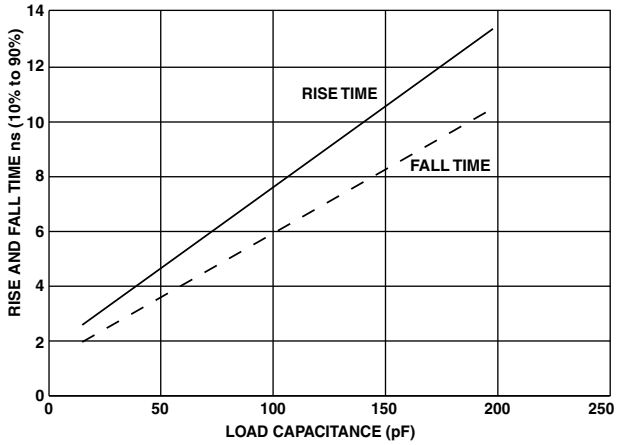



*Figure 49. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at $V_{DDEXT}$ = 2.25 V*

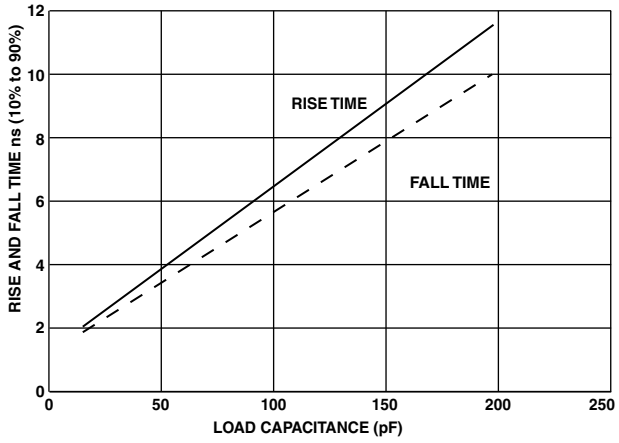



*Figure 50. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at $V_{DDEXT}$ = 3.65 V*

## THERMAL CHARACTERISTICS

To determine the junction temperature on the application printed circuit board, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

$T_J$ = Junction temperature (°C).

$T_{CASE}$ = Case temperature (°C) measured by customer at top center of package.

$\Psi_{JT}$ = From Table 38 through Table 40.

$P_D$ = Power dissipation (see the power dissipation discussion and the tables on 23 for the method to calculate $P_D$).

Values of $\theta_{JA}$ are provided for package comparison and printed circuit board design considerations. $\theta_{JA}$ can be used for a first order approximation of $T_J$ by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

$T_A$ = ambient temperature (°C).

In Table 38 through Table 40, airflow measurements comply with JEDEC standards JESD51–2 and JESD51–6, and the junction-to-board measurement complies with JESD51–8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Thermal resistance $\theta_{JA}$ in Table 38 through Table 40 is the figure of merit relating to performance of the package and board in a convective environment. $\theta_{JMA}$ represents the thermal resistance under two conditions of airflow. $\Psi_{JT}$ represents the correlation between $T_J$ and $T_{CASE}$.

**Table 38. Thermal Characteristics for BC-160 Package**

| Parameter | Condition | Typical | Unit |
|---|---|---|---|
| $\theta_{JA}$ | 0 Linear m/s Airflow | 27.1 | °C/W |
| $\theta_{JMA}$ | 1 Linear m/s Airflow | 23.85 | °C/W |
| $\theta_{JMA}$ | 2 Linear m/s Airflow | 22.7 | °C/W |
| $\theta_{JC}$ | Not Applicable | 7.26 | °C/W |
| $\Psi_{JT}$ | 0 Linear m/s Airflow | 0.14 | °C/W |
| $\Psi_{JT}$ | 1 Linear m/s Airflow | 0.26 | °C/W |
| $\Psi_{JT}$ | 2 Linear m/s Airflow | 0.35 | °C/W |

**Table 39. Thermal Characteristics for ST-176-1 Package**

| Parameter | Condition | Typical | Unit |
|---|---|---|---|
| $\theta_{JA}$ | 0 Linear m/s Airflow | 34.9 | °C/W |
| $\theta_{JMA}$ | 1 Linear m/s Airflow | 33.0 | °C/W |
| $\theta_{JMA}$ | 2 Linear m/s Airflow | 32.0 | °C/W |
| $\Psi_{JT}$ | 0 Linear m/s Airflow | 0.50 | °C/W |
| $\Psi_{JT}$ | 1 Linear m/s Airflow | 0.75 | °C/W |
| $\Psi_{JT}$ | 2 Linear m/s Airflow | 1.00 | °C/W |

**Table 40. Thermal Characteristics for B-169 Package**

| Parameter | Condition | Typical | Unit |
|---|---|---|---|
| $\theta_{JA}$ | 0 Linear m/s Airflow | 22.8 | °C/W |
| $\theta_{JMA}$ | 1 Linear m/s Airflow | 20.3 | °C/W |
| $\theta_{JMA}$ | 2 Linear m/s Airflow | 19.3 | °C/W |
| $\theta_{JC}$ | Not Applicable | 10.39 | °C/W |
| $\Psi_{JT}$ | 0 Linear m/s Airflow | 0.59 | °C/W |
| $\Psi_{JT}$ | 1 Linear m/s Airflow | 0.88 | °C/W |
| $\Psi_{JT}$ | 2 Linear m/s Airflow | 1.37 | °C/W |

# 169-BALL PBGA BALL ASSIGNMENT

Table 43 lists the PBGA ball assignment by signal. Table 44 on Page 54 lists the PBGA ball assignment by ball number.

**Table 43. 169-Ball PBGA Ball Assignment (Alphabetical by Signal)**

| Signal | Ball No. | Signal | Ball No. | Signal | Ball No. | Signal | Ball No. | Signal | Ball No. |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{ABE0}$ | H16 | DATA4 | U12 | GND | K9 | RTXI | A10 | $V_{DDEXT}$ | K6 |
| $\overline{ABE1}$ | H17 | DATA5 | U11 | GND | K10 | RTXO | A11 | $V_{DDEXT}$ | L6 |
| ADDR1 | J16 | DATA6 | T10 | GND | K11 | RX | T1 | $V_{DDEXT}$ | M6 |
| ADDR2 | J17 | DATA7 | U10 | GND | L7 | SA10 | B15 | $V_{DDEXT}$ | M7 |
| ADDR3 | K16 | DATA8 | T9 | GND | L8 | $\overline{SCAS}$ | A16 | $V_{DDEXT}$ | M8 |
| ADDR4 | K17 | DATA9 | U9 | GND | L9 | SCK | D1 | $V_{DDEXT}$ | T2 |
| ADDR5 | L16 | DATA10 | T8 | GND | L10 | SCKE | B14 | VROUT0 | B12 |
| ADDR6 | L17 | DATA11 | U8 | GND | L11 | $\overline{SMS}$ | A17 | VROUT1 | B13 |
| ADDR7 | M16 | DATA12 | U7 | GND | M9 | $\overline{SRAS}$ | A15 | XTAL | A13 |
| ADDR8 | M17 | DATA13 | T7 | GND | T16 | $\overline{SWE}$ | B17 | | |
| ADDR9 | N17 | DATA14 | U6 | MISO | E2 | TCK | U4 | | |
| ADDR10 | N16 | DATA15 | T6 | MOSI | E1 | TDI | U3 | | |
| ADDR11 | P17 | DR0PRI | M2 | NMI | B11 | TDO | T4 | | |
| ADDR12 | P16 | DR0SEC | M1 | PF0 | D2 | TFS0 | L1 | | |
| ADDR13 | R17 | DR1PRI | H1 | PF1 | C1 | TFS1 | G2 | | |
| ADDR14 | R16 | DR1SEC | H2 | PF2 | B1 | TMR0 | R1 | | |
| ADDR15 | T17 | DT0PRI | K2 | PF3 | C2 | TMR1 | P2 | | |
| ADDR16 | U15 | DT0SEC | K1 | PF4 | A1 | TMR2 | P1 | | |
| ADDR17 | T15 | DT1PRI | F1 | PF5 | A2 | TMS | T3 | | |
| ADDR18 | U16 | DT1SEC | F2 | PF6 | B3 | $\overline{TRST}$ | U2 | | |
| ADDR19 | T14 | $\overline{EMU}$ | U1 | PF7 | A3 | TSCLK0 | L2 | | |
| $\overline{AMS0}$ | D17 | GND | B16 | PF8 | B4 | TSCLK1 | G1 | | |
| $\overline{AMS1}$ | E16 | GND | F11 | PF9 | A4 | TX | R2 | | |
| $\overline{AMS2}$ | E17 | GND | G7 | PF10 | B5 | VDD | F12 | | |
| $\overline{AMS3}$ | F16 | GND | G8 | PF11 | A5 | VDD | G12 | | |
| $\overline{AOE}$ | F17 | GND | G9 | PF12 | A6 | VDD | H12 | | |
| ARDY | C16 | GND | G10 | PF13 | B6 | VDD | J12 | | |
| $\overline{ARE}$ | G16 | GND | G11 | PF14 | A7 | VDD | K12 | | |
| $\overline{AWE}$ | G17 | GND | H7 | PF15 | B7 | VDD | L12 | | |
| $\overline{BG}$ | T13 | GND | H8 | PPI_CLK | B10 | VDD | M10 | | |
| $\overline{BGH}$ | U17 | GND | H9 | PPI0 | B9 | VDD | M11 | | |
| BMODE0 | U5 | GND | H10 | PPI1 | A9 | VDD | M12 | | |
| BMODE1 | T5 | GND | H11 | PPI2 | B8 | $V_{DDEXT}$ | B2 | | |
| $\overline{BR}$ | C17 | GND | J7 | PPI3 | A8 | $V_{DDEXT}$ | F6 | | |
| CLKIN | A14 | GND | J8 | $\overline{RESET}$ | A12 | $V_{DDEXT}$ | F7 | | |
| CLKOUT | D16 | GND | J9 | RFS0 | N1 | $V_{DDEXT}$ | F8 | | |
| DATA0 | U14 | GND | J10 | RFS1 | J1 | $V_{DDEXT}$ | F9 | | |
| DATA1 | T12 | GND | J11 | RSCLK0 | N2 | $V_{DDEXT}$ | G6 | | |
| DATA2 | U13 | GND | K7 | RSCLK1 | J2 | $V_{DDEXT}$ | H6 | | |
| DATA3 | T11 | GND | K8 | RTCVDD | F10 | $V_{DDEXT}$ | J6 | | |

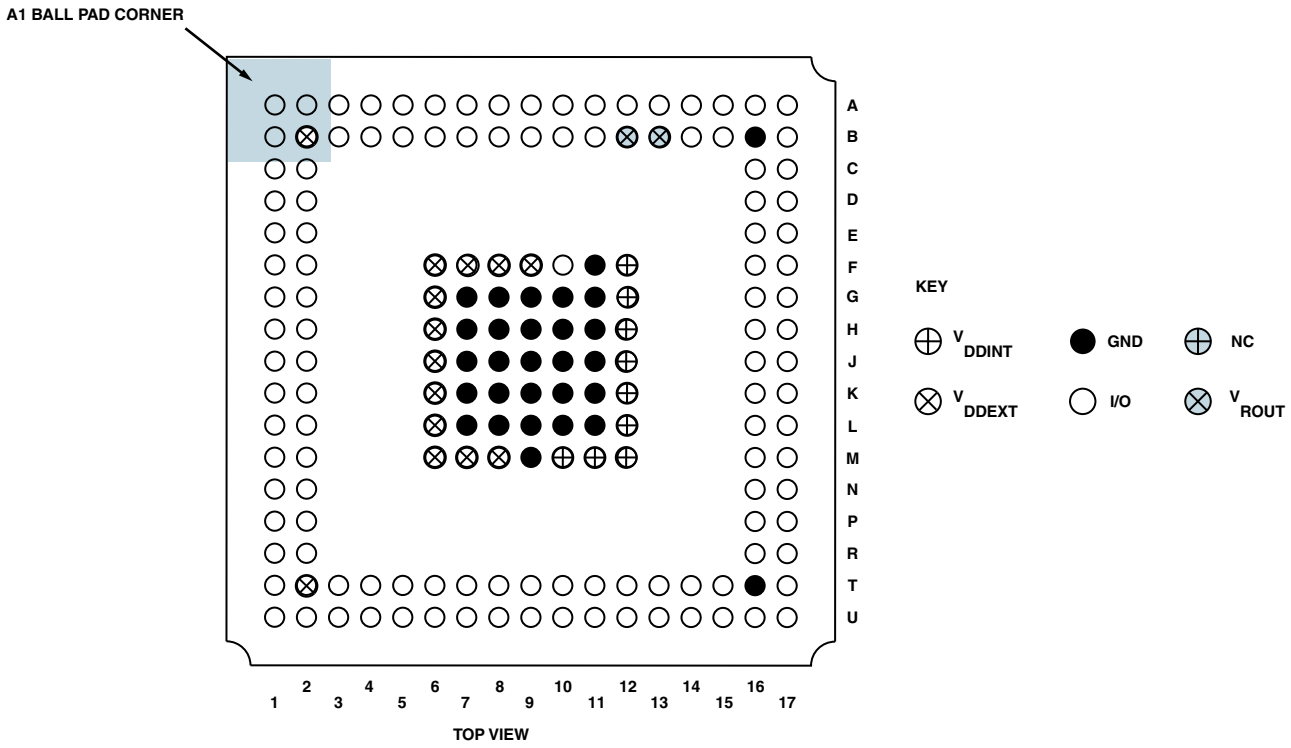



*Figure 62. 169-Ball PBGA Ground Configuration (Top View)*

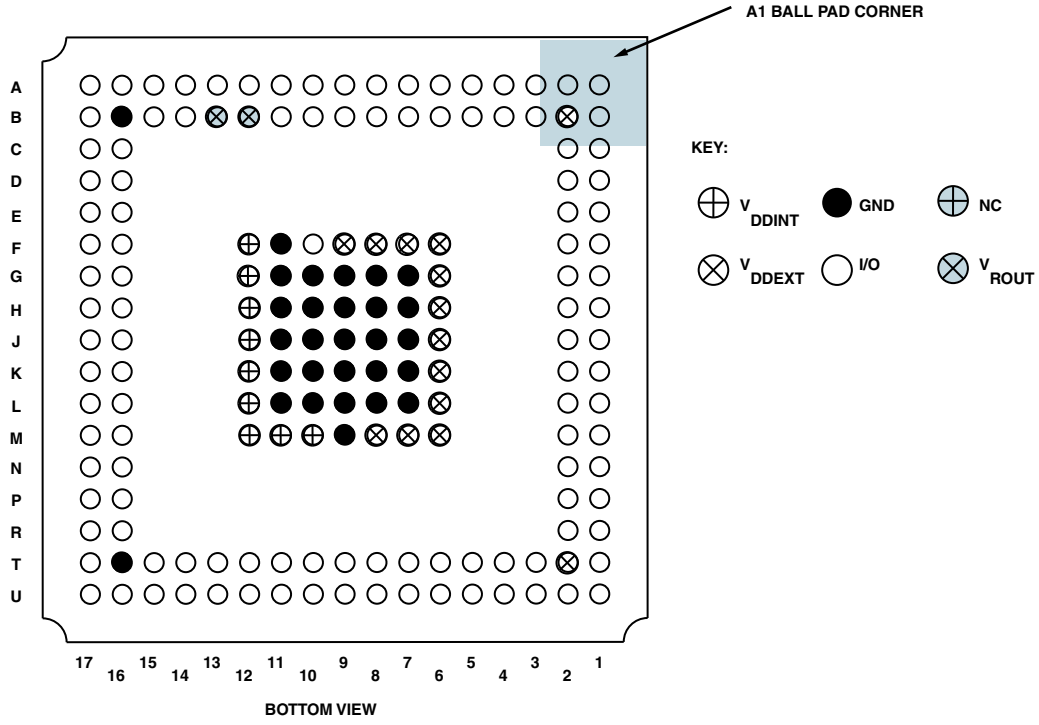



*Figure 63. 169-Ball PBGA Ground Configuration (Bottom View)*

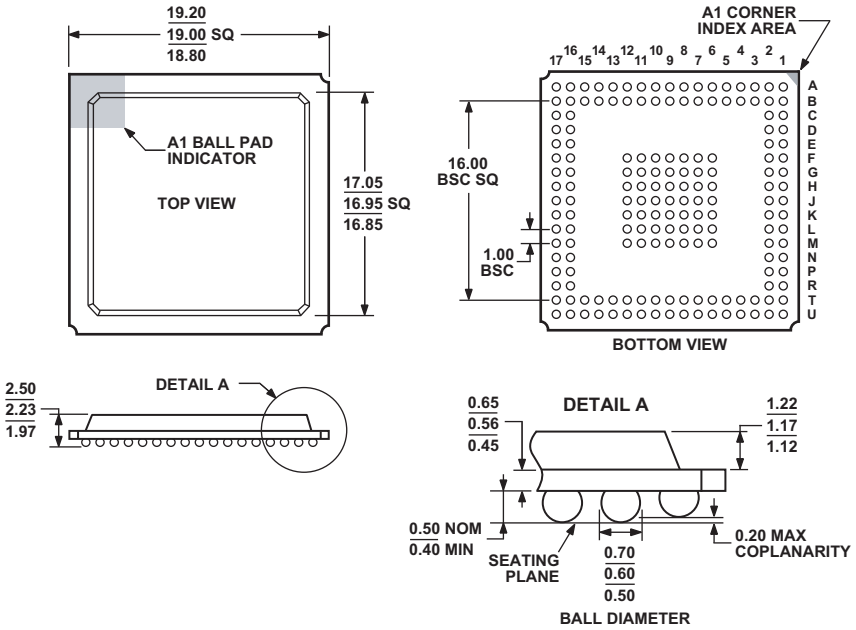



*Figure 66. 169-Ball Plastic Ball Grid Array [PBGA]*
*(B-169)*
*Dimensions shown in millimeters*

## AUTOMOTIVE PRODUCTS

The ADBF531W, ADBF532W, and ADBF533W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 48 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

**Table 48. Automotive Products**

| Product Family[1,2] | Temperature Range[3] | Speed Grade (Max) | Package Description | Package Option |
|---|---|---|---|---|
| ADBF531WBSTZ4xx | –40°C to +85°C | 400 MHz | 176-Lead LQFP | ST-176-1 |
| ADBF531WBBCZ4xx | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADBF531WYBCZ4xx | –40°C to +105°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADBF532WBSTZ4xx | –40°C to +85°C | 400 MHz | 176-Lead LQFP | ST-176-1 |
| ADBF532WBBCZ4xx | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADBF532WYBCZ4xx | –40°C to +105°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADBF533WBBCZ5xx | –40°C to +85°C | 533 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADBF533WBBZ5xx | –40°C to +85°C | 533 MHz | 169-Ball PBGA | B-169 |
| ADBF533WYBCZ4xx | –40°C to +105°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADBF533WYBBZ4xx | –40°C to +105°C | 400 MHz | 169-Ball PBGA | B-169 |

[1] Z = RoHS compliant part.
[2] xx denotes silicon revision.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 20 for junction temperature ($T_J$) specification which is the only temperature specification.

## ORDERING GUIDE

| Model [1] | Temperature Range [2] | Speed Grade (Max) | Package Description | Package Option |
|---|---|---|---|---|
| ADSP-BF531SBB400 | –40°C to +85°C | 400 MHz | 169-Ball PBGA | B-169 |
| ADSP-BF531SBBZ400 | –40°C to +85°C | 400 MHz | 169-Ball PBGA | B-169 |
| ADSP-BF531SBBC400 | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF531SBBCZ400 | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF531SBBCZ4RL | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA, 13" Tape and Reel | BC-160-2 |
| ADSP-BF531SBSTZ400 | –40°C to +85°C | 400 MHz | 176-Lead LQFP | ST-176-1 |
| ADSP-BF532SBBZ400 | –40°C to +85°C | 400 MHz | 169-Ball PBGA | B-169 |
| ADSP-BF532SBBC400 | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF532SBBCZ400 | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF532SBSTZ400 | –40°C to +85°C | 400 MHz | 176-Lead LQFP | ST-176-1 |
| ADSP-BF533SBBZ400 | –40°C to +85°C | 400 MHz | 169-Ball PBGA | B-169 |
| ADSP-BF533SBBC400 | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF533SBBCZ400 | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF533SBSTZ400 | –40°C to +85°C | 400 MHz | 176-Lead LQFP | ST-176-1 |
| ADSP-BF533SBB500 | –40°C to +85°C | 500 MHz | 169-Ball PBGA | B-169 |
| ADSP-BF533SBBZ500 | –40°C to +85°C | 500 MHz | 169-Ball PBGA | B-169 |
| ADSP-BF533SBBC500 | –40°C to +85°C | 500 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF533SBBCZ500 | –40°C to +85°C | 500 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF533SBBC-5V | –40°C to +85°C | 533 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF533SBBCZ-5V | –40°C to +85°C | 533 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF533SKBC-6V | 0°C to +70°C | 600 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF533SKBCZ-6V | 0°C to +70°C | 600 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF533SKSTZ-5V | 0°C to +70°C | 533 MHz | 176-Lead LQFP | ST-176-1 |

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 20 for junction temperature ($T_J$) specification which is the only temperature specification.