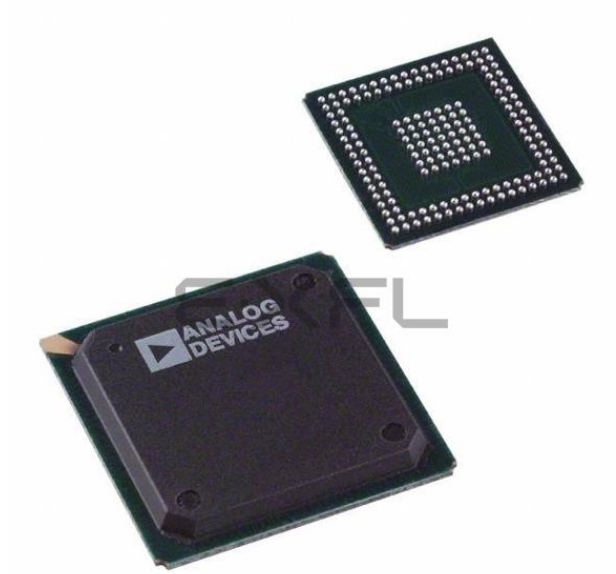


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	400MHz
Non-Volatile Memory	ROM (1kB)
On-Chip RAM	84kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-BBGA
Supplier Device Package	169-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf532sbbz400

TABLE OF CONTENTS

Features 1
Memory 1
Peripherals 1
General Description 3
Portable Low Power Architecture 3
System Integration 3
Processor Peripherals 3
Blackfin Processor Core 4
Memory Architecture 4
DMA Controllers 8
Real-Time Clock 8
Watchdog Timer 9
Timers 9
Serial Ports (SPORTs) 9
Serial Peripheral Interface (SPI) Port 10
UART Port 10
General-Purpose I/O Port F 10
Parallel Peripheral Interface 11
Dynamic Power Management 11
Voltage Regulation 13
Clock Signals 13
Booting Modes 14
Instruction Set Description 15
Development Tools 15
Additional Information 16
Related Signal Chains 16
Pin Descriptions 17
Specifications 20
Operating Conditions 20
Electrical Characteristics 22
Absolute Maximum Ratings 25
ESD Sensitivity 25
Package Information 26
Timing Specifications 27
Output Drive Currents 43
Test Conditions 45
Thermal Characteristics 49
160-Ball CSP_BGA Ball Assignment 50
169-Ball PBGA Ball Assignment 53
176-Lead LQFP Pinout 56
Outline Dimensions 58
Surface-Mount Design 61
Automotive Products 62
Ordering Guide 63

REVISION HISTORY

8/13— Rev. H to Rev. I

Updated Development Tools 15

Corrected Conditions value of the V_{IL} specification in Operating Conditions 20

Added notes to Table 30 in Serial Ports—Enable and Three-State 36

Added Timer Clock Timing 41

Revised Timer Cycle Timing 41

Updated Ordering Guide 63

BLACKFIN PROCESSOR CORE

As shown in Figure 2 on Page 5, the Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-bit, 16-bit, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo 2^{32} multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions includes byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). Quad 16-bit operations are possible using the second ALU.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

MEMORY ARCHITECTURE

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors view memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low latency on-chip memory as cache or SRAM, and larger, lower cost and performance off-chip memory systems. See Figure 3, Figure 4, and Figure 5 on Page 6.

The L1 memory system is the primary highest performance memory available to the Blackfin processor. The off-chip memory system, accessed through the external bus interface unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing up to 132M bytes of physical memory.

The memory DMA controller provides high bandwidth data-movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

Internal (On-Chip) Memory

The processors have three blocks of on-chip memory that provide high bandwidth access to the core.

The first block is the L1 instruction memory, consisting of up to 80K bytes SRAM, of which 16K bytes can be configured as a four way set-associative cache. This memory is accessed at full processor speed.

- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data-word or after transferring an entire data buffer or buffers through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1,024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

An additional 250 mV of SPORT input hysteresis can be enabled by setting Bit 15 of the PLL_CTL register. When this bit is set, all SPORT input pins have the increased hysteresis.

SERIAL PERIPHERAL INTERFACE (SPI) PORT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have an SPI-compatible port that enables the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins (master output-slave input, MOSI, and master input-slave output, MISO) and a clock pin (serial clock, SCK). An SPI chip select input pin ($\overline{\text{SPISS}}$) lets other SPI devices select the processor, and seven SPI chip select output pins ($\overline{\text{SPISEL7–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface which supports both master/slave modes and multimaster environments.

The baud rate and clock phase/polarities for the SPI port are programmable, and it has an integrated DMA controller, configurable to support transmit or receive data streams. The SPI DMA controller can only service unidirectional accesses at any given time.

The SPI port clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provide a full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART port includes support for 5 data bits to 8 data bits, 1 stop bit or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The baud rate, serial data format, error code generation and status, and interrupts for the UART port are programmable.

The UART programmable features include:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) bits per second to (f_{SCLK}/16) bits per second.
- Supporting data formats from seven bits to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as:

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16 \times UART\_Divisor}$$

where the 16-bit UART_Divisor comes from the UART_DLH register (most significant 8 bits) and UART_DLL register (least significant 8 bits).

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The capabilities of the UART are further extended with support for the Infrared Data Association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

GENERAL-PURPOSE I/O PORT F

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have 16 bidirectional, general-purpose I/O pins on Port F (PF15–0). Each general-purpose I/O pin can be individually controlled by manipulation of the GPIO control, status and interrupt registers:

- GPIO direction control register – Specifies the direction of each individual PFx pin as input or output.
- GPIO control and status registers – The processor employs a "write one to modify" mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins. Four control registers are provided. One register is written in order to set GPIO pin values, one register is written in order to clear GPIO pin values, one register is written in order to toggle GPIO pin values, and one register is written in order to specify GPIO pin values. Reading the GPIO status register allows software to interrogate the sense of the GPIO pin.
- GPIO interrupt mask registers – The two GPIO interrupt mask registers allow each individual PFx pin to function as an interrupt to the processor. Similar to the two GPIO control registers that are used to set and clear individual GPIO pin values, one GPIO interrupt mask register sets bits to enable interrupt function, and the other GPIO interrupt mask register clears bits to disable interrupt function.

Active Operating Mode—Moderate Power Savings

In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. DMA access is available to appropriately configured L1 memories.

In the active mode, it is possible to disable the PLL through the PLL control register (PLL_CTL). If disabled, the PLL must be re-enabled before it can transition to the full-on or sleep modes.

Table 4. Power Settings

Mode	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)	Internal Power (V_{DDINT})
Full On	Enabled	No	Enabled	Enabled	On
Active	Enabled/ Disabled	Yes	Enabled	Enabled	On
Sleep	Enabled	—	Disabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event or RTC activity will wake up the processor. When in the sleep mode, assertion of wakeup causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor will transition to the full-on mode. If BYPASS is enabled, the processor will transition to the active mode.

When in the sleep mode, system DMA access to L1 memory is not supported.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals, such as the RTC, may still be running but cannot access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. When in deep sleep mode, an RTC asynchronous interrupt causes the processor to transition to the active mode. Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full-on mode.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and to all the synchronous peripherals (SCLK). The internal voltage regulator for the processor can be shut off by writing b#00 to the FREQ bits of the VR_CTL register. In addition to disabling the clocks, this sets the internal power supply voltage (V_{DDINT}) to 0 V to provide the lowest static power dissipation. Any critical information stored internally (memory contents, register contents, etc.) must be written to a nonvolatile storage device prior to removing power if the processor state is to be preserved. Since V_{DDEXT} is still supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current. The internal supply regulator can be woken up either by a real-time clock wakeup or by asserting the $\overline{\text{RESET}}$ pin.

Power Savings

As shown in Table 5, the processors support three different power domains. The use of multiple power domains maximizes flexibility, while maintaining compliance with industry standards and conventions. By isolating the internal logic of the processor into its own power domain, separate from the RTC and other I/O, the processor can take advantage of dynamic power management without affecting the RTC or other I/O devices. There are no sequencing requirements for the various power domains.

Table 5. Power Domains

Power Domain	V_{DD} Range
All internal logic, except RTC	V_{DDINT}
RTC internal logic and crystal I/O	V_{DDRTC}
All other I/O	V_{DDEXT}

The power dissipated by a processor is largely a function of the clock frequency of the processor and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic.

The dynamic power management feature of the processor allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The savings in power dissipation can be modeled using the power savings factor and % power savings calculations.

The power savings factor is calculated as:

$$\textit{power savings factor} = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{t_{RED}}{t_{NOM}}\right)$$

where the variables in the equation are:

$f_{CCLKNOM}$ is the nominal core clock frequency

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage

$V_{DDINTRED}$ is the reduced internal supply voltage

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *“Analog Devices JTAG Emulation Technical Reference”* (EE-68) on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started With Blackfin Processors*
- *ADSP-BF533 Blackfin Processor Hardware Reference*
- *Blackfin Processor Programming Reference*
- *ADSP-BF531/ADSP-BF532/ADSP-BF533 Blackfin Processor Anomaly List*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

SPECIFICATIONS

Component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 400 MHz and 500 MHz speed grade models[2]	0.8	1.2	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 533 MHz speed grade models[2]	0.8	1.25	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	600 MHz speed grade models[2]	0.8	1.30	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	Automotive 400 MHz speed grade models[2]	0.95	1.2	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	Automotive 533 MHz speed grade models[2]	0.95	1.25	1.45	V
V_{DDEXT}	External Supply Voltage[3]	Nonautomotive grade models[2]	1.75	1.8/3.3	3.6	V
V_{DDEXT}	External Supply Voltage	Automotive grade models[2]	2.7	3.3	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage	Nonautomotive grade models[2]	1.75	1.8/3.3	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage	Automotive grade models[2]	2.7	3.3	3.6	V
V_{IH}	High Level Input Voltage[4, 5]	V_{DDEXT} = 1.85 V	1.3			V
V_{IH}	High Level Input Voltage[4, 5]	V_{DDEXT} = Maximum	2.0			V
$V_{IHCLKIN}$	High Level Input Voltage[6]	V_{DDEXT} = Maximum	2.2			V
V_{IL}	Low Level Input Voltage[7]	V_{DDEXT} = 1.75 V			+0.3	V
V_{IL}	Low Level Input Voltage[7]	V_{DDEXT} = 2.7 V			+0.6	V
T_J	Junction Temperature	160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = 0°C to +70°C	0		+95	°C
T_J	Junction Temperature	160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C
T_J	Junction Temperature	169-Ball Plastic Ball Grid Array (PBGA) @ $T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C
T_J	Junction Temperature	169-Ball Plastic Ball Grid Array (PBGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	176-Lead Quad Flatpack (LQFP) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+100	°C

[1] The regulator can generate V_{DDINT} at levels of 0.85 V to 1.2 V with –5% to +10% tolerance, 1.25 V with –4% to +10% tolerance, and 1.3 V with –0% to +10% tolerance.

[2] See Ordering Guide on Page 63.

[3] When V_{DDEXT} < 2.25 V, on-chip voltage regulation is not supported.

[4] Applies to all input and bidirectional pins except CLKIN.

[5] The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are 3.3 V tolerant (always accepts up to 3.6 V maximum V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}, because V_{OH} (maximum) approximately equals V_{DDEXT} (maximum). This 3.3 V tolerance applies to bidirectional pins (DATA15–0, TMR2–0, PF15–0, PPI3–0, RSCLK1–0, TSCLK1–0, RFS1–0, TFS1–0, MOSI, MISO, SCK) and input only pins ($\overline{BR}$, ARDY, PPI_CLK, DR0PRI, DR0SEC, DR1PRI, DR1SEC, RX, RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, NMI, and BMODE1–0).

[6] Applies to CLKIN pin only.

[7] Applies to all input and bidirectional pins.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	400 MHz[1] Min	400 MHz[1] Typical	400 MHz[1] Max	500 MHz/533 MHz/600 MHz[2] Min	500 MHz/533 MHz/600 MHz[2] Typical	500 MHz/533 MHz/600 MHz[2] Max	Unit
V_{OH}	High Level Output Voltage[3]	V_{DDEXT} = 1.75 V, I_{OH} = –0.5 mA V_{DDEXT} = 2.25 V, I_{OH} = –0.5 mA V_{DDEXT} = 3.0 V, I_{OH} = –0.5 mA	1.5 1.9 2.4			1.5 1.9 2.4			V V V
V_{OL}	Low Level Output Voltage[3]	V_{DDEXT} = 1.75 V, I_{OL} = 2.0 mA V_{DDEXT} = 2.25 V/3.0 V, I_{OL} = 2.0 mA			0.2 0.4			0.2 0.4	V V
I_{IH}	High Level Input Current[4]	V_{DDEXT} = Max, V_{IN} = V_{DD} Max			10.0			10.0	µA
I_{IHP}	High Level Input Current JTAG[5]	V_{DDEXT} = Max, V_{IN} = V_{DD} Max			50.0			50.0	µA
I_{IL}[6]	Low Level Input Current[4]	V_{DDEXT} = Max, V_{IN} = 0 V			10.0			10.0	µA
I_{OZH}	Three-State Leakage Current[7]	V_{DDEXT} = Max, V_{IN} = V_{DD} Max			10.0			10.0	µA
I_{OZL}[6]	Three-State Leakage Current[7]	V_{DDEXT} = Max, V_{IN} = 0 V			10.0			10.0	µA
C_{IN}	Input Capacitance[8]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		4	8[9]		4	8[9]	pF
$I_{DDDEEPSLEEP}$[10]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.0 V, f_{CCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		7.5			32.5		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 0.8 V, T_J = 25°C, SCLK = 25 MHz			10			37.5	mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.14 V, f_{CCLK} = 400 MHz, T_J = 25°C		125			152		mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.2 V, f_{CCLK} = 500 MHz, T_J = 25°C					190		mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.2 V, f_{CCLK} = 533 MHz, T_J = 25°C					200		mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.3 V, f_{CCLK} = 600 MHz, T_J = 25°C					245		mA
$I_{DDHIBERNATE}$[10]	V_{DDEXT} Current in Hibernate State	V_{DDEXT} = 3.6 V, CLKIN = 0 MHz, T_J = Max, voltage regulator off (V_{DDINT} = 0 V)		50	100		50	100	µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J = 25°C		20			20		µA
$I_{DDDEEPSLEEP}$[10]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz		6	Table 15		16	Table 14	mA
I_{DD-INT}	V_{DDINT} Current	f_{CCLK} > 0 MHz			$I_{DDDEEPSLEEP}$ + (Table 17 × ASF)			$I_{DDDEEPSLEEP}$ + (Table 17 × ASF)	mA

[1] Applies to all 400 MHz speed grade models. See Ordering Guide on Page 63.
[2] Applies to all 500 MHz, 533 MHz, and 600 MHz speed grade models. See Ordering Guide on Page 63.
[3] Applies to output and bidirectional pins.
[4] Applies to input pins except JTAG inputs.

PACKAGE INFORMATION

The information presented in Figure 10 and Table 20 provides details about the package branding for the Blackfin processors. For a complete listing of product availability, see the Ordering Guide on Page 63.

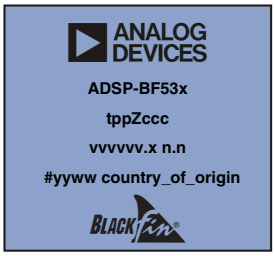


Figure 10. Product Information on Package

Table 20. Package Brand Information[1]

Brand Key	Field Description
ADSP-BF53x	Either ADSP-BF531, ADSP-BF532, or ADSP-BF533
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

[1] Non Automotive only. For branding information specific to Automotive products, contact Analog Devices Inc.

TIMING SPECIFICATIONS

Clock and Reset Timing

Table 21 and Figure 11 describe clock and reset operations. Per Absolute Maximum Ratings on Page 25, combinations of CLKIN and clock multipliers/divisors must not result in core/system clocks exceeding the maximum limits allowed for the processor, including system clock restrictions related to supply voltage.

Table 21. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN Period[1, 2, 3, 4]	25.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse	10.0		ns
t_{CKINH}	CLKIN High Pulse	10.0		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[5]	11 × t_{CKIN}		ns
t_{NOBOOT}	$\overline{\text{RESET}}$ Deassertion to First External Access Delay[6]	3 × t_{CKIN}	5 × t_{CKIN}	ns

[1] Applies to PLL bypass mode and PLL non bypass mode.
[2] CLKIN frequency must not change on the fly.
[3] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 11 on Page 21 through Table 13 on Page 21. Since the default behavior of the PLL is to multiply the CLKIN frequency by 10, the 400 MHz speed grade parts cannot use the full CLKIN period range.
[4] If the DF bit in the PLL_CTL register is set, then the maximum t_{CKIN} period is 50 ns.
[5] Applies after power-up sequence is complete. See Table 22 and Figure 12 for power-up reset timing.
[6] Applies when processor is configured in No Boot Mode (BMODE1-0 = b#00).

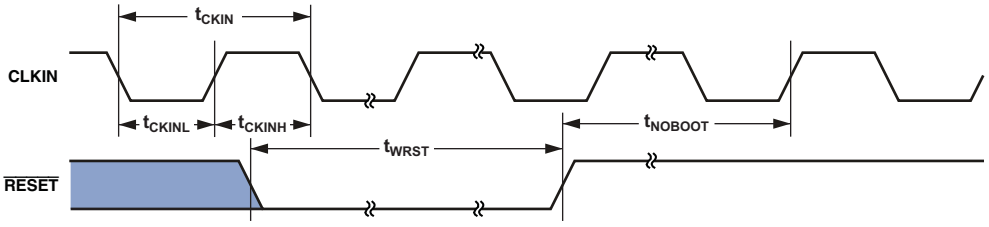
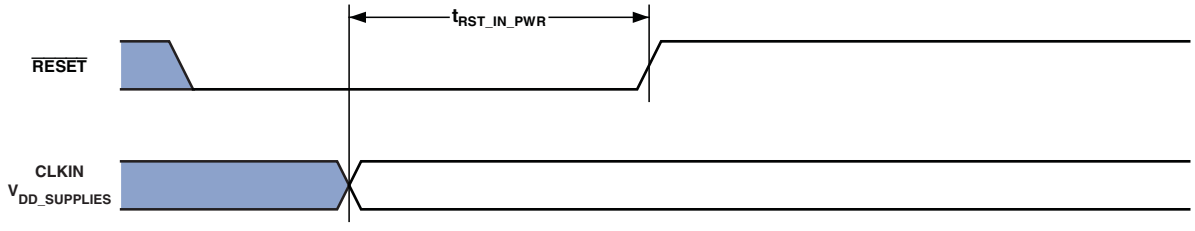


Figure 11. Clock and Reset Timing

Table 22. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted After the V_{DDINT}, V_{DDEXT}, V_{DDRTC}, and CLKIN Pins Are Stable and Within Specification	3500 × t_{CKIN}		ns



In Figure 12, $V_{DD\_SUPPLIES}$ is V_{DDINT}, V_{DDEXT}, V_{DDRTC}

Figure 12. Power-Up Reset Timing

Asynchronous Memory Read Cycle Timing

Table 23. Asynchronous Memory Read Cycle Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{SDAT}	DATA15–0 Setup Before CLKOUT	2.1		2.1		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	1.0		0.8		ns
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	1.0		0.0		ns
Switching Characteristics						
t_{DO}	Output Delay After CLKOUT[1]		6.0		6.0	ns
t_{HO}	Output Hold After CLKOUT [1]	1.0		0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, DATA15–0, $\overline{AOE}$, $\overline{ARE}$.

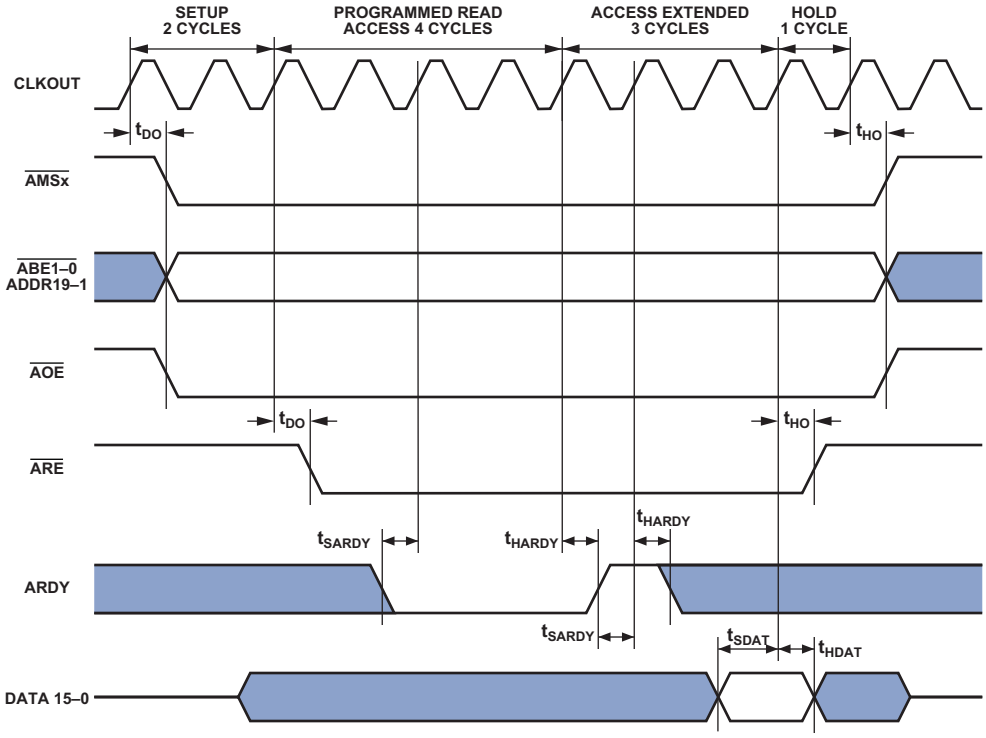


Figure 13. Asynchronous Memory Read Cycle Timing

Parallel Peripheral Interface Timing

Table 27 and Figure 17 through Figure 22 describe parallel peripheral interface operations.

Table 27. Parallel Peripheral Interface Timing

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Timing Requirements								
t_{PCLKW}	PPI_CLK Width	8.0		8.0		6.0		ns
t_{PCLK}	PPI_CLK Period[1]	20.0		20.0		15.0		ns
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK Edge (Nonsampling Edge for Rx, Sampling Edge for Tx)	6.0		6.0		4.0[2]		ns ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.0[2]		1.0[2]		1.0[2]		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	3.5		3.5		3.5		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	1.5		1.5		1.5		ns
Switching Characteristics—GP Output and Frame Capture Modes								
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		11.0		8.0		8.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	1.7		1.7		1.7		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		11.0		9.0		9.0	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	1.8		1.8		1.8		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$.
[2] Applies when PPI_CONTROL Bit 8 is cleared. See Figure 19 and Figure 22.

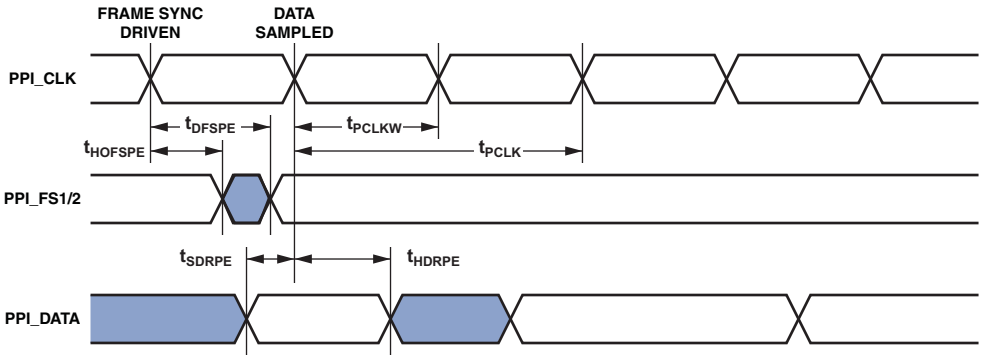


Figure 17. PPI GP Rx Mode with Internal Frame Sync Timing

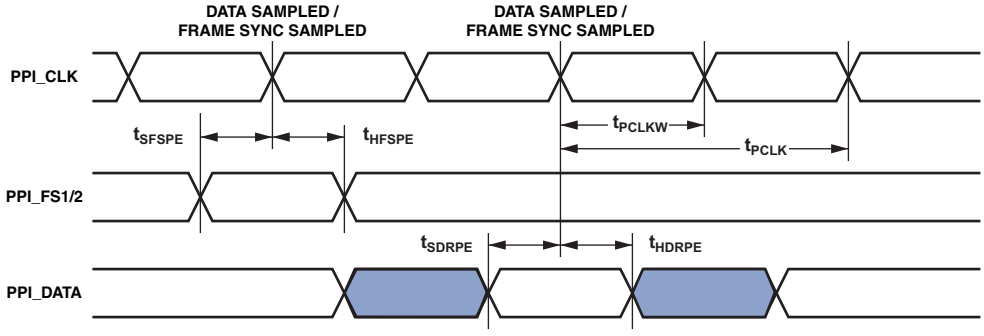


Figure 18. PPI GP Rx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 1)

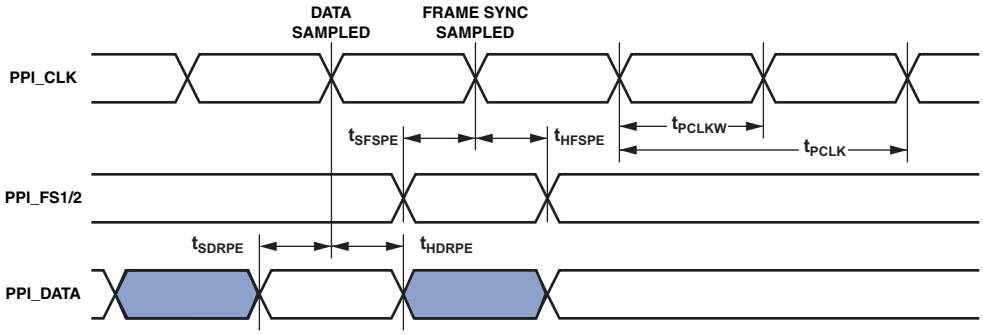


Figure 19. PPI GP Rx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 0)

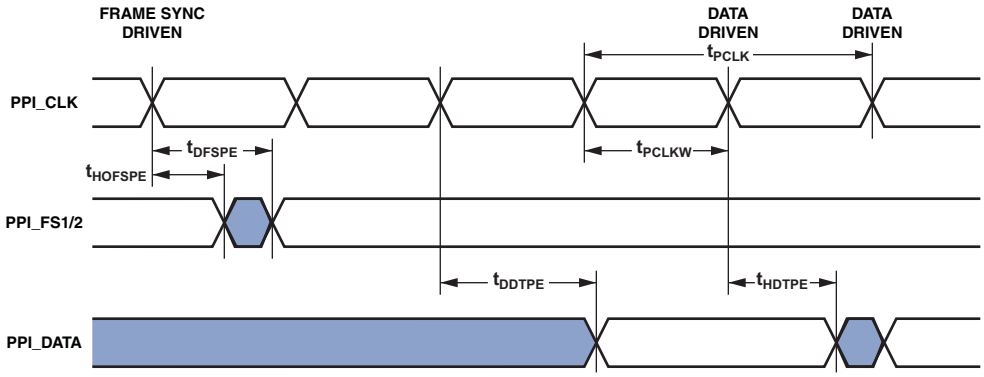


Figure 20. PPI GP Tx Mode with Internal Frame Sync Timing

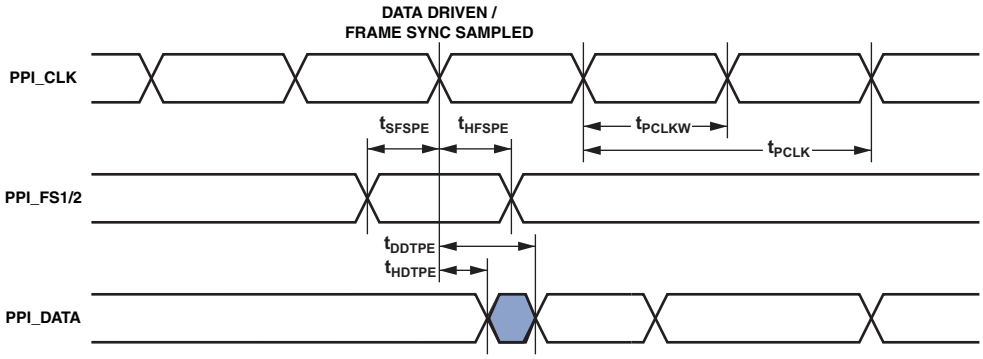


Figure 21. PPI GP Tx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 1)

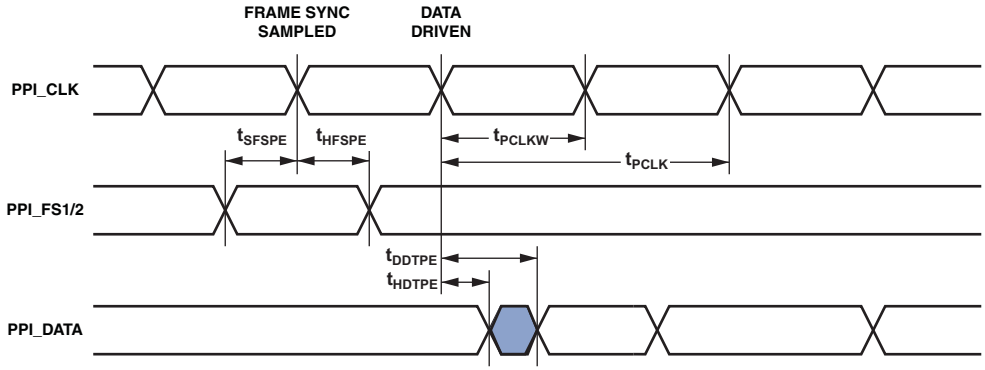


Figure 22. PPI GP Tx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 0)

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 33. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Timing Requirements								
t_{SPICHS}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK}$		$4 \times t_{SCLK}$		$4 \times t_{SCLK}$		ns
t_{HDS}	Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{SPISS}$ Assertion to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		1.6		1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	1.6		1.6		1.6		ns
Switching Characteristics								
t_{DSOE}	$\overline{SPISS}$ Assertion to Data Out Active	0	10	0	9	0	8	ns
t_{DSDHI}	$\overline{SPISS}$ Deassertion to Data High Impedance	0	10	0	9	0	8	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)		10		10		10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0		0		0		ns

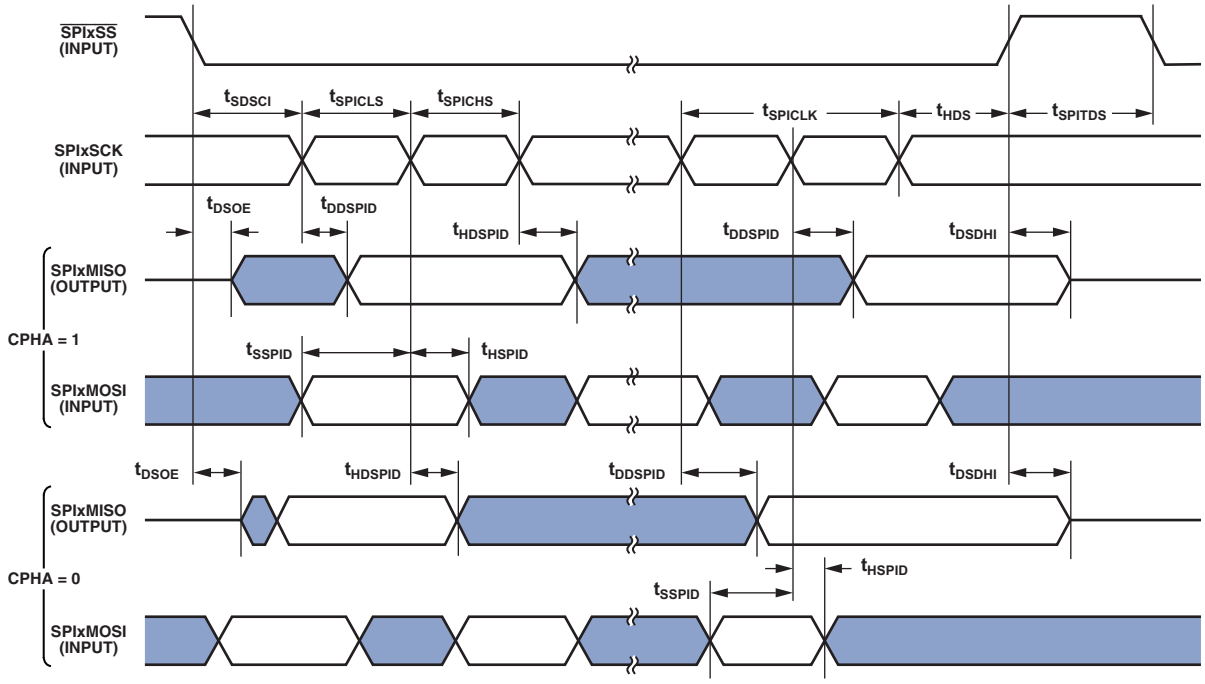


Figure 28. Serial Peripheral Interface (SPI) Port—Slave Timing

OUTPUT DRIVE CURRENTS

Figure 33 through Figure 44 show typical current-voltage characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

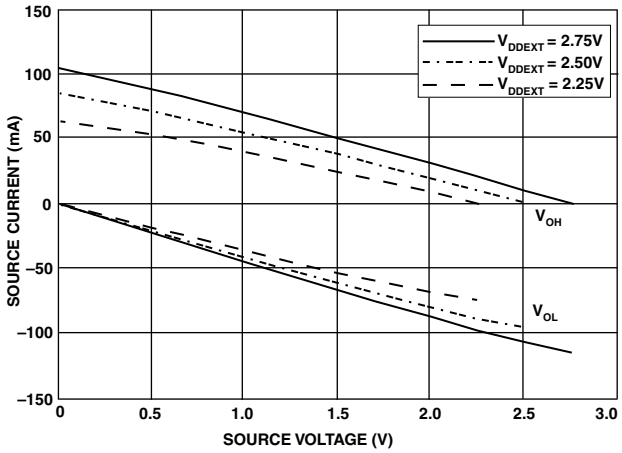


Figure 33. Drive Current A (V_{DDEXT} = 2.5 V)

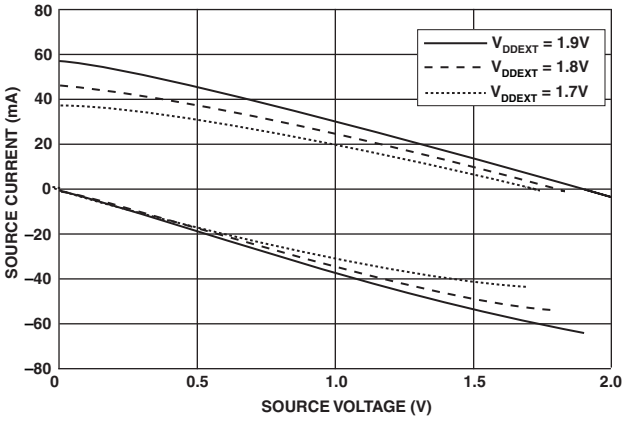


Figure 34. Drive Current A (V_{DDEXT} = 1.8 V)

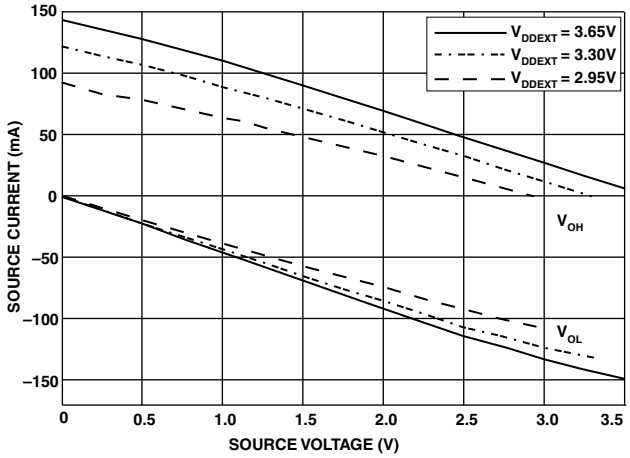


Figure 35. Drive Current A (V_{DDEXT} = 3.3 V)

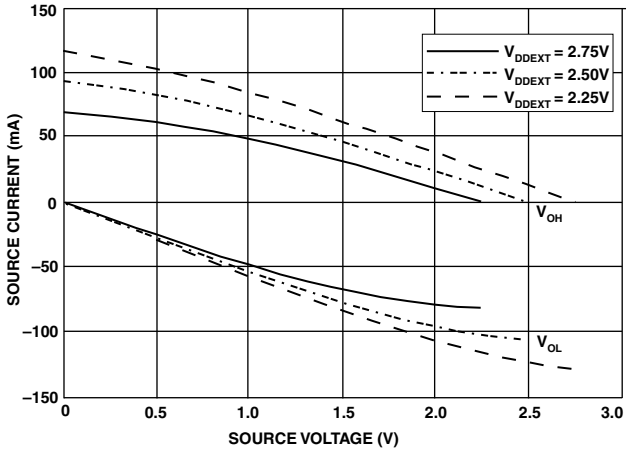


Figure 36. Drive Current B (V_{DDEXT} = 2.5 V)

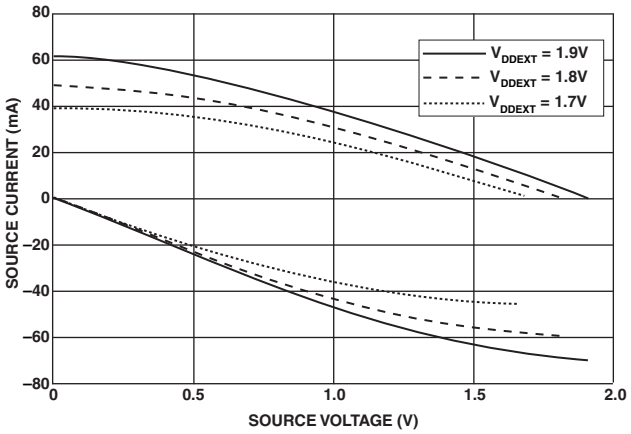


Figure 37. Drive Current B (V_{DDEXT} = 1.8 V)

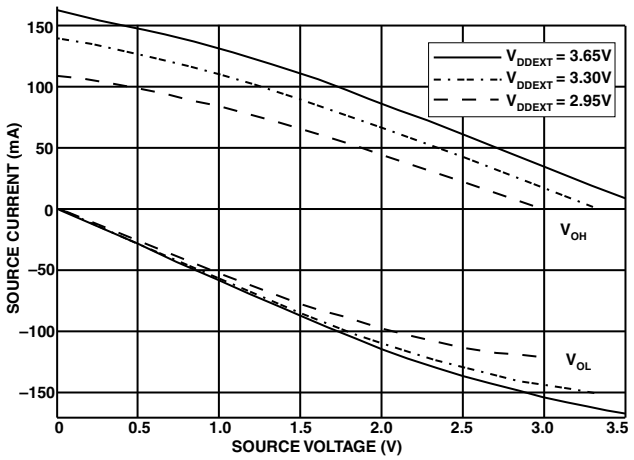


Figure 38. Drive Current B (V_{DDEXT} = 3.3 V)

160-BALL CSP_BGA BALL ASSIGNMENT

Table 41 lists the CSP_BGA ball assignment by signal. Table 42 on Page 51 lists the CSP_BGA ball assignment by ball number.

Table 41. 160-Ball CSP_BGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{ABE0}$	H13	DATA4	N8	GND	L6	SCK	D1
$\overline{ABE1}$	H12	DATA5	P8	GND	L8	SCKE	B13
ADDR1	J14	DATA6	M7	GND	L10	$\overline{SMS}$	C13
ADDR2	K14	DATA7	N7	GND	M4	$\overline{SRAS}$	D13
ADDR3	L14	DATA8	P7	GND	M10	$\overline{SWE}$	D12
ADDR4	J13	DATA9	M6	GND	P14	TCK	P2
ADDR5	K13	DATA10	N6	MISO	E2	TDI	M3
ADDR6	L13	DATA11	P6	MOSI	D3	TDO	N3
ADDR7	K12	DATA12	M5	NMI	B10	TFS0	H3
ADDR8	L12	DATA13	N5	PF0	D2	TFS1	E1
ADDR9	M12	DATA14	P5	PF1	C1	TMR0	L2
ADDR10	M13	DATA15	P4	PF2	C2	TMR1	M1
ADDR11	M14	DR0PRI	K1	PF3	C3	TMR2	K2
ADDR12	N14	DR0SEC	J2	PF4	B1	TMS	N2
ADDR13	N13	DR1PRI	G3	PF5	B2	$\overline{TRST}$	N1
ADDR14	N12	DR1SEC	F3	PF6	B3	TSCLK0	J1
ADDR15	M11	DT0PRI	H1	PF7	B4	TSCLK1	F1
ADDR16	N11	DT0SEC	H2	PF8	A2	TX	K3
ADDR17	P13	DT1PRI	F2	PF9	A3	V_{DDEXT}	A1
ADDR18	P12	DT1SEC	E3	PF10	A4	V_{DDEXT}	C7
ADDR19	P11	$\overline{EMU}$	M2	PF11	A5	V_{DDEXT}	C12
$\overline{AMS0}$	E14	GND	A10	PF12	B5	V_{DDEXT}	D5
$\overline{AMS1}$	F14	GND	A14	PF13	B6	V_{DDEXT}	D9
$\overline{AMS2}$	F13	GND	B11	PF14	A6	V_{DDEXT}	F12
$\overline{AMS3}$	G12	GND	C4	PF15	C6	V_{DDEXT}	G4
$\overline{AOE}$	G13	GND	C5	PPI_CLK	C9	V_{DDEXT}	J4
ARDY	E13	GND	C11	PPI0	C8	V_{DDEXT}	J12
$\overline{ARE}$	G14	GND	D4	PPI1	B8	V_{DDEXT}	L7
$\overline{AWE}$	H14	GND	D7	PPI2	A7	V_{DDEXT}	L11
$\overline{BG}$	P10	GND	D8	PPI3	B7	V_{DDEXT}	P1
$\overline{BGH}$	N10	GND	D10	$\overline{RESET}$	C10	V_{DDINT}	D6
BMODE0	N4	GND	D11	RFS0	J3	V_{DDINT}	E4
BMODE1	P3	GND	F4	RFS1	G2	V_{DDINT}	E11
$\overline{BR}$	D14	GND	F11	RSCLK0	L1	V_{DDINT}	J11
CLKIN	A12	GND	G11	RSCLK1	G1	V_{DDINT}	L4
CLKOUT	B14	GND	H4	RTXI	A9	V_{DDINT}	L9
DATA0	M9	GND	H11	RTXO	A8	V_{DDRTC}	B9
DATA1	N9	GND	K4	RX	L3	VROUT0	A13
DATA2	P9	GND	K11	SA10	E12	VROUT1	B12
DATA3	M8	GND	L5	$\overline{SCAS}$	C14	XTAL	A11

Table 42. 160-Ball CSP_BGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	V_{DDEXT}	C13	$\overline{SMS}$	H1	DT0PRI	M3	TDI
A2	PF8	C14	$\overline{SCAS}$	H2	DT0SEC	M4	GND
A3	PF9	D1	SCK	H3	TFS0	M5	DATA12
A4	PF10	D2	PF0	H4	GND	M6	DATA9
A5	PF11	D3	MOSI	H11	GND	M7	DATA6
A6	PF14	D4	GND	H12	$\overline{ABE1}$	M8	DATA3
A7	PPI2	D5	V_{DDEXT}	H13	$\overline{ABE0}$	M9	DATA0
A8	RTXO	D6	V_{DDINT}	H14	$\overline{AWE}$	M10	GND
A9	RTXI	D7	GND	J1	TSCLK0	M11	ADDR15
A10	GND	D8	GND	J2	DR0SEC	M12	ADDR9
A11	XTAL	D9	V_{DDEXT}	J3	RFS0	M13	ADDR10
A12	CLKIN	D10	GND	J4	V_{DDEXT}	M14	ADDR11
A13	VROUT0	D11	GND	J11	V_{DDINT}	N1	$\overline{TRST}$
A14	GND	D12	$\overline{SWE}$	J12	V_{DDEXT}	N2	TMS
B1	PF4	D13	$\overline{SRAS}$	J13	ADDR4	N3	TDO
B2	PF5	D14	$\overline{BR}$	J14	ADDR1	N4	BMODE0
B3	PF6	E1	TFS1	K1	DR0PRI	N5	DATA13
B4	PF7	E2	MISO	K2	TMR2	N6	DATA10
B5	PF12	E3	DT1SEC	K3	TX	N7	DATA7
B6	PF13	E4	V_{DDINT}	K4	GND	N8	DATA4
B7	PPI3	E11	V_{DDINT}	K11	GND	N9	DATA1
B8	PPI1	E12	SA10	K12	ADDR7	N10	$\overline{BGH}$
B9	V_{DDRTC}	E13	ARDY	K13	ADDR5	N11	ADDR16
B10	NMI	E14	$\overline{AMS0}$	K14	ADDR2	N12	ADDR14
B11	GND	F1	TSCLK1	L1	RSCLK0	N13	ADDR13
B12	VROUT1	F2	DT1PRI	L2	TMR0	N14	ADDR12
B13	SCKE	F3	DR1SEC	L3	RX	P1	V_{DDEXT}
B14	CLKOUT	F4	GND	L4	V_{DDINT}	P2	TCK
C1	PF1	F11	GND	L5	GND	P3	BMODE1
C2	PF2	F12	V_{DDEXT}	L6	GND	P4	DATA15
C3	PF3	F13	$\overline{AMS2}$	L7	V_{DDEXT}	P5	DATA14
C4	GND	F14	$\overline{AMS1}$	L8	GND	P6	DATA11
C5	GND	G1	RSCLK1	L9	V_{DDINT}	P7	DATA8
C6	PF15	G2	RFS1	L10	GND	P8	DATA5
C7	V_{DDEXT}	G3	DR1PRI	L11	V_{DDEXT}	P9	DATA2
C8	PPI0	G4	V_{DDEXT}	L12	ADDR8	P10	$\overline{BG}$
C9	PPI_CLK	G11	GND	L13	ADDR6	P11	ADDR19
C10	$\overline{RESET}$	G12	$\overline{AMS3}$	L14	ADDR3	P12	ADDR18
C11	GND	G13	$\overline{AOE}$	M1	TMR1	P13	ADDR17
C12	V_{DDEXT}	G14	$\overline{ARE}$	M2	$\overline{EMU}$	P14	GND

169-BALL PBGA BALL ASSIGNMENT

Table 43 lists the PBGA ball assignment by signal. Table 44 on Page 54 lists the PBGA ball assignment by ball number.

Table 43. 169-Ball PBGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{ABE0}$	H16	DATA4	U12	GND	K9	RTXI	A10	V_{DDEXT}	K6
$\overline{ABE1}$	H17	DATA5	U11	GND	K10	RTXO	A11	V_{DDEXT}	L6
ADDR1	J16	DATA6	T10	GND	K11	RX	T1	V_{DDEXT}	M6
ADDR2	J17	DATA7	U10	GND	L7	SA10	B15	V_{DDEXT}	M7
ADDR3	K16	DATA8	T9	GND	L8	$\overline{SCAS}$	A16	V_{DDEXT}	M8
ADDR4	K17	DATA9	U9	GND	L9	SCK	D1	V_{DDEXT}	T2
ADDR5	L16	DATA10	T8	GND	L10	SCKE	B14	VROUT0	B12
ADDR6	L17	DATA11	U8	GND	L11	$\overline{SMS}$	A17	VROUT1	B13
ADDR7	M16	DATA12	U7	GND	M9	$\overline{SRAS}$	A15	XTAL	A13
ADDR8	M17	DATA13	T7	GND	T16	$\overline{SWE}$	B17		
ADDR9	N17	DATA14	U6	MISO	E2	TCK	U4		
ADDR10	N16	DATA15	T6	MOSI	E1	TDI	U3		
ADDR11	P17	DR0PRI	M2	NMI	B11	TDO	T4		
ADDR12	P16	DR0SEC	M1	PF0	D2	TFS0	L1		
ADDR13	R17	DR1PRI	H1	PF1	C1	TFS1	G2		
ADDR14	R16	DR1SEC	H2	PF2	B1	TMR0	R1		
ADDR15	T17	DT0PRI	K2	PF3	C2	TMR1	P2		
ADDR16	U15	DT0SEC	K1	PF4	A1	TMR2	P1		
ADDR17	T15	DT1PRI	F1	PF5	A2	TMS	T3		
ADDR18	U16	DT1SEC	F2	PF6	B3	$\overline{TRST}$	U2		
ADDR19	T14	$\overline{EMU}$	U1	PF7	A3	TSCLK0	L2		
$\overline{AMS0}$	D17	GND	B16	PF8	B4	TSCLK1	G1		
$\overline{AMS1}$	E16	GND	F11	PF9	A4	TX	R2		
$\overline{AMS2}$	E17	GND	G7	PF10	B5	VDD	F12		
$\overline{AMS3}$	F16	GND	G8	PF11	A5	VDD	G12		
$\overline{AOE}$	F17	GND	G9	PF12	A6	VDD	H12		
ARDY	C16	GND	G10	PF13	B6	VDD	J12		
$\overline{ARE}$	G16	GND	G11	PF14	A7	VDD	K12		
$\overline{AWE}$	G17	GND	H7	PF15	B7	VDD	L12		
$\overline{BG}$	T13	GND	H8	PPI_CLK	B10	VDD	M10		
$\overline{BGH}$	U17	GND	H9	PPI0	B9	VDD	M11		
BMODE0	U5	GND	H10	PPI1	A9	VDD	M12		
BMODE1	T5	GND	H11	PPI2	B8	V_{DDEXT}	B2		
$\overline{BR}$	C17	GND	J7	PPI3	A8	V_{DDEXT}	F6		
CLKIN	A14	GND	J8	$\overline{RESET}$	A12	V_{DDEXT}	F7		
CLKOUT	D16	GND	J9	RFS0	N1	V_{DDEXT}	F8		
DATA0	U14	GND	J10	RFS1	J1	V_{DDEXT}	F9		
DATA1	T12	GND	J11	RSCLK0	N2	V_{DDEXT}	G6		
DATA2	U13	GND	K7	RSCLK1	J2	V_{DDEXT}	H6		
DATA3	T11	GND	K8	RTCVDD	F10	V_{DDEXT}	J6		

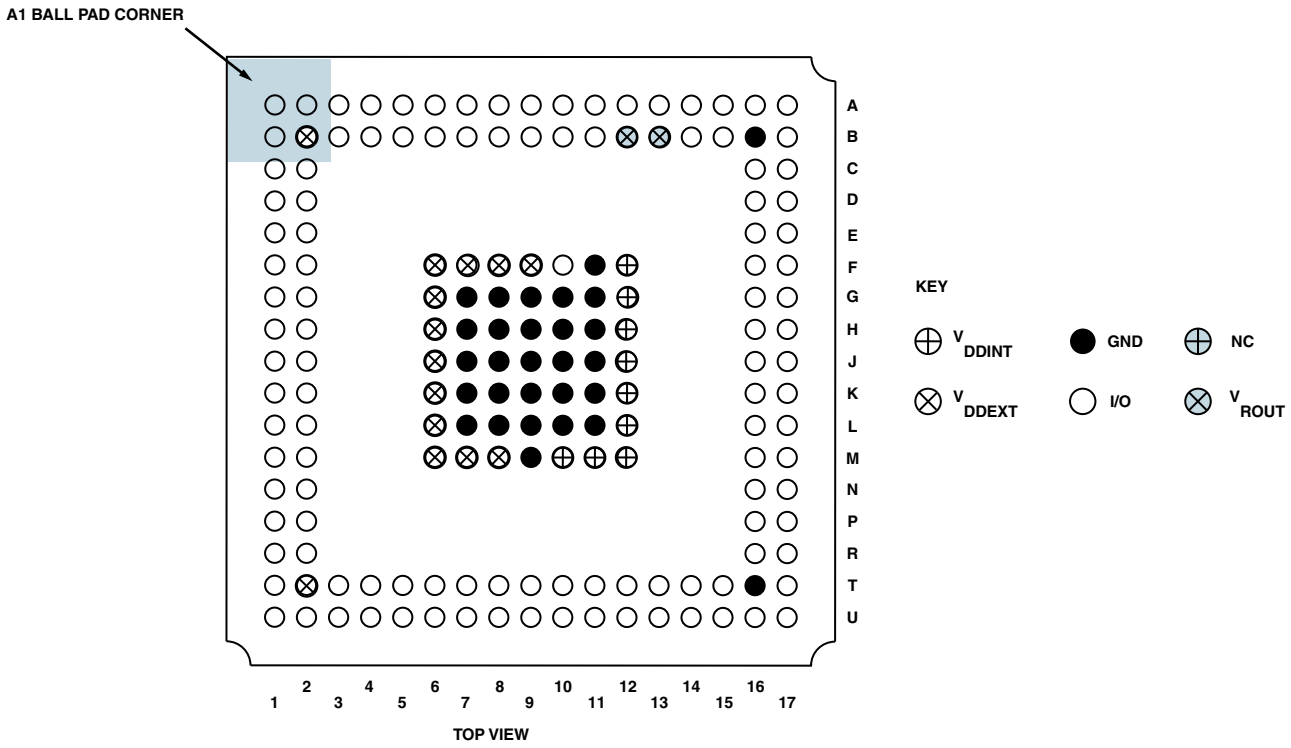


Figure 62. 169-Ball PBGA Ground Configuration (Top View)

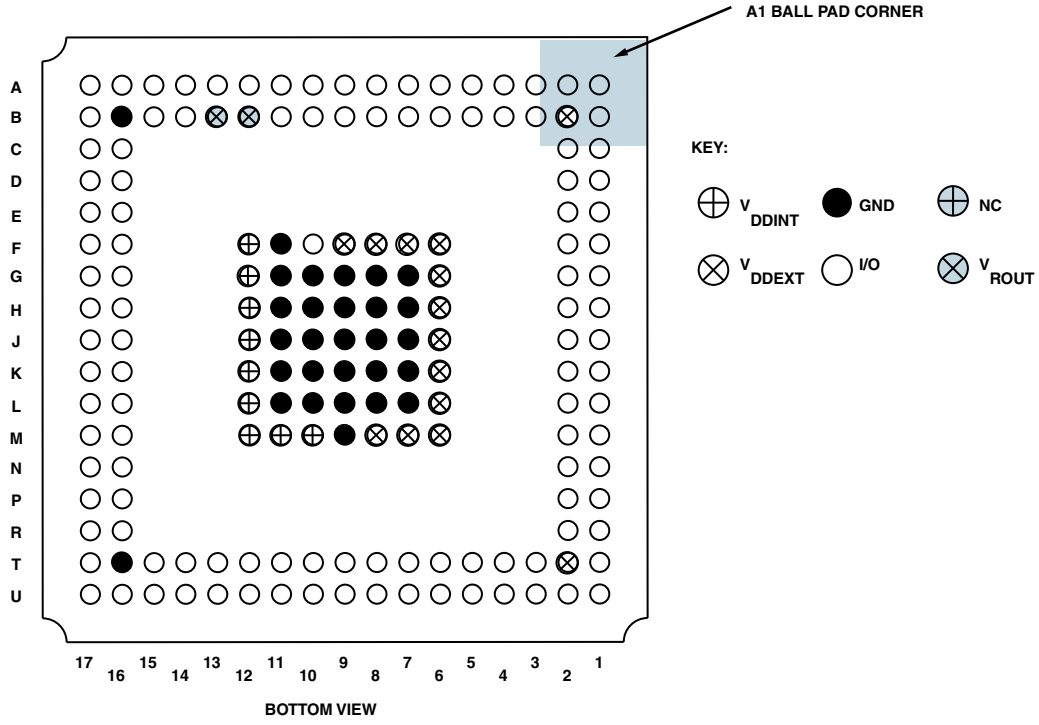


Figure 63. 169-Ball PBGA Ground Configuration (Bottom View)

SURFACE-MOUNT DESIGN

Table 47 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 47. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
Chip Scale Package Ball Grid Array (CSP_BGA) BC-160-2	Solder Mask Defined	0.40 mm diameter	0.55 mm diameter
Plastic Ball Grid Array (PBGA) B-169	Solder Mask Defined	0.43 mm diameter	0.56 mm diameter

ORDERING GUIDE

Model [1]	Temperature Range [2]	Speed Grade (Max)	Package Description	Package Option
ADSP-BF531SBB400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF531SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF531SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF531SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF531SBBCZ4RL	–40°C to +85°C	400 MHz	160-Ball CSP_BGA, 13" Tape and Reel	BC-160-2
ADSP-BF531SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF532SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF532SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF532SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF532SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF533SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF533SBB500	–40°C to +85°C	500 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBZ500	–40°C to +85°C	500 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBC500	–40°C to +85°C	500 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ500	–40°C to +85°C	500 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBC-5V	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ-5V	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKBC-6V	0°C to +70°C	600 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKBCZ-6V	0°C to +70°C	600 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKSTZ-5V	0°C to +70°C	533 MHz	176-Lead LQFP	ST-176-1

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 20 for junction temperature (T_J) specification which is the only temperature specification.