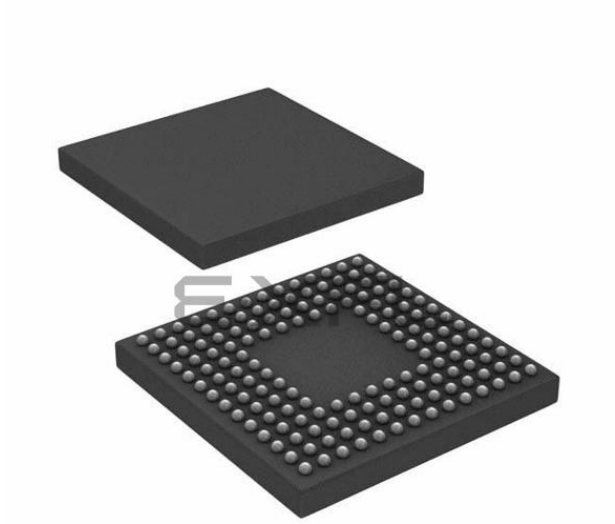

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	400MHz
Non-Volatile Memory	ROM (1kB)
On-Chip RAM	148kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LFBGA, CSPBGA
Supplier Device Package	160-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf533sbbc400

- CEC interrupt pending register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but can be read while in supervisor mode.

The SIC allows further control of event processing by providing three 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in Table 3.

- SIC interrupt mask register (SIC_IMASK) – This register controls the masking and unmasking of each peripheral interrupt event. When a bit is set in this register, that peripheral event is unmasked and is processed by the system when asserted. A cleared bit in this register masks the peripheral event, preventing the processor from servicing the event.
- SIC interrupt status register (SIC_ISR) – As multiple peripherals can be mapped to a single event, this register allows the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt, and a cleared bit indicates the peripheral is not asserting the event.
- SIC interrupt wakeup enable register (SIC_IWR) – By enabling the corresponding bit in this register, a peripheral can be configured to wake up the processor, should the core be idled when the event is generated. See Dynamic Power Management on Page 11.

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC recognizes and queues the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

DMA CONTROLLERS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have multiple, independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the SPORTs, SPI port, UART, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The DMA controller supports both 1-dimensional (1-D) and 2-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, autorefreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two pairs of memory DMA channels provided for transfers between the various memories of the processor system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

REAL-TIME CLOCK

The processor real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors. The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

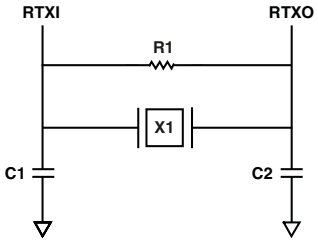
The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60 second counter, a 60 minute counter, a 24 hour counter, and a 32,768 day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. The two alarms are time of day and a day and time of that day.

The stopwatch function counts down from a programmed value, with one second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like other peripherals, the RTC can wake up the processor from sleep mode upon generation of any RTC wakeup event. Additionally, an RTC wakeup event can wake up the processor from deep sleep mode, and wake up the on-chip internal voltage regulator from a powered-down state.

Connect RTC pins RTXI and RTXO with external components as shown in Figure 6.



SUGGESTED COMPONENTS:
X1 = ECLIPTEK EC38J (THROUGH-HOLE PACKAGE) OR
EPSON MC405 12 pF LOAD (SURFACE-MOUNT PACKAGE)
C1 = 22 pF
C2 = 22 pF
R1 = 10 MΩ

NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

Figure 6. External Components for RTC

WATCHDOG TIMER

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors include a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK), at a maximum frequency of f_{SCLK}.

TIMERS

There are four general-purpose programmable timer units in the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors. Three timers have an external pin that can be configured either as a pulse-width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the PF1 pin (TACLK), an external clock input to the PPI_CLK pin (TMRCLK), or to the internal SCLK.

The timer units can be used in conjunction with the UART to measure the width of the pulses in the data stream to provide an autobaud detect function for a serial channel.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the three general-purpose programmable timers, a fourth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

SERIAL PORTS (SPORTs)

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- I^2S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I^2S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131,070) Hz to (f_{SCLK}/2) Hz.
- Word length – Each SPORT supports serial data words from 3 bits to 32 bits in length, transferred most-significant-bit first or least-significant-bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.

PFx pins defined as inputs can be configured to generate hardware interrupts, while output PFx pins can be triggered by software interrupts.

- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual PFx pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

PARALLEL PERIPHERAL INTERFACE

The processors provide a parallel peripheral interface (PPI) that can connect directly to parallel ADCs and DACs, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bi-directional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bi-directional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications.

Three distinct sub modes are supported:

- Input mode – Frame syncs and data are inputs into the PPI.
- Frame capture mode – Frame syncs are outputs from the PPI, but data are inputs.
- Output mode – Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (e.g., for frame capture). The processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct sub modes are supported:

- Active video only mode
- Vertical blanking only mode
- Entire field mode

Active Video Only Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that can be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

DYNAMIC POWER MANAGEMENT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provides four operating modes, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

As shown in Figure 9, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a user programmable 0.5× to 64× multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 10×, but it can be modified by a software instruction sequence. On-the-fly frequency changes can be effected by simply writing to the PLL_DIV register.

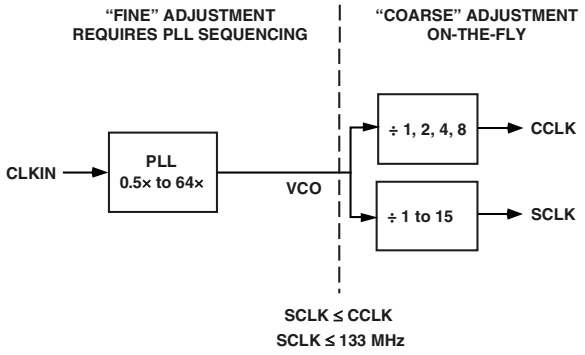


Figure 9. Frequency Modification Methods

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 6 illustrates typical system clock ratios.

Table 6. Example System Clock Ratios

Signal Name SSEL3–0	Divider Ratio VCO/SCLK	Example Frequency Ratios (MHz)	
		VCO	SCLK
0001	1:1	100	100
0101	5:1	400	80
1010	10:1	500	50

The maximum frequency of the system clock is f_{SCLK}. The divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV). When the SSEL value is changed, it affects all of the peripherals that derive their clock signals from the SCLK signal.

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 7. This programmable core clock capability is useful for fast core frequency modifications.

Table 7. Core Clock Ratios

Signal Name CSEL1–0	Divider Ratio VCO/CCLK	Example Frequency Ratios (MHz)	
		VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	400	100
11	8:1	200	25

BOOTING MODES

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have two mechanisms (listed in Table 8) for automatically loading internal L1 instruction memory after a reset. A third mode is provided to execute from external memory, bypassing the boot sequence.

Table 8. Booting Modes

BMODE1–0	Description
00	Execute from 16-bit external memory (bypass boot ROM)
01	Boot from 8-bit or 16-bit FLASH
10	Boot from serial master connected to SPI
11	Boot from serial slave EEPROM/flash (8-,16-, or 24-bit address range, or Atmel AT45DB041, AT45DB081, or AT45DB161serial flash)

The BMODE pins of the reset configuration register, sampled during power-on resets and software-initiated resets, implement the following modes:

- Execute from 16-bit external memory – Execution starts from address 0x2000 0000 with 16-bit packing. The boot ROM is bypassed in this mode. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).
- Boot from 8-bit or 16-bit external flash memory – The flash boot routine located in boot ROM memory space is set up using asynchronous Memory Bank 0. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).
- Boot from SPI serial EEPROM/flash (8-, 16-, or 24-bit addressable, or Atmel AT45DB041, AT45DB081, or AT45DB161) – The SPI uses the PF2 output pin to select a single SPI EEPROM/flash device, submits a read command and successive address bytes (0x00) until a valid 8-, 16-, or 24-bit addressable EEPROM/flash device is detected, and begins clocking data into the processor at the beginning of L1 instruction memory.
- Boot from SPI serial master – The Blackfin processor operates in SPI slave mode and is configured to receive the bytes of the LDR file from an SPI host (master) agent. To hold off the host device from transmitting while the boot ROM is busy, the Blackfin processor asserts a GPIO pin, called host wait (HWAIT), to signal the host device not to send any

more bytes until the flag is deasserted. The GPIO pin is chosen by the user and this information is transferred to the Blackfin processor via bits[10:5] of the FLAG header in the LDR image.

For each of the boot modes, a 10-byte header is first read from an external memory device. The header specifies the number of bytes to be transferred and the memory destination address. Multiple memory blocks can be loaded by any boot sequence. Once all blocks are loaded, program execution commences from the start of L1 instruction SRAM.

In addition, Bit 4 of the reset configuration register can be set by application code to bypass the normal boot sequence during a software reset. For this case, the processor jumps directly to the beginning of L1 instruction memory.

INSTRUCTION SET DESCRIPTION

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both user (algorithm/application code) and supervisor (O/S kernel, device drivers, debuggers, ISRs) modes of operation, allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/CPU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU + two load/store + two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4G byte memory space, providing a simplified programming model.
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data types; and separate user and supervisor stack pointers.
- Code density enhancements, which include intermixing of 16-bit and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded in 16 bits.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	400 MHz[1] Min	400 MHz[1] Typical	400 MHz[1] Max	500 MHz/533 MHz/600 MHz[2] Min	500 MHz/533 MHz/600 MHz[2] Typical	500 MHz/533 MHz/600 MHz[2] Max	Unit
V_{OH}	High Level Output Voltage[3]	V_{DDEXT} = 1.75 V, I_{OH} = –0.5 mA V_{DDEXT} = 2.25 V, I_{OH} = –0.5 mA V_{DDEXT} = 3.0 V, I_{OH} = –0.5 mA	1.5 1.9 2.4			1.5 1.9 2.4			V V V
V_{OL}	Low Level Output Voltage[3]	V_{DDEXT} = 1.75 V, I_{OL} = 2.0 mA V_{DDEXT} = 2.25 V/3.0 V, I_{OL} = 2.0 mA			0.2 0.4			0.2 0.4	V V
I_{IH}	High Level Input Current[4]	V_{DDEXT} = Max, V_{IN} = V_{DD} Max			10.0			10.0	µA
I_{IHP}	High Level Input Current JTAG[5]	V_{DDEXT} = Max, V_{IN} = V_{DD} Max			50.0			50.0	µA
I_{IL}[6]	Low Level Input Current[4]	V_{DDEXT} = Max, V_{IN} = 0 V			10.0			10.0	µA
I_{OZH}	Three-State Leakage Current[7]	V_{DDEXT} = Max, V_{IN} = V_{DD} Max			10.0			10.0	µA
I_{OZL}[6]	Three-State Leakage Current[7]	V_{DDEXT} = Max, V_{IN} = 0 V			10.0			10.0	µA
C_{IN}	Input Capacitance[8]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		4	8[9]		4	8[9]	pF
$I_{DDDEEPSLEEP}$[10]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.0 V, f_{CCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		7.5			32.5		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 0.8 V, T_J = 25°C, SCLK = 25 MHz			10			37.5	mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.14 V, f_{CCLK} = 400 MHz, T_J = 25°C		125			152		mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.2 V, f_{CCLK} = 500 MHz, T_J = 25°C					190		mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.2 V, f_{CCLK} = 533 MHz, T_J = 25°C					200		mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.3 V, f_{CCLK} = 600 MHz, T_J = 25°C					245		mA
$I_{DDHIBERNATE}$[10]	V_{DDEXT} Current in Hibernate State	V_{DDEXT} = 3.6 V, CLKIN = 0 MHz, T_J = Max, voltage regulator off (V_{DDINT} = 0 V)		50	100		50	100	µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J = 25°C		20			20		µA
$I_{DDDEEPSLEEP}$[10]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz		6	Table 15		16	Table 14	mA
I_{DD-INT}	V_{DDINT} Current	f_{CCLK} > 0 MHz			$I_{DDDEEPSLEEP}$ + (Table 17 × ASF)			$I_{DDDEEPSLEEP}$ + (Table 17 × ASF)	mA

[1] Applies to all 400 MHz speed grade models. See Ordering Guide on Page 63.
[2] Applies to all 500 MHz, 533 MHz, and 600 MHz speed grade models. See Ordering Guide on Page 63.
[3] Applies to output and bidirectional pins.
[4] Applies to input pins except JTAG inputs.

PACKAGE INFORMATION

The information presented in Figure 10 and Table 20 provides details about the package branding for the Blackfin processors. For a complete listing of product availability, see the Ordering Guide on Page 63.

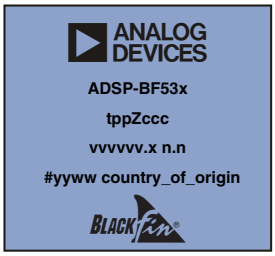


Figure 10. Product Information on Package

Table 20. Package Brand Information[1]

Brand Key	Field Description
ADSP-BF53x	Either ADSP-BF531, ADSP-BF532, or ADSP-BF533
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

[1] Non Automotive only. For branding information specific to Automotive products, contact Analog Devices Inc.

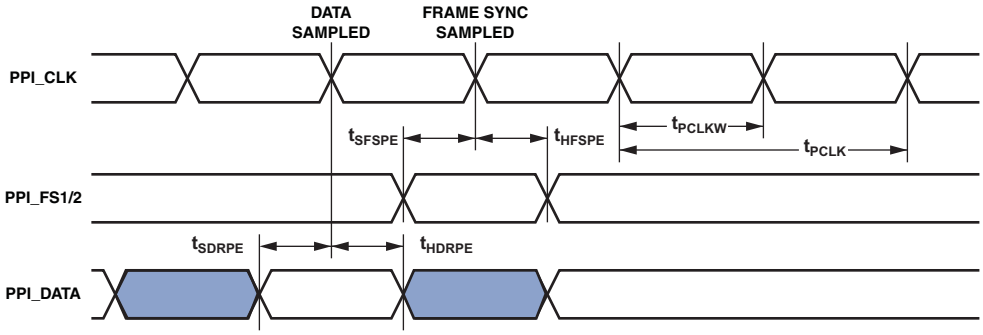


Figure 19. PPI GP Rx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 0)

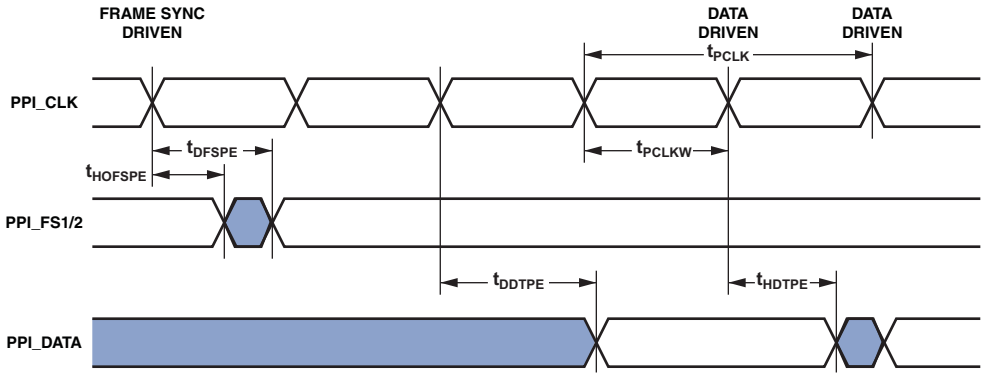


Figure 20. PPI GP Tx Mode with Internal Frame Sync Timing

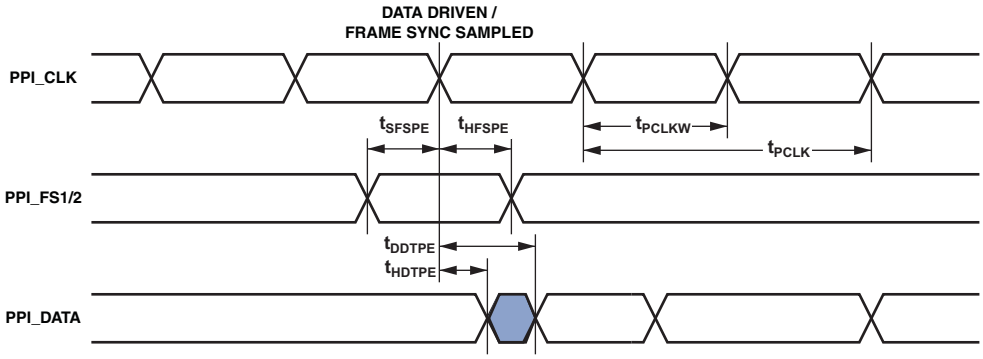


Figure 21. PPI GP Tx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 1)

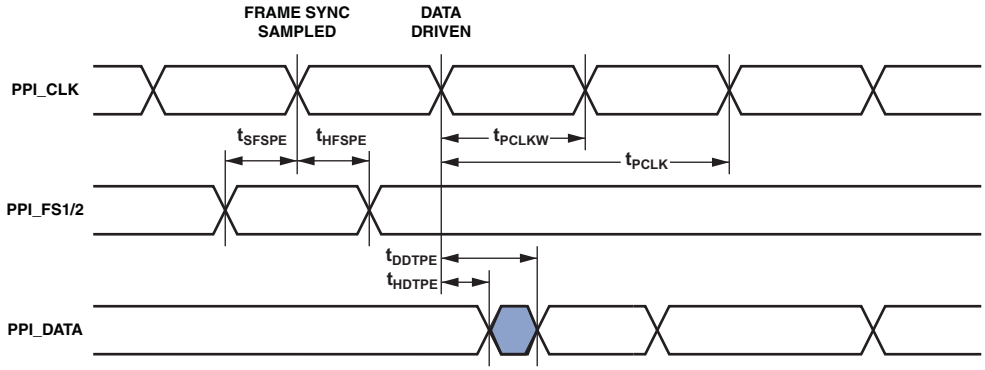


Figure 22. PPI GP Tx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 0)

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 33. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Timing Requirements								
t_{SPICHS}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK}$		$4 \times t_{SCLK}$		$4 \times t_{SCLK}$		ns
t_{HDS}	Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{SPISS}$ Assertion to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		1.6		1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	1.6		1.6		1.6		ns
Switching Characteristics								
t_{DSOE}	$\overline{SPISS}$ Assertion to Data Out Active	0	10	0	9	0	8	ns
t_{DSDHI}	$\overline{SPISS}$ Deassertion to Data High Impedance	0	10	0	9	0	8	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)		10		10		10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0		0		0		ns

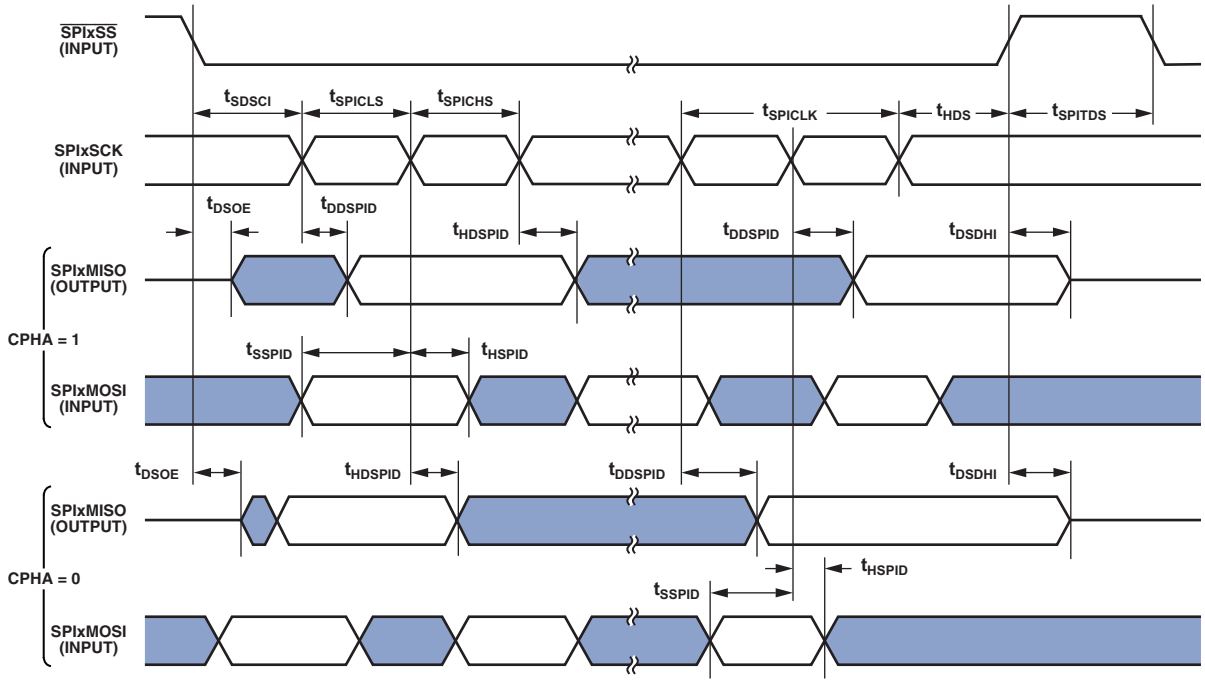


Figure 28. Serial Peripheral Interface (SPI) Port—Slave Timing

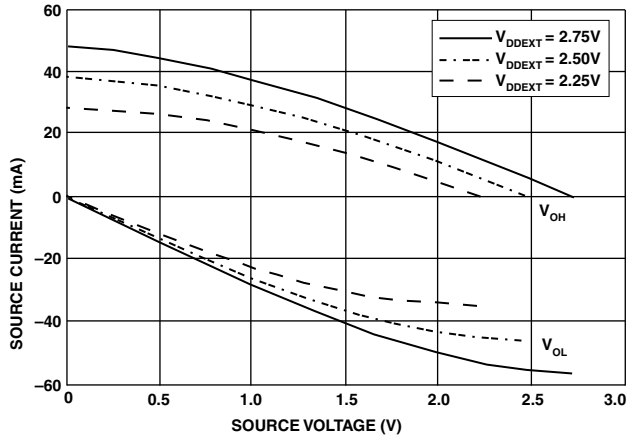


Figure 39. Drive Current C (V_{DDEXT} = 2.5 V)

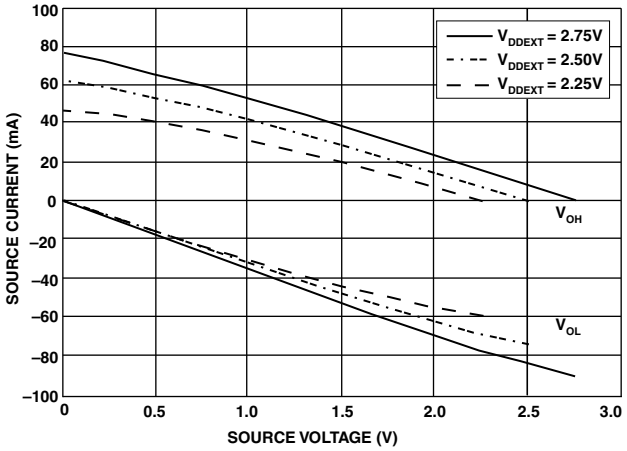


Figure 42. Drive Current D (V_{DDEXT} = 2.5 V)

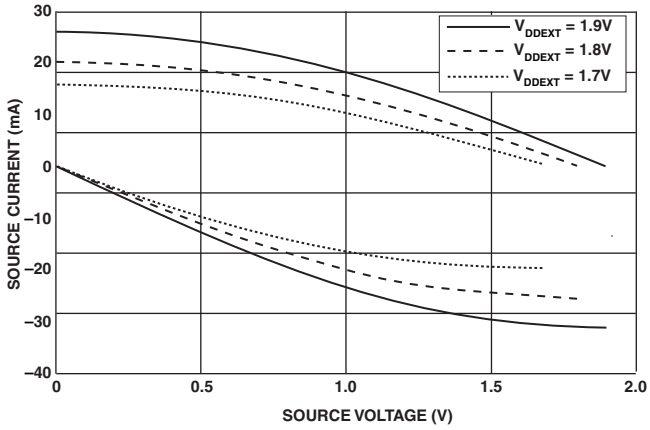


Figure 40. Drive Current C (V_{DDEXT} = 1.8 V)

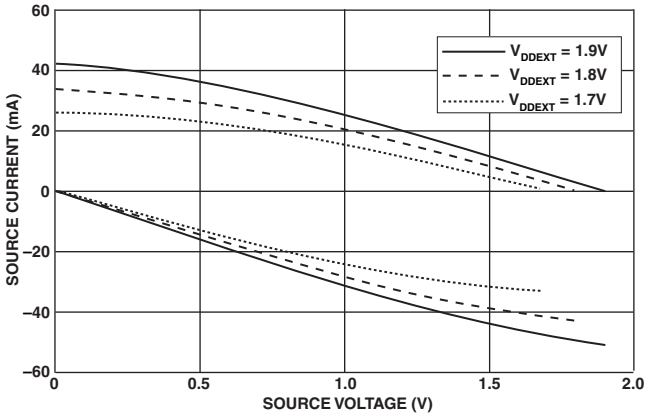


Figure 43. Drive Current D (V_{DDEXT} = 1.8 V)

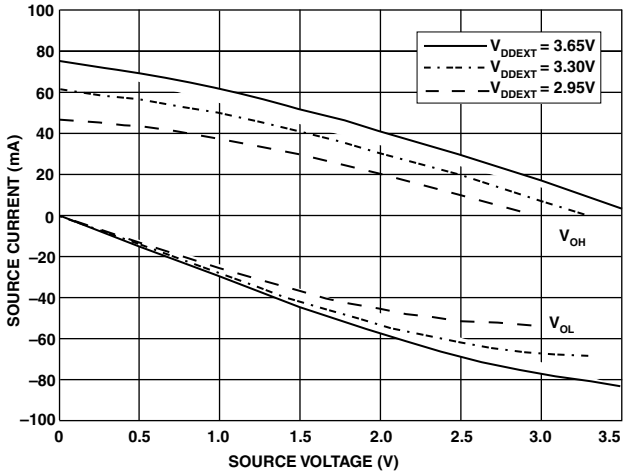


Figure 41. Drive Current C (V_{DDEXT} = 3.3 V)

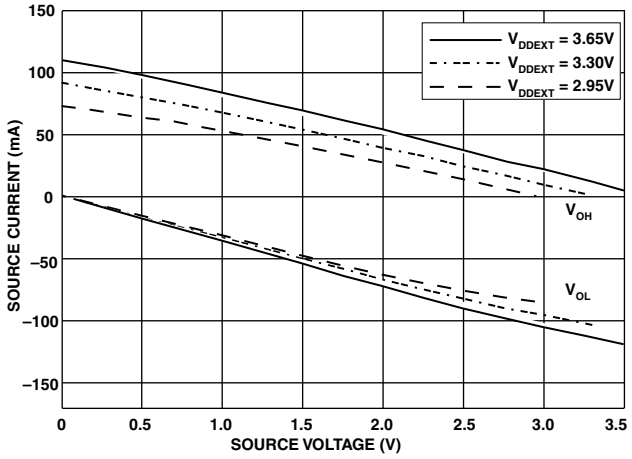


Figure 44. Drive Current D (V_{DDEXT} = 3.3 V)

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 45 shows the measurement point for ac measurements (except output enable/disable). The measurement point V_{MEAS} is 0.95 V for V_{DDEXT} (nominal) = 1.8 V or 1.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V.

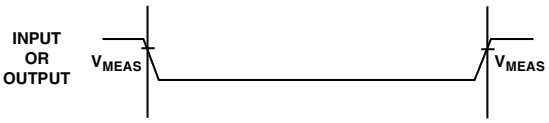


Figure 45. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 46.

The time $t_{ENA\_MEASURED}$ is the interval, from when the reference signal switches, to when the output voltage reaches V_{TRIP}(high) or V_{TRIP} (low).

For V_{DDEXT} (nominal) = 1.8 V—V_{TRIP} (high) is 1.3 V and V_{TRIP} (low) is 0.7 V.

For V_{DDEXT} (nominal) = 2.5 V/3.3 V—V_{TRIP} (high) is 2.0 V and V_{TRIP} (low) is 1.0 V.

Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the V_{TRIP} (high) or V_{TRIP} (low) trip voltage.

Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 45.

$$t_{DIS} = t_{DIS\_MEASURED} - t_{DECAY}$$

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load C_L and the load current I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.1 V for V_{DDEXT} (nominal) = 1.8 V or 0.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V.

The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches, to when the output voltage decays ΔV from the measured output high or output low voltage.

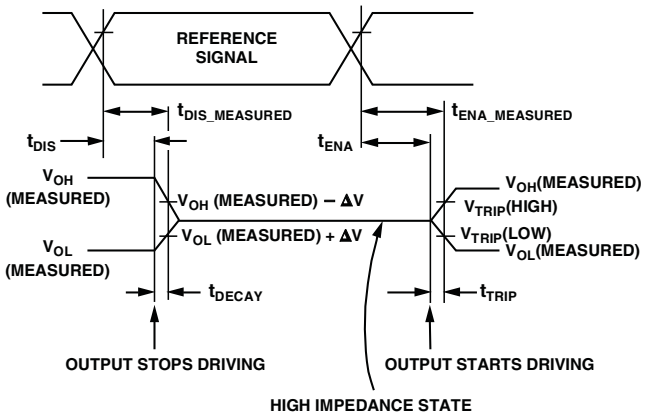


Figure 46. Output Enable/Disable

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the processor's output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time is t_{DECAY} plus the various output disable times as specified in the Timing Specifications on Page 27 (for example t_{DSDAT} for an SDRAM write cycle as shown in SDRAM Interface Timing on Page 30).

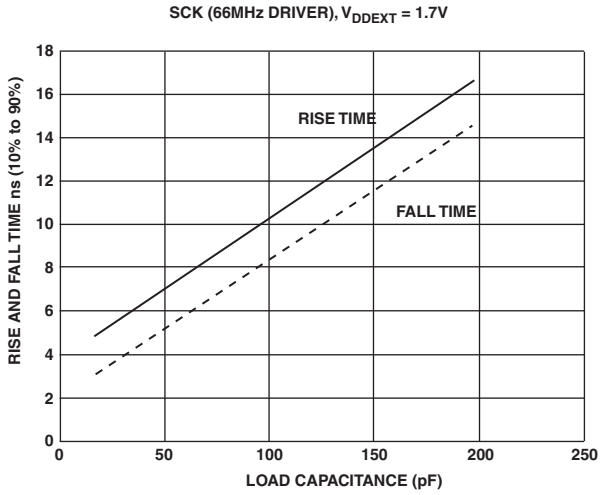


Figure 57. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at V_{DDEXT} = 1.75 V

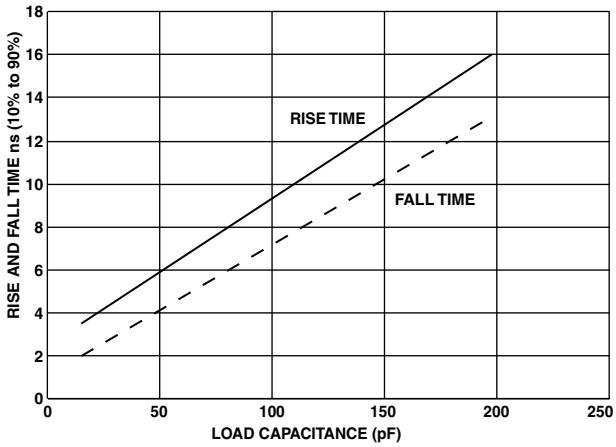


Figure 58. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at V_{DDEXT} = 2.25 V

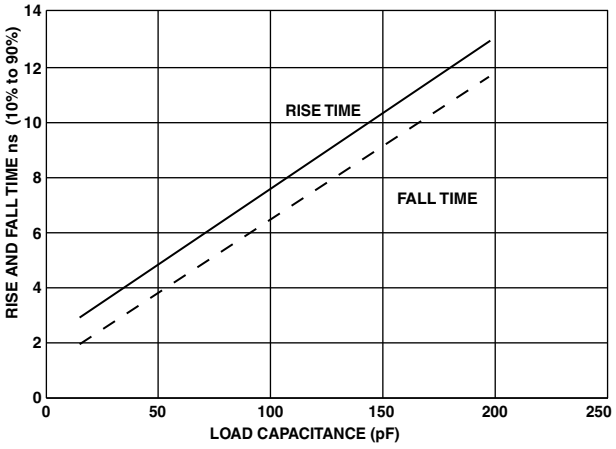


Figure 59. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at V_{DDEXT} = 3.65 V

THERMAL CHARACTERISTICS

To determine the junction temperature on the application printed circuit board, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C).

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 38 through Table 40.

P_D = Power dissipation (see the power dissipation discussion and the tables on 23 for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature (°C).

In Table 38 through Table 40, airflow measurements comply with JEDEC standards JESD51–2 and JESD51–6, and the junction-to-board measurement complies with JESD51–8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Thermal resistance θ_{JA} in Table 38 through Table 40 is the figure of merit relating to performance of the package and board in a convective environment. θ_{JMA} represents the thermal resistance under two conditions of airflow. Ψ_{JT} represents the correlation between T_J and T_{CASE}.

Table 38. Thermal Characteristics for BC-160 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	27.1	°C/W
θ_{JMA}	1 Linear m/s Airflow	23.85	°C/W
θ_{JMA}	2 Linear m/s Airflow	22.7	°C/W
θ_{JC}	Not Applicable	7.26	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.14	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.26	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.35	°C/W

Table 39. Thermal Characteristics for ST-176-1 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	34.9	°C/W
θ_{JMA}	1 Linear m/s Airflow	33.0	°C/W
θ_{JMA}	2 Linear m/s Airflow	32.0	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.50	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.75	°C/W
Ψ_{JT}	2 Linear m/s Airflow	1.00	°C/W

Table 40. Thermal Characteristics for B-169 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	22.8	°C/W
θ_{JMA}	1 Linear m/s Airflow	20.3	°C/W
θ_{JMA}	2 Linear m/s Airflow	19.3	°C/W
θ_{JC}	Not Applicable	10.39	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.59	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.88	°C/W
Ψ_{JT}	2 Linear m/s Airflow	1.37	°C/W

Figure 60 shows the top view of the CSP_BGA ball configuration. Figure 61 shows the bottom view of the CSP_BGA ball configuration.

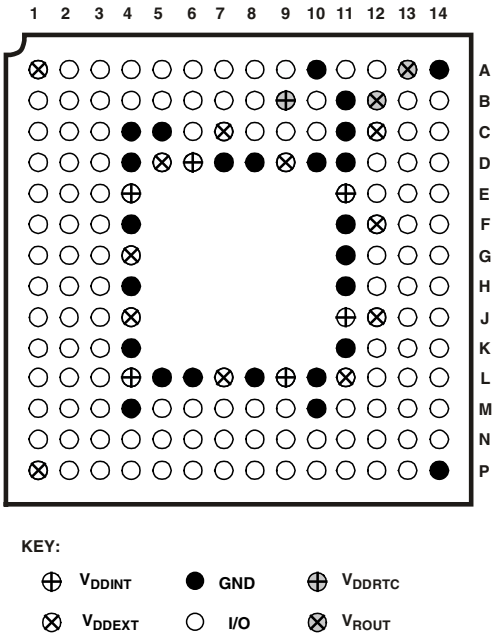


Figure 60. 160-Ball CSP_BGA Ground Configuration (Top View)

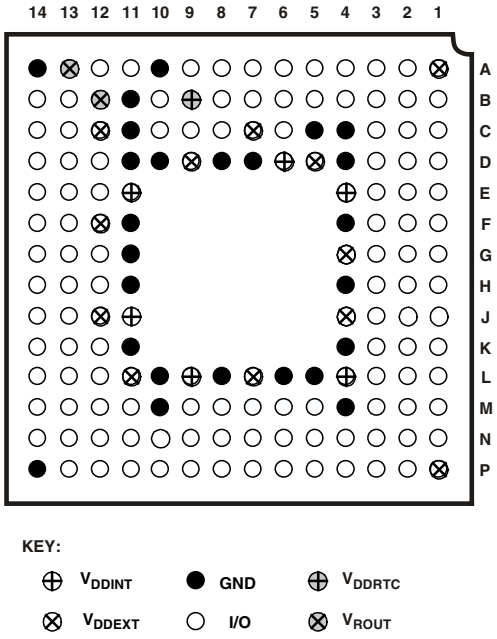


Figure 61. 160-Ball CSP_BGA Ground Configuration (Bottom View)

169-BALL PBGA BALL ASSIGNMENT

Table 43 lists the PBGA ball assignment by signal. Table 44 on Page 54 lists the PBGA ball assignment by ball number.

Table 43. 169-Ball PBGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{ABE0}$	H16	DATA4	U12	GND	K9	RTXI	A10	V_{DDEXT}	K6
$\overline{ABE1}$	H17	DATA5	U11	GND	K10	RTXO	A11	V_{DDEXT}	L6
ADDR1	J16	DATA6	T10	GND	K11	RX	T1	V_{DDEXT}	M6
ADDR2	J17	DATA7	U10	GND	L7	SA10	B15	V_{DDEXT}	M7
ADDR3	K16	DATA8	T9	GND	L8	$\overline{SCAS}$	A16	V_{DDEXT}	M8
ADDR4	K17	DATA9	U9	GND	L9	SCK	D1	V_{DDEXT}	T2
ADDR5	L16	DATA10	T8	GND	L10	SCKE	B14	VROUT0	B12
ADDR6	L17	DATA11	U8	GND	L11	$\overline{SMS}$	A17	VROUT1	B13
ADDR7	M16	DATA12	U7	GND	M9	$\overline{SRAS}$	A15	XTAL	A13
ADDR8	M17	DATA13	T7	GND	T16	$\overline{SWE}$	B17		
ADDR9	N17	DATA14	U6	MISO	E2	TCK	U4		
ADDR10	N16	DATA15	T6	MOSI	E1	TDI	U3		
ADDR11	P17	DR0PRI	M2	NMI	B11	TDO	T4		
ADDR12	P16	DR0SEC	M1	PF0	D2	TFS0	L1		
ADDR13	R17	DR1PRI	H1	PF1	C1	TFS1	G2		
ADDR14	R16	DR1SEC	H2	PF2	B1	TMR0	R1		
ADDR15	T17	DT0PRI	K2	PF3	C2	TMR1	P2		
ADDR16	U15	DT0SEC	K1	PF4	A1	TMR2	P1		
ADDR17	T15	DT1PRI	F1	PF5	A2	TMS	T3		
ADDR18	U16	DT1SEC	F2	PF6	B3	$\overline{TRST}$	U2		
ADDR19	T14	$\overline{EMU}$	U1	PF7	A3	TSCLK0	L2		
$\overline{AMS0}$	D17	GND	B16	PF8	B4	TSCLK1	G1		
$\overline{AMS1}$	E16	GND	F11	PF9	A4	TX	R2		
$\overline{AMS2}$	E17	GND	G7	PF10	B5	VDD	F12		
$\overline{AMS3}$	F16	GND	G8	PF11	A5	VDD	G12		
$\overline{AOE}$	F17	GND	G9	PF12	A6	VDD	H12		
ARDY	C16	GND	G10	PF13	B6	VDD	J12		
$\overline{ARE}$	G16	GND	G11	PF14	A7	VDD	K12		
$\overline{AWE}$	G17	GND	H7	PF15	B7	VDD	L12		
$\overline{BG}$	T13	GND	H8	PPI_CLK	B10	VDD	M10		
$\overline{BGH}$	U17	GND	H9	PPI0	B9	VDD	M11		
BMODE0	U5	GND	H10	PPI1	A9	VDD	M12		
BMODE1	T5	GND	H11	PPI2	B8	V_{DDEXT}	B2		
$\overline{BR}$	C17	GND	J7	PPI3	A8	V_{DDEXT}	F6		
CLKIN	A14	GND	J8	$\overline{RESET}$	A12	V_{DDEXT}	F7		
CLKOUT	D16	GND	J9	RFS0	N1	V_{DDEXT}	F8		
DATA0	U14	GND	J10	RFS1	J1	V_{DDEXT}	F9		
DATA1	T12	GND	J11	RSCLK0	N2	V_{DDEXT}	G6		
DATA2	U13	GND	K7	RSCLK1	J2	V_{DDEXT}	H6		
DATA3	T11	GND	K8	RTCVDD	F10	V_{DDEXT}	J6		

176-LEAD LQFP PINOUT

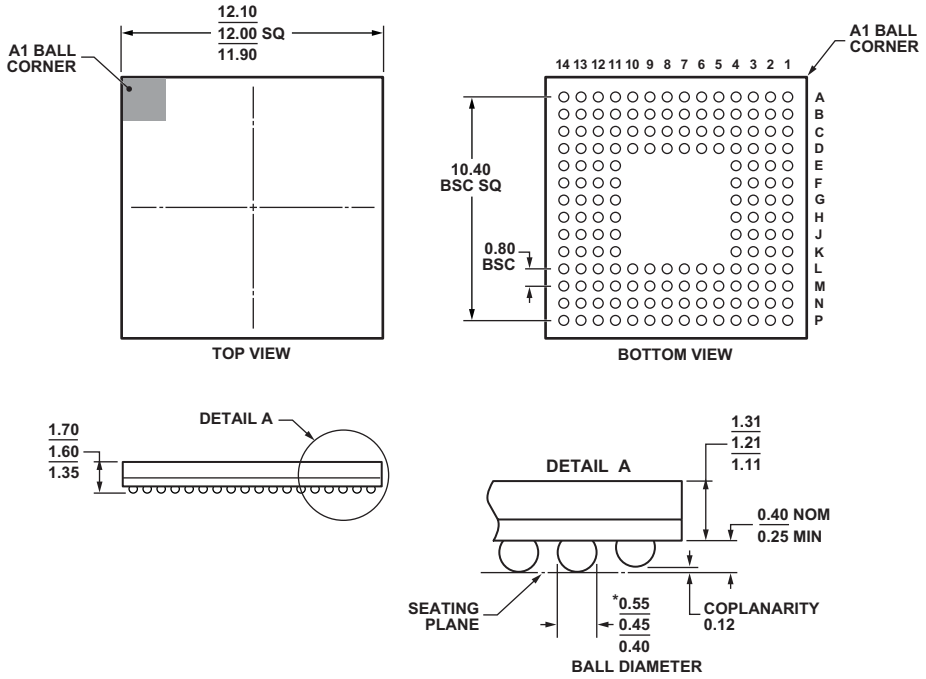
Table 45 lists the LQFP pinout by signal. Table 46 on Page 57 lists the LQFP pinout by lead number.

Table 45. 176-Lead LQFP Pin Assignment (Alphabetical by Signal)

Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.
$\overline{ABE0}$	151	DATA3	113	GND	88	PPI_CLK	21	V_{DDEXT}	71
$\overline{ABE1}$	150	DATA4	112	GND	89	PPI0	22	V_{DDEXT}	93
ADDR1	149	DATA5	110	GND	90	PPI1	23	V_{DDEXT}	107
ADDR2	148	DATA6	109	GND	91	PPI2	24	V_{DDEXT}	118
ADDR3	147	DATA7	108	GND	92	PPI3	26	V_{DDEXT}	134
ADDR4	146	DATA8	105	GND	97	$\overline{RESET}$	13	V_{DDEXT}	145
ADDR5	142	DATA9	104	GND	106	RFS0	75	V_{DDEXT}	156
ADDR6	141	DATA10	103	GND	117	RFS1	64	V_{DDEXT}	171
ADDR7	140	DATA11	102	GND	128	RSCLK0	76	V_{DDINT}	25
ADDR8	139	DATA12	101	GND	129	RSCLK1	65	V_{DDINT}	52
ADDR9	138	DATA13	100	GND	130	RTXI	17	V_{DDINT}	66
ADDR10	137	DATA14	99	GND	131	RTXO	16	V_{DDINT}	80
ADDR11	136	DATA15	98	GND	132	RX	82	V_{DDINT}	111
ADDR12	135	DR0PRI	74	GND	133	SA10	164	V_{DDINT}	143
ADDR13	127	DR0SEC	73	GND	144	$\overline{SCAS}$	166	V_{DDINT}	157
ADDR14	126	DR1PRI	63	GND	155	SCK	53	V_{DDINT}	168
ADDR15	125	DR1SEC	62	GND	170	SCKE	173	V_{DDRTC}	18
ADDR16	124	DT0PRI	68	GND	174	$\overline{SMS}$	172	VROUT0	5
ADDR17	123	DT0SEC	67	GND	175	$\overline{SRAS}$	167	VROUT1	4
ADDR18	122	DT1PRI	59	GND	176	$\overline{SWE}$	165	XTAL	11
ADDR19	121	DT1SEC	58	MISO	54	TCK	94		
$\overline{AMS0}$	161	$\overline{EMU}$	83	MOSI	55	TDI	86		
$\overline{AMS1}$	160	GND	1	NMI	14	TDO	87		
$\overline{AMS2}$	159	GND	2	PF0	51	TFS0	69		
$\overline{AMS3}$	158	GND	3	PF1	50	TFS1	60		
$\overline{AOE}$	154	GND	7	PF2	49	TMR0	79		
ARDY	162	GND	8	PF3	48	TMR1	78		
$\overline{ARE}$	153	GND	9	PF4	47	TMR2	77		
$\overline{AWE}$	152	GND	15	PF5	46	TMS	85		
$\overline{BG}$	119	GND	19	PF6	38	$\overline{TRST}$	84		
$\overline{BGH}$	120	GND	30	PF7	37	TSCLK0	72		
BMODE0	96	GND	39	PF8	36	TSCLK1	61		
BMODE1	95	GND	40	PF9	35	TX	81		
$\overline{BR}$	163	GND	41	PF10	34	V_{DDEXT}	6		
CLKIN	10	GND	42	PF11	33	V_{DDEXT}	12		
CLKOUT	169	GND	43	PF12	32	V_{DDEXT}	20		
DATA0	116	GND	44	PF13	29	V_{DDEXT}	31		
DATA1	115	GND	56	PF14	28	V_{DDEXT}	45		
DATA2	114	GND	70	PF15	27	V_{DDEXT}	57		

Table 46. 176-Lead LQFP Pin Assignment (Numerical by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	GND	41	GND	81	TX	121	ADDR19	161	$\overline{AMS0}$
2	GND	42	GND	82	RX	122	ADDR18	162	ARDY
3	GND	43	GND	83	$\overline{EMU}$	123	ADDR17	163	$\overline{BR}$
4	VROUT1	44	GND	84	$\overline{TRST}$	124	ADDR16	164	SA10
5	VROUT0	45	V_{DDEXT}	85	TMS	125	ADDR15	165	$\overline{SWE}$
6	V_{DDEXT}	46	PF5	86	TDI	126	ADDR14	166	$\overline{SCAS}$
7	GND	47	PF4	87	TDO	127	ADDR13	167	$\overline{SRAS}$
8	GND	48	PF3	88	GND	128	GND	168	V_{DDINT}
9	GND	49	PF2	89	GND	129	GND	169	CLKOUT
10	CLKIN	50	PF1	90	GND	130	GND	170	GND
11	XTAL	51	PF0	91	GND	131	GND	171	V_{DDEXT}
12	V_{DDEXT}	52	V_{DDINT}	92	GND	132	GND	172	$\overline{SMS}$
13	$\overline{RESET}$	53	SCK	93	V_{DDEXT}	133	GND	173	SCKE
14	NMI	54	MISO	94	TCK	134	V_{DDEXT}	174	GND
15	GND	55	MOSI	95	BMODE1	135	ADDR12	175	GND
16	RTXO	56	GND	96	BMODE0	136	ADDR11	176	GND
17	RTXI	57	V_{DDEXT}	97	GND	137	ADDR10		
18	V_{DDRTC}	58	DT1SEC	98	DATA15	138	ADDR9		
19	GND	59	DT1PRI	99	DATA14	139	ADDR8		
20	V_{DDEXT}	60	TFS1	100	DATA13	140	ADDR7		
21	PPI_CLK	61	TSCLK1	101	DATA12	141	ADDR6		
22	PPI0	62	DR1SEC	102	DATA11	142	ADDR5		
23	PPI1	63	DR1PRI	103	DATA10	143	V_{DDINT}		
24	PPI2	64	RFS1	104	DATA9	144	GND		
25	V_{DDINT}	65	RSCLK1	105	DATA8	145	V_{DDEXT}		
26	PPI3	66	V_{DDINT}	106	GND	146	ADDR4		
27	PF15	67	DT0SEC	107	V_{DDEXT}	147	ADDR3		
28	PF14	68	DT0PRI	108	DATA7	148	ADDR2		
29	PF13	69	TFS0	109	DATA6	149	ADDR1		
30	GND	70	GND	110	DATA5	150	$\overline{ABE1}$		
31	V_{DDEXT}	71	V_{DDEXT}	111	V_{DDINT}	151	$\overline{ABE0}$		
32	PF12	72	TSCLK0	112	DATA4	152	$\overline{AWE}$		
33	PF11	73	DR0SEC	113	DATA3	153	$\overline{ARE}$		
34	PF10	74	DR0PRI	114	DATA2	154	$\overline{AOE}$		
35	PF9	75	RFS0	115	DATA1	155	GND		
36	PF8	76	RSCLK0	116	DATA0	156	V_{DDEXT}		
37	PF7	77	TMR2	117	GND	157	V_{DDINT}		
38	PF6	78	TMR1	118	V_{DDEXT}	158	$\overline{AMS3}$		
39	GND	79	TMR0	119	$\overline{BG}$	159	$\overline{AMS2}$		
40	GND	80	V_{DDINT}	120	$\overline{BGH}$	160	$\overline{AMS1}$		



*COMPLIANT TO JEDEC STANDARDS MO-205-AE WITH THE EXCEPTION TO BALL DIAMETER.

Figure 65. 160-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-160-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model [1]	Temperature Range [2]	Speed Grade (Max)	Package Description	Package Option
ADSP-BF531SBB400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF531SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF531SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF531SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF531SBBCZ4RL	–40°C to +85°C	400 MHz	160-Ball CSP_BGA, 13" Tape and Reel	BC-160-2
ADSP-BF531SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF532SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF532SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF532SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF532SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF533SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF533SBB500	–40°C to +85°C	500 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBZ500	–40°C to +85°C	500 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBC500	–40°C to +85°C	500 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ500	–40°C to +85°C	500 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBC-5V	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ-5V	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKBC-6V	0°C to +70°C	600 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKBCZ-6V	0°C to +70°C	600 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKSTZ-5V	0°C to +70°C	533 MHz	176-Lead LQFP	ST-176-1

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 20 for junction temperature (T_J) specification which is the only temperature specification.