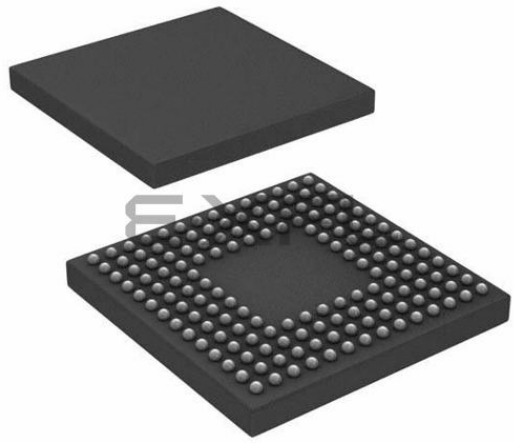

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	533MHz
Non-Volatile Memory	ROM (1kB)
On-Chip RAM	148kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LFBGA, CSPBGA
Supplier Device Package	160-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf533sbbcz-5v

BLACKFIN PROCESSOR CORE

As shown in Figure 2 on Page 5, the Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-bit, 16-bit, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo 2^{32} multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions includes byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). Quad 16-bit operations are possible using the second ALU.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

MEMORY ARCHITECTURE

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors view memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low latency on-chip memory as cache or SRAM, and larger, lower cost and performance off-chip memory systems. See Figure 3, Figure 4, and Figure 5 on Page 6.

The L1 memory system is the primary highest performance memory available to the Blackfin processor. The off-chip memory system, accessed through the external bus interface unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing up to 132M bytes of physical memory.

The memory DMA controller provides high bandwidth data-movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

Internal (On-Chip) Memory

The processors have three blocks of on-chip memory that provide high bandwidth access to the core.

The first block is the L1 instruction memory, consisting of up to 80K bytes SRAM, of which 16K bytes can be configured as a four way set-associative cache. This memory is accessed at full processor speed.

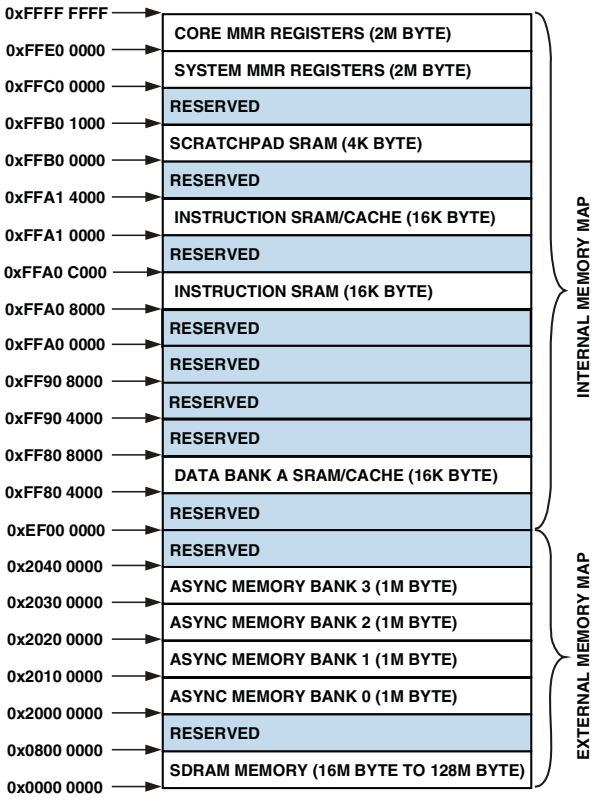


Figure 3. ADSP-BF531 Internal/External Memory Map

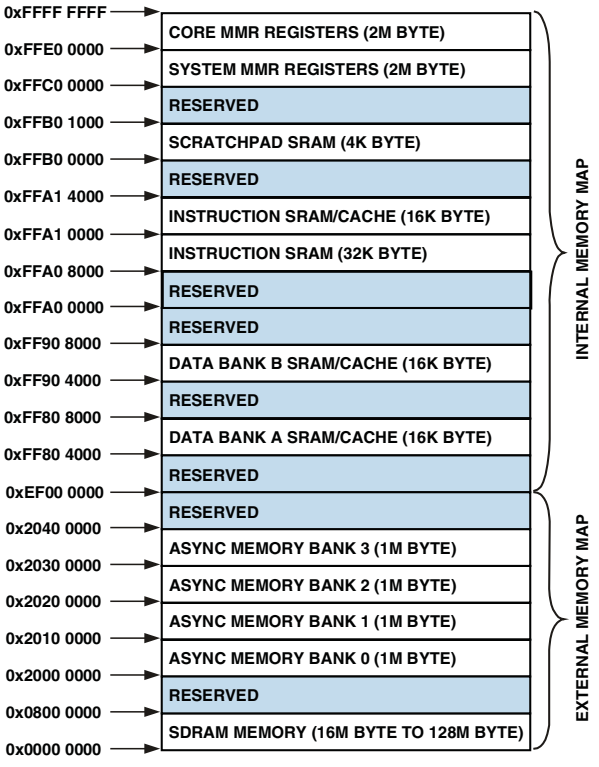


Figure 4. ADSP-BF532 Internal/External Memory Map

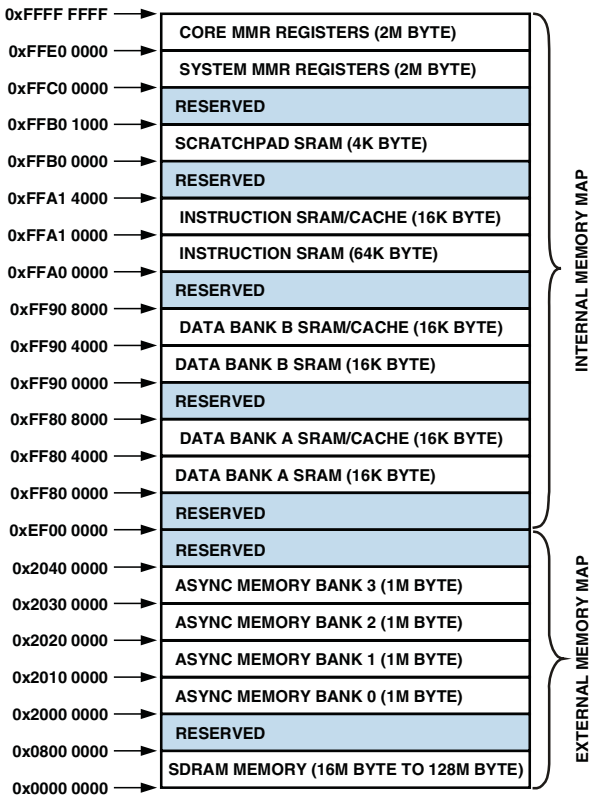


Figure 5. ADSP-BF533 Internal/External Memory Map

Event Handling

The event controller on the processors handle all asynchronous and synchronous events to the processor. The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provide event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher priority event takes precedence over servicing of a lower priority event. The controller provides support for five different types of events:

- Emulation – An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- Reset – This event resets the processor.
- Nonmaskable Interrupt (NMI) – The NMI event can be generated by the software watchdog timer or by the NMI input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- Exceptions – Events that occur synchronously to program flow (i.e., the exception is taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts – Events that occur asynchronously to program flow. They are caused by input pins, timers, and other peripherals, as well as by an explicit software instruction.

- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data-word or after transferring an entire data buffer or buffers through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1,024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

An additional 250 mV of SPORT input hysteresis can be enabled by setting Bit 15 of the PLL_CTL register. When this bit is set, all SPORT input pins have the increased hysteresis.

SERIAL PERIPHERAL INTERFACE (SPI) PORT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have an SPI-compatible port that enables the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins (master output-slave input, MOSI, and master input-slave output, MISO) and a clock pin (serial clock, SCK). An SPI chip select input pin ($\overline{\text{SPISS}}$) lets other SPI devices select the processor, and seven SPI chip select output pins ($\overline{\text{SPISEL7–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface which supports both master/slave modes and multimaster environments.

The baud rate and clock phase/polarities for the SPI port are programmable, and it has an integrated DMA controller, configurable to support transmit or receive data streams. The SPI DMA controller can only service unidirectional accesses at any given time.

The SPI port clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provide a full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART port includes support for 5 data bits to 8 data bits, 1 stop bit or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The baud rate, serial data format, error code generation and status, and interrupts for the UART port are programmable.

The UART programmable features include:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) bits per second to (f_{SCLK}/16) bits per second.
- Supporting data formats from seven bits to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as:

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16 \times UART\_Divisor}$$

where the 16-bit UART_Divisor comes from the UART_DLH register (most significant 8 bits) and UART_DLL register (least significant 8 bits).

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The capabilities of the UART are further extended with support for the Infrared Data Association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

GENERAL-PURPOSE I/O PORT F

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have 16 bidirectional, general-purpose I/O pins on Port F (PF15–0). Each general-purpose I/O pin can be individually controlled by manipulation of the GPIO control, status and interrupt registers:

- GPIO direction control register – Specifies the direction of each individual PFx pin as input or output.
- GPIO control and status registers – The processor employs a "write one to modify" mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins. Four control registers are provided. One register is written in order to set GPIO pin values, one register is written in order to clear GPIO pin values, one register is written in order to toggle GPIO pin values, and one register is written in order to specify GPIO pin values. Reading the GPIO status register allows software to interrogate the sense of the GPIO pin.
- GPIO interrupt mask registers – The two GPIO interrupt mask registers allow each individual PFx pin to function as an interrupt to the processor. Similar to the two GPIO control registers that are used to set and clear individual GPIO pin values, one GPIO interrupt mask register sets bits to enable interrupt function, and the other GPIO interrupt mask register clears bits to disable interrupt function.

PFx pins defined as inputs can be configured to generate hardware interrupts, while output PFx pins can be triggered by software interrupts.

- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual PFx pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

PARALLEL PERIPHERAL INTERFACE

The processors provide a parallel peripheral interface (PPI) that can connect directly to parallel ADCs and DACs, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bi-directional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bi-directional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications.

Three distinct sub modes are supported:

- Input mode – Frame syncs and data are inputs into the PPI.
- Frame capture mode – Frame syncs are outputs from the PPI, but data are inputs.
- Output mode – Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (e.g., for frame capture). The processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct sub modes are supported:

- Active video only mode
- Vertical blanking only mode
- Entire field mode

Active Video Only Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that can be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

DYNAMIC POWER MANAGEMENT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provides four operating modes, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

PIN DESCRIPTIONS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors pin definitions are listed in Table 9.

All pins are three-stated during and immediately after reset, except the memory interface, asynchronous memory control, and synchronous memory control pins. These pins are all driven high, with the exception of CLKOUT, which toggles at the system clock rate. During hibernate, all outputs are three-stated unless otherwise noted in Table 9.

If $\overline{BR}$ is active (whether or not $\overline{RESET}$ is asserted), the memory pins are also three-stated. All unused I/O pins have their input buffers disabled with the exception of the pins that need pull-ups or pull-downs as noted in the table.

In order to maintain maximum functionality and reduce package size and pin count, some pins have dual, multiplexed functionality. In cases where pin functionality is reconfigurable, the default state is shown in plain text, while alternate functionality is shown in italics.

Table 9. Pin Descriptions

Pin Name	Type	Function	Driver Type[1]
Memory Interface			
ADDR19–1	O	Address Bus for Async/Sync Access	A
DATA15–0	I/O	Data Bus for Async/Sync Access	A
$\overline{ABE1–0}$/SDQM1–0	O	Byte Enables/Data Masks for Async/Sync Access	A
$\overline{BR}$	I	Bus Request (This pin should be pulled high if not used.)	
$\overline{BG}$	O	Bus Grant	A
$\overline{BGH}$	O	Bus Grant Hang	A
Asynchronous Memory Control			
$\overline{AMS3–0}$	O	Bank Select (Require pull-ups if hibernate is used.)	A
ARDY	I	Hardware Ready Control (This pin should be pulled high if not used.)	
$\overline{AOE}$	O	Output Enable	A
$\overline{ARE}$	O	Read Enable	A
$\overline{AWE}$	O	Write Enable	A
Synchronous Memory Control			
$\overline{SRAS}$	O	Row Address Strobe	A
$\overline{SCAS}$	O	Column Address Strobe	A
$\overline{SWE}$	O	Write Enable	A
SCKE	O	Clock Enable (Requires pull-down if hibernate is used.)	A
CLKOUT	O	Clock Output	B
SA10	O	A10 Pin	A
$\overline{SMS}$	O	Bank Select	A
Timers			
TMR0	I/O	Timer 0	C
TMR1/*PPI_FS1*	I/O	Timer 1/*PPI Frame Sync1*	C
TMR2/*PPI_FS2*	I/O	Timer 2/*PPI Frame Sync2*	C
PPI Port			
PPI3–0	I/O	PPI3–0	C
PPI_CLK/*TMRCLK*	I	PPI Clock/*External Timer Reference*	

Table 9. Pin Descriptions (Continued)

Pin Name	Type	Function	Driver Type[1]
RFS1	I/O	SPORT1 Receive Frame Sync	C
DR1PRI	I	SPORT1 Receive Data Primary	
DR1SEC	I	SPORT1 Receive Data Secondary	
TSCLK1	I/O	SPORT1 Transmit Serial Clock	D
TFS1	I/O	SPORT1 Transmit Frame Sync	C
DT1PRI	O	SPORT1 Transmit Data Primary	C
DT1SEC	O	SPORT1 Transmit Data Secondary	C
UART Port			
RX	I	UART Receive	
TX	O	UART Transmit	C
Real-Time Clock			
RTXI	I	RTC Crystal Input (This pin should be pulled low when not used.)	
RTXO	O	RTC Crystal Output (Does not three-state in hibernate.)	
Clock			
CLKIN	I	Clock/Crystal Input (This pin needs to be at a level or clocking.)	
XTAL	O	Crystal Output	
Mode Controls			
$\overline{\text{RESET}}$	I	Reset (This pin is always active during core power-on.)	
NMI	I	Nonmaskable Interrupt (This pin should be pulled low when not used.)	
BMODE1–0	I	Boot Mode Strap (These pins must be pulled to the state required for the desired boot mode.)	
Voltage Regulator			
VROUT1–0	O	External FET Drive (These pins should be left unconnected when unused and are driven high during hibernate.)	
Supplies			
V_{DDEXT}	P	I/O Power Supply	
V_{DDINT}	P	Core Power Supply	
V_{DDRTC}	P	Real-Time Clock Power Supply (This pin should be connected to V_{DDEXT} when not used and should remain powered at all times.)	
GND	G	External Ground	

[1] Refer to Figure 33 on Page 43 to Figure 44 on Page 44.

The following three tables describe the voltage/frequency requirements for the processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock (Table 10 and Table 11) and system clock (Table 13) specifications. Table 12 describes phase-locked loop operating conditions.

Table 10. Core Clock (CCLK) Requirements—500 MHz, 533 MHz, and 600 MHz Models

Parameter		Internal Regulator Setting	Max	Unit
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.3 V Minimum)[1]	1.30 V	600	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.2 V Minimum)[2]	1.25 V	533	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.14 V Minimum)[3]	1.20 V	500	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	444	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	400	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V	333	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V	250	MHz

[1] Applies to 600 MHz models only. See Ordering Guide on Page 63.
[2] Applies to 533 MHz and 600 MHz models only. See Ordering Guide on Page 63. 533 MHz models cannot support internal regulator levels above 1.25 V.
[3] Applies to 500 MHz, 533 MHz, and 600 MHz models. See Ordering Guide on Page 63. 500 MHz models cannot support internal regulator levels above 1.20 V.

Table 11. Core Clock (CCLK) Requirements—400 MHz Models[1]

Parameter		Internal Regulator Setting	T_J = 125°C Max	All[2] Other T_J Max	Unit
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	400	400	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	333	364	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	295	333	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V		280	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V		250	MHz

[1] See Ordering Guide on Page 63.
[2] See Operating Conditions on Page 20.

Table 12. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	50	Max f_{CCLK}	MHz

Table 13. System Clock (SCLK) Requirements

Parameter[1]		V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
CSP_BGA/PBGA				
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} \geq$ 1.14 V)	100	133	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.14 V)	100	100	MHz
LQFP				
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} \geq$ 1.14 V)	100	133	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.14 V)	83	83	MHz

[1] t_{SCLK} (= $1/f_{SCLK}$) must be greater than or equal to t_{CCLK}.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 18 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Table 18. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.45 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.5 V to +3.8 V
Input Voltage[1, 2]	–0.5 V to +3.8 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	125°C

[1] Applies to 100% transient duty cycle. For other duty cycles see Table 19.
[2] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2 V.

Table 19. Maximum Duty Cycle for Input Transient Voltage[1]

V_{IN} Min (V)[2]	V_{IN} Max (V)[2]	Maximum Duty Cycle[3]
–0.50	+3.80	100%
–0.70	+4.00	40%
–0.80	+4.10	25%
–0.90	+4.20	15%
–1.00	+4.30	10%

[1] Applies to all signal pins with the exception of CLKIN, XTAL, VROUT1–0.
[2] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.
[3] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

External Port Bus Request and Grant Cycle Timing

Table 26 and Figure 16 describe external port bus request and bus grant operations.

Table 26. External Port Bus Request and Grant Cycle Timing

Parameter	V_{DDEXT} = 1.8 V LQFP/PBGA Packages		V_{DDEXT} = 1.8 V CSP_BGA Package		V_{DDEXT} = 2.5 V/3.3 V All Packages		Unit
	Min	Max	Min	Max	Min	Max	
Timing Requirements							
t_{BS} $\overline{BR}$ Asserted to CLKOUT High Setup	4.6		4.6		4.6		ns
t_{BH} CLKOUT High to $\overline{BR}$ Deasserted Hold Time	1.0		1.0		0.0		ns
Switching Characteristics							
t_{SD} CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Disable		4.5		4.5		4.5	ns
t_{SE} CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Enable		4.5		4.5		4.5	ns
t_{DBG} CLKOUT High to $\overline{BG}$ High Setup		6.0		5.5		3.6	ns
t_{EBG} CLKOUT High to $\overline{BG}$ Deasserted Hold Time		6.0		4.6		3.6	ns
t_{DBH} CLKOUT High to $\overline{BGH}$ High Setup		6.0		5.5		3.6	ns
t_{EBH} CLKOUT High to $\overline{BGH}$ Deasserted Hold Time		6.0		4.6		3.6	ns

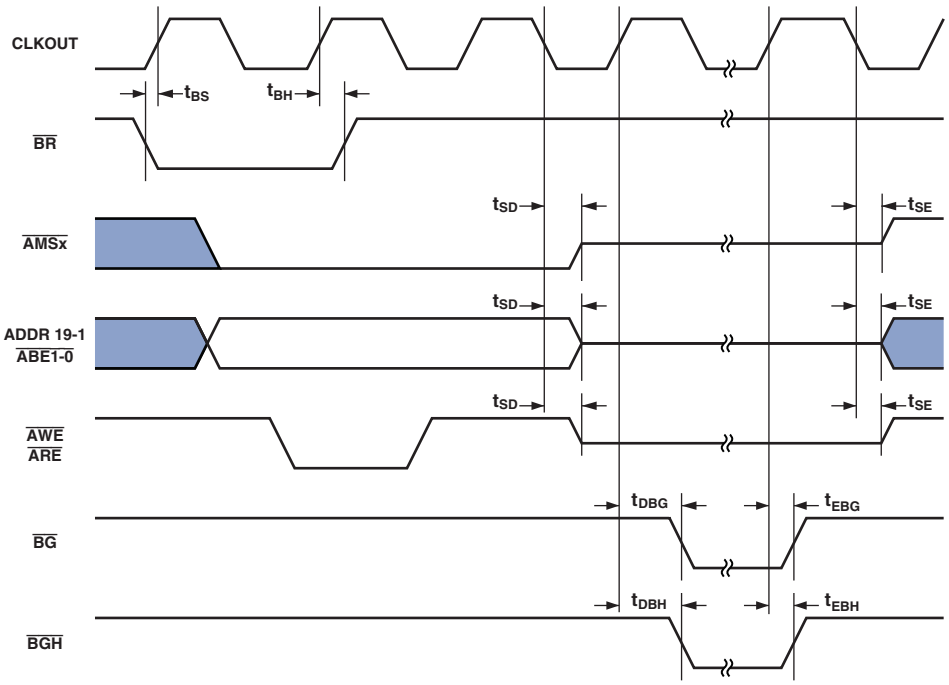


Figure 16. External Port Bus Request and Grant Cycle Timing

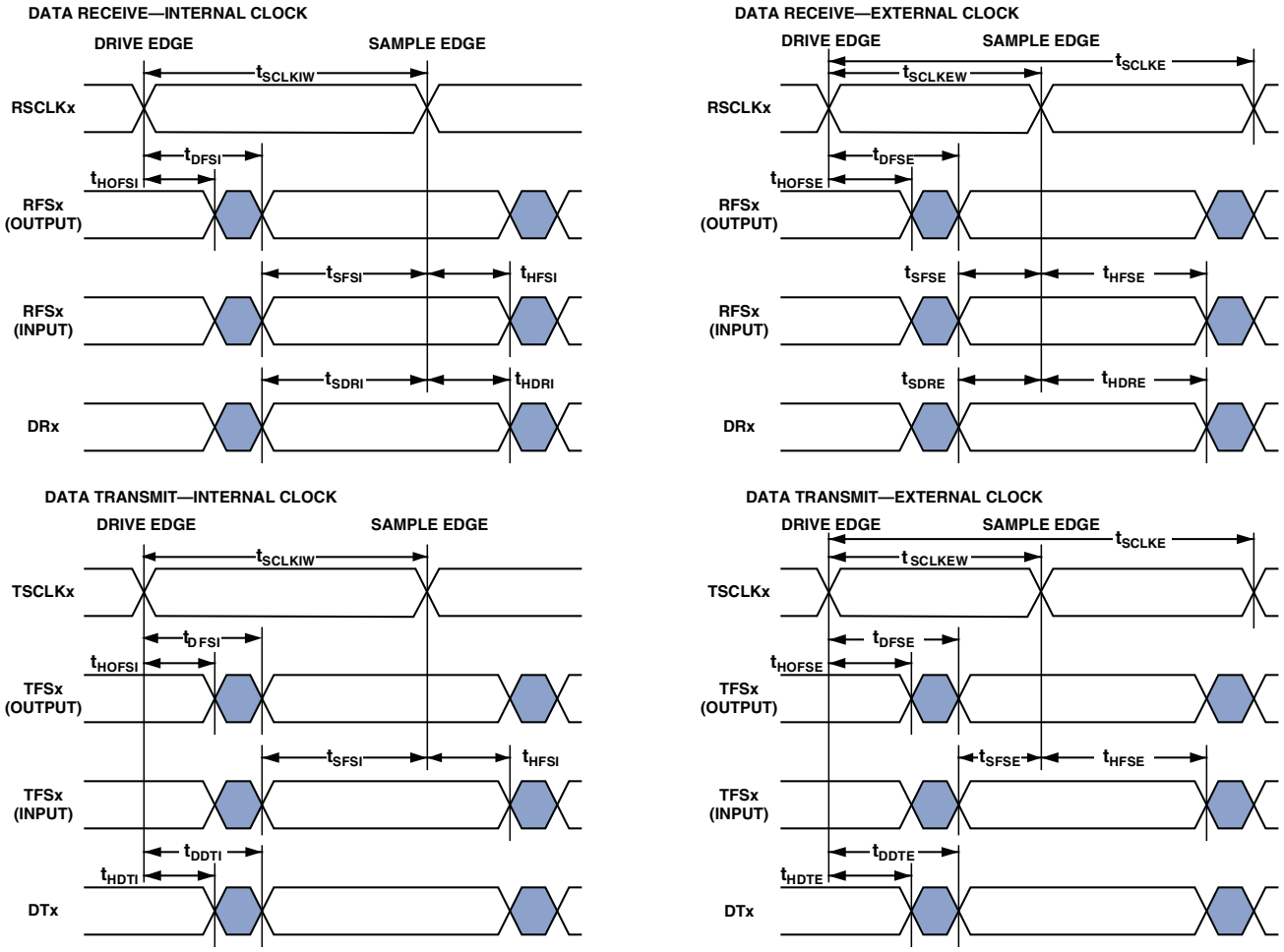


Figure 23. Serial Ports

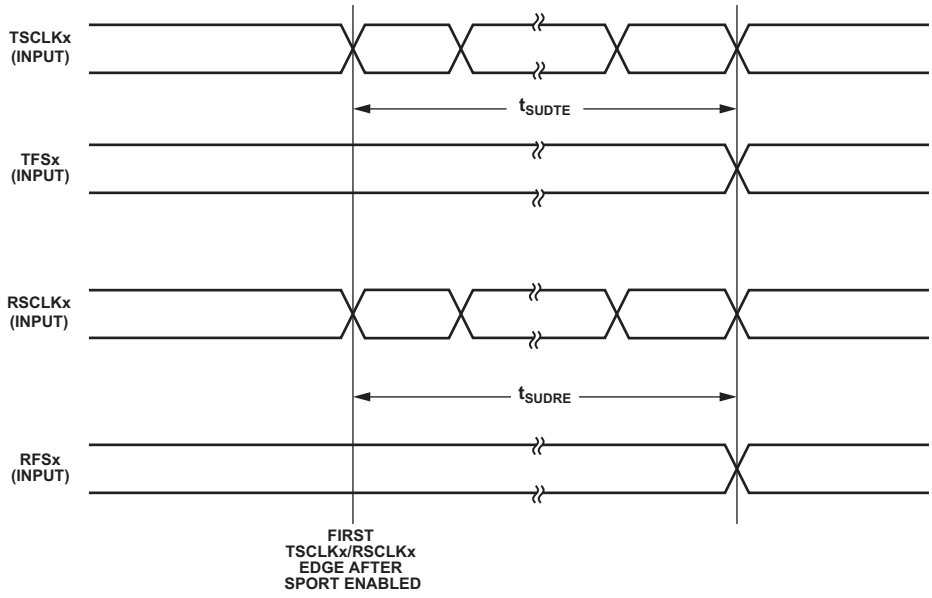


Figure 24. Serial Port Start Up with External Clock and Frame Sync

Timer Clock Timing

Table 35 and Figure 30 describe timer clock timing.

Table 35. Timer Clock Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TODP}	Timer Output Update Delay After PPI_CLK High		12	ns

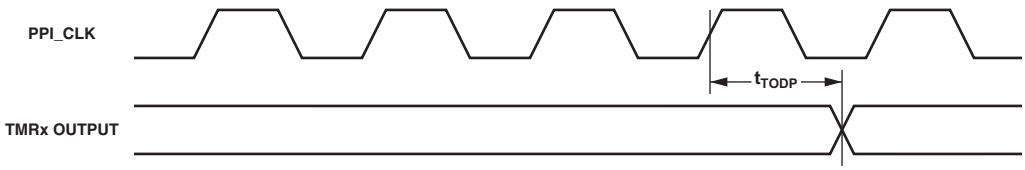


Figure 30. Timer Clock Timing

Timer Cycle Timing

Table 36 and Figure 31 describe timer expired operations. The input signal is asynchronous in width capture mode and external clock mode and has an absolute maximum input frequency of $f_{SCLK}/2$ MHz.

Table 36. Timer Cycle Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Characteristics						
t_{WL}	Timer Pulse Width Low[1]	$1 \times t_{SCLK}$		$1 \times t_{SCLK}$		ns
t_{WH}	Timer Pulse Width High[1]	$1 \times t_{SCLK}$		$1 \times t_{SCLK}$		ns
t_{TIS}	Timer Input Setup Time Before CLKOUT Low[2]	8.0		6.5		ns
t_{TIH}	Timer Input Hold Time After CLKOUT Low[2]	1.5		1.5		ns
Switching Characteristics						
t_{HTO}	Timer Pulse Width Output	$1 \times t_{SCLK}$	$(2^{32}-1) \times t_{SCLK}$	$1 \times t_{SCLK}$	$(2^{32}-1) \times t_{SCLK}$	ns
t_{TOD}	Timer Output Update Delay After CLKOUT High		7.5		6.5	ns

[1] The minimum pulse widths apply for TMRx input pins in width capture and external clock modes. They also apply to the PF1 or PPI_CLK input pins in PWM output mode.
[2] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize programmable flag inputs.

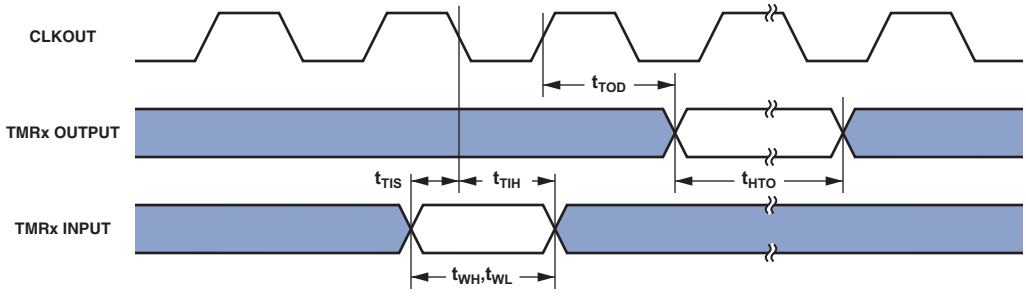


Figure 31. Timer PWM_OUT Cycle Timing

OUTPUT DRIVE CURRENTS

Figure 33 through Figure 44 show typical current-voltage characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

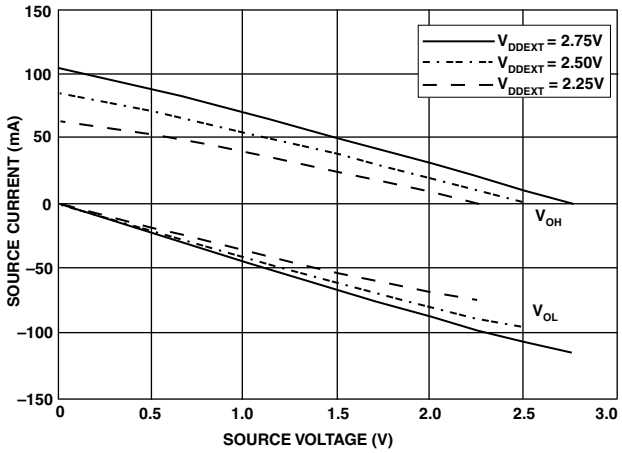


Figure 33. Drive Current A (V_{DDEXT} = 2.5 V)

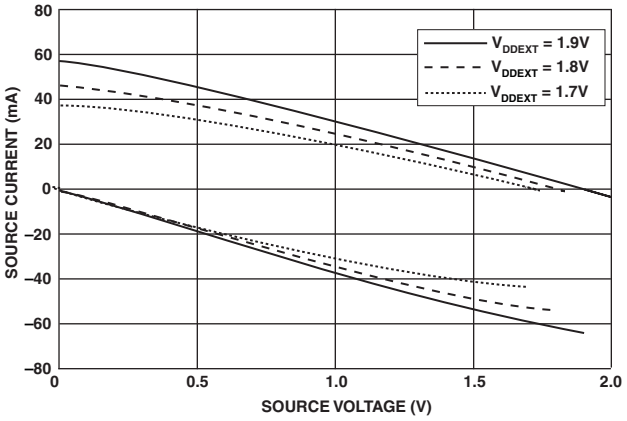


Figure 34. Drive Current A (V_{DDEXT} = 1.8 V)

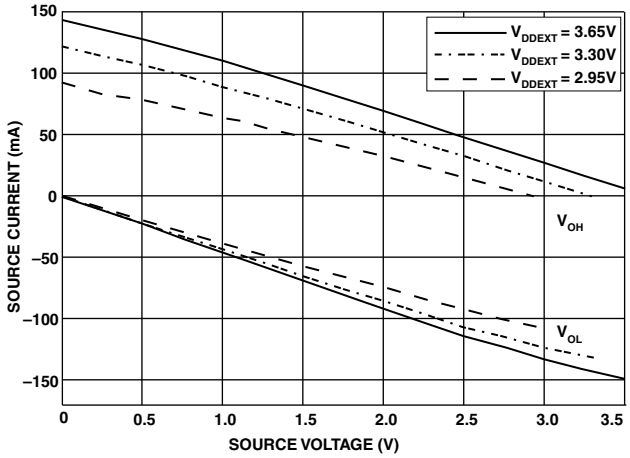


Figure 35. Drive Current A (V_{DDEXT} = 3.3 V)

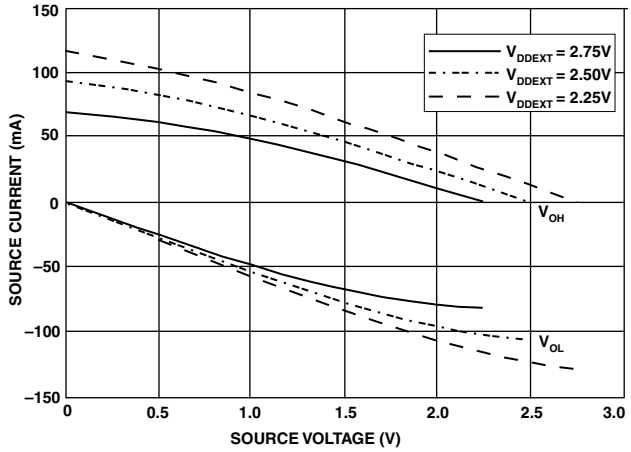


Figure 36. Drive Current B (V_{DDEXT} = 2.5 V)

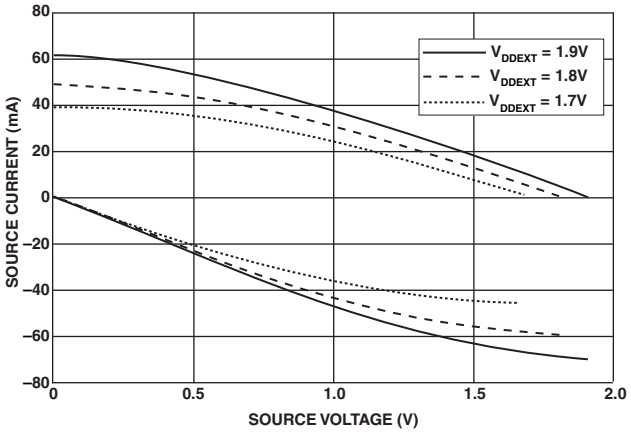


Figure 37. Drive Current B (V_{DDEXT} = 1.8 V)

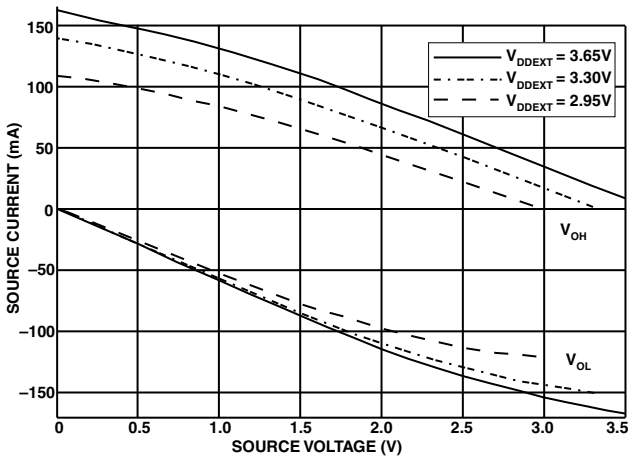
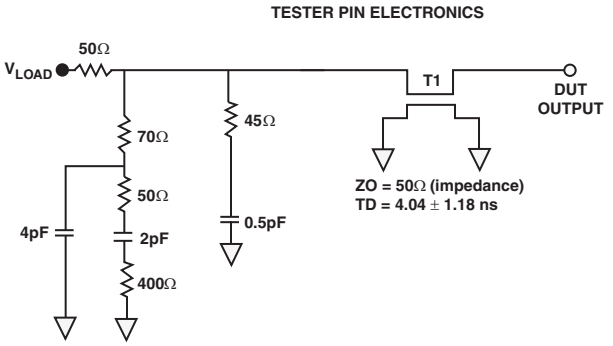


Figure 38. Drive Current B (V_{DDEXT} = 3.3 V)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 47). V_{LOAD} is 0.95 V for V_{DDEXT} (nominal) = 1.8 V or 1.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V. Figure 48 through Figure 59 on Page 48 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 47. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

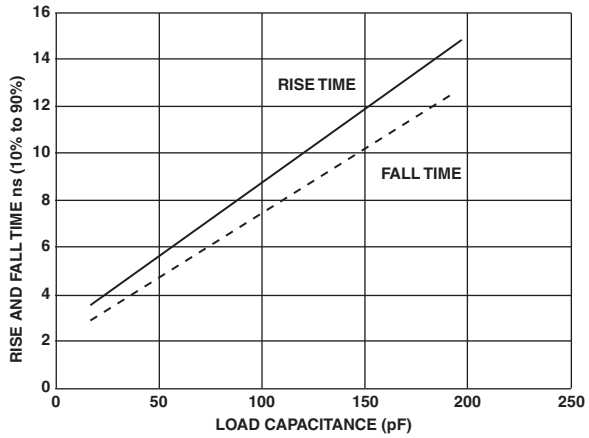


Figure 48. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 1.75 V

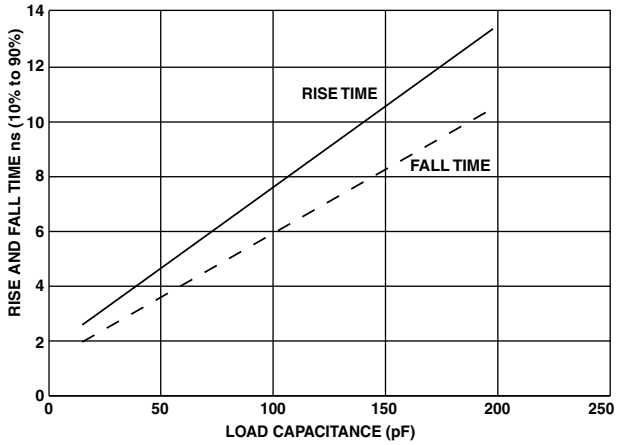


Figure 49. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 2.25 V

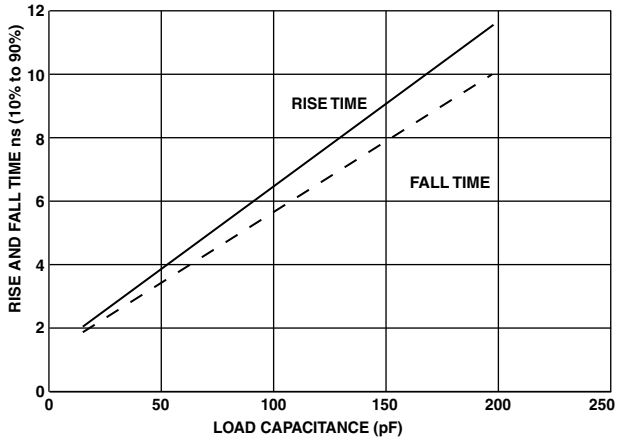


Figure 50. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 3.65 V

THERMAL CHARACTERISTICS

To determine the junction temperature on the application printed circuit board, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C).

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 38 through Table 40.

P_D = Power dissipation (see the power dissipation discussion and the tables on 23 for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature (°C).

In Table 38 through Table 40, airflow measurements comply with JEDEC standards JESD51–2 and JESD51–6, and the junction-to-board measurement complies with JESD51–8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Thermal resistance θ_{JA} in Table 38 through Table 40 is the figure of merit relating to performance of the package and board in a convective environment. θ_{JMA} represents the thermal resistance under two conditions of airflow. Ψ_{JT} represents the correlation between T_J and T_{CASE}.

Table 38. Thermal Characteristics for BC-160 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	27.1	°C/W
θ_{JMA}	1 Linear m/s Airflow	23.85	°C/W
θ_{JMA}	2 Linear m/s Airflow	22.7	°C/W
θ_{JC}	Not Applicable	7.26	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.14	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.26	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.35	°C/W

Table 39. Thermal Characteristics for ST-176-1 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	34.9	°C/W
θ_{JMA}	1 Linear m/s Airflow	33.0	°C/W
θ_{JMA}	2 Linear m/s Airflow	32.0	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.50	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.75	°C/W
Ψ_{JT}	2 Linear m/s Airflow	1.00	°C/W

Table 40. Thermal Characteristics for B-169 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	22.8	°C/W
θ_{JMA}	1 Linear m/s Airflow	20.3	°C/W
θ_{JMA}	2 Linear m/s Airflow	19.3	°C/W
θ_{JC}	Not Applicable	10.39	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.59	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.88	°C/W
Ψ_{JT}	2 Linear m/s Airflow	1.37	°C/W

160-BALL CSP_BGA BALL ASSIGNMENT

Table 41 lists the CSP_BGA ball assignment by signal. Table 42 on Page 51 lists the CSP_BGA ball assignment by ball number.

Table 41. 160-Ball CSP_BGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{ABE0}$	H13	DATA4	N8	GND	L6	SCK	D1
$\overline{ABE1}$	H12	DATA5	P8	GND	L8	SCKE	B13
ADDR1	J14	DATA6	M7	GND	L10	$\overline{SMS}$	C13
ADDR2	K14	DATA7	N7	GND	M4	$\overline{SRAS}$	D13
ADDR3	L14	DATA8	P7	GND	M10	$\overline{SWE}$	D12
ADDR4	J13	DATA9	M6	GND	P14	TCK	P2
ADDR5	K13	DATA10	N6	MISO	E2	TDI	M3
ADDR6	L13	DATA11	P6	MOSI	D3	TDO	N3
ADDR7	K12	DATA12	M5	NMI	B10	TFS0	H3
ADDR8	L12	DATA13	N5	PF0	D2	TFS1	E1
ADDR9	M12	DATA14	P5	PF1	C1	TMR0	L2
ADDR10	M13	DATA15	P4	PF2	C2	TMR1	M1
ADDR11	M14	DR0PRI	K1	PF3	C3	TMR2	K2
ADDR12	N14	DR0SEC	J2	PF4	B1	TMS	N2
ADDR13	N13	DR1PRI	G3	PF5	B2	$\overline{TRST}$	N1
ADDR14	N12	DR1SEC	F3	PF6	B3	TSCLK0	J1
ADDR15	M11	DT0PRI	H1	PF7	B4	TSCLK1	F1
ADDR16	N11	DT0SEC	H2	PF8	A2	TX	K3
ADDR17	P13	DT1PRI	F2	PF9	A3	V_{DDEXT}	A1
ADDR18	P12	DT1SEC	E3	PF10	A4	V_{DDEXT}	C7
ADDR19	P11	$\overline{EMU}$	M2	PF11	A5	V_{DDEXT}	C12
$\overline{AMS0}$	E14	GND	A10	PF12	B5	V_{DDEXT}	D5
$\overline{AMS1}$	F14	GND	A14	PF13	B6	V_{DDEXT}	D9
$\overline{AMS2}$	F13	GND	B11	PF14	A6	V_{DDEXT}	F12
$\overline{AMS3}$	G12	GND	C4	PF15	C6	V_{DDEXT}	G4
$\overline{AOE}$	G13	GND	C5	PPI_CLK	C9	V_{DDEXT}	J4
ARDY	E13	GND	C11	PPI0	C8	V_{DDEXT}	J12
$\overline{ARE}$	G14	GND	D4	PPI1	B8	V_{DDEXT}	L7
$\overline{AWE}$	H14	GND	D7	PPI2	A7	V_{DDEXT}	L11
$\overline{BG}$	P10	GND	D8	PPI3	B7	V_{DDEXT}	P1
$\overline{BGH}$	N10	GND	D10	$\overline{RESET}$	C10	V_{DDINT}	D6
BMODE0	N4	GND	D11	RFS0	J3	V_{DDINT}	E4
BMODE1	P3	GND	F4	RFS1	G2	V_{DDINT}	E11
$\overline{BR}$	D14	GND	F11	RSCLK0	L1	V_{DDINT}	J11
CLKIN	A12	GND	G11	RSCLK1	G1	V_{DDINT}	L4
CLKOUT	B14	GND	H4	RTXI	A9	V_{DDINT}	L9
DATA0	M9	GND	H11	RTXO	A8	V_{DDRTC}	B9
DATA1	N9	GND	K4	RX	L3	VROUT0	A13
DATA2	P9	GND	K11	SA10	E12	VROUT1	B12
DATA3	M8	GND	L5	$\overline{SCAS}$	C14	XTAL	A11

Table 44. 169-Ball PBGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	PF4	D16	CLKOUT	J2	RSCLK1	M12	VDD	U9	DATA9
A2	PF5	D17	$\overline{\text{AMS0}}$	J6	V_{DDEXT}	M16	ADDR7	U10	DATA7
A3	PF7	E1	MOSI	J7	GND	M17	ADDR8	U11	DATA5
A4	PF9	E2	MISO	J8	GND	N1	RFS0	U12	DATA4
A5	PF11	E16	$\overline{\text{AMS1}}$	J9	GND	N2	RSCLK0	U13	DATA2
A6	PF12	E17	$\overline{\text{AMS2}}$	J10	GND	N16	ADDR10	U14	DATA0
A7	PF14	F1	DT1PRI	J11	GND	N17	ADDR9	U15	ADDR16
A8	PPI3	F2	DT1SEC	J12	VDD	P1	TMR2	U16	ADDR18
A9	PPI1	F6	V_{DDEXT}	J16	ADDR1	P2	TMR1	U17	$\overline{\text{BGH}}$
A10	RTXI	F7	V_{DDEXT}	J17	ADDR2	P16	ADDR12		
A11	RTXO	F8	V_{DDEXT}	K1	DT0SEC	P17	ADDR11		
A12	$\overline{\text{RESET}}$	F9	V_{DDEXT}	K2	DT0PRI	R1	TMR0		
A13	XTAL	F10	RTCVDD	K6	V_{DDEXT}	R2	TX		
A14	CLKIN	F11	GND	K7	GND	R16	ADDR14		
A15	$\overline{\text{SRAS}}$	F12	VDD	K8	GND	R17	ADDR13		
A16	$\overline{\text{SCAS}}$	F16	$\overline{\text{AMS3}}$	K9	GND	T1	RX		
A17	$\overline{\text{SMS}}$	F17	$\overline{\text{AOE}}$	K10	GND	T2	V_{DDEXT}		
B1	PF2	G1	TSCLK1	K11	GND	T3	TMS		
B2	V_{DDEXT}	G2	TFS1	K12	VDD	T4	TDO		
B3	PF6	G6	V_{DDEXT}	K16	ADDR3	T5	BMODE1		
B4	PF8	G7	GND	K17	ADDR4	T6	DATA15		
B5	PF10	G8	GND	L1	TFS0	T7	DATA13		
B6	PF13	G9	GND	L2	TSCLK0	T8	DATA10		
B7	PF15	G10	GND	L6	V_{DDEXT}	T9	DATA8		
B8	PPI2	G11	GND	L7	GND	T10	DATA6		
B9	PPI0	G12	VDD	L8	GND	T11	DATA3		
B10	PPI_CLK	G16	$\overline{\text{ARE}}$	L9	GND	T12	DATA1		
B11	NMI	G17	$\overline{\text{AWE}}$	L10	GND	T13	$\overline{\text{BG}}$		
B12	VROUT0	H1	DR1PRI	L11	GND	T14	ADDR19		
B13	VROUT1	H2	DR1SEC	L12	VDD	T15	ADDR17		
B14	SCKE	H6	V_{DDEXT}	L16	ADDR5	T16	GND		
B15	SA10	H7	GND	L17	ADDR6	T17	ADDR15		
B16	GND	H8	GND	M1	DR0SEC	U1	$\overline{\text{EMU}}$		
B17	$\overline{\text{SWE}}$	H9	GND	M2	DR0PRI	U2	$\overline{\text{TRST}}$		
C1	PF1	H10	GND	M6	V_{DDEXT}	U3	TDI		
C2	PF3	H11	GND	M7	V_{DDEXT}	U4	TCK		
C16	ARDY	H12	VDD	M8	V_{DDEXT}	U5	BMODE0		
C17	$\overline{\text{BR}}$	H16	$\overline{\text{ABE0}}$	M9	GND	U6	DATA14		
D1	SCK	H17	$\overline{\text{ABE1}}$	M10	VDD	U7	DATA12		
D2	PF0	J1	RFS1	M11	VDD	U8	DATA11		

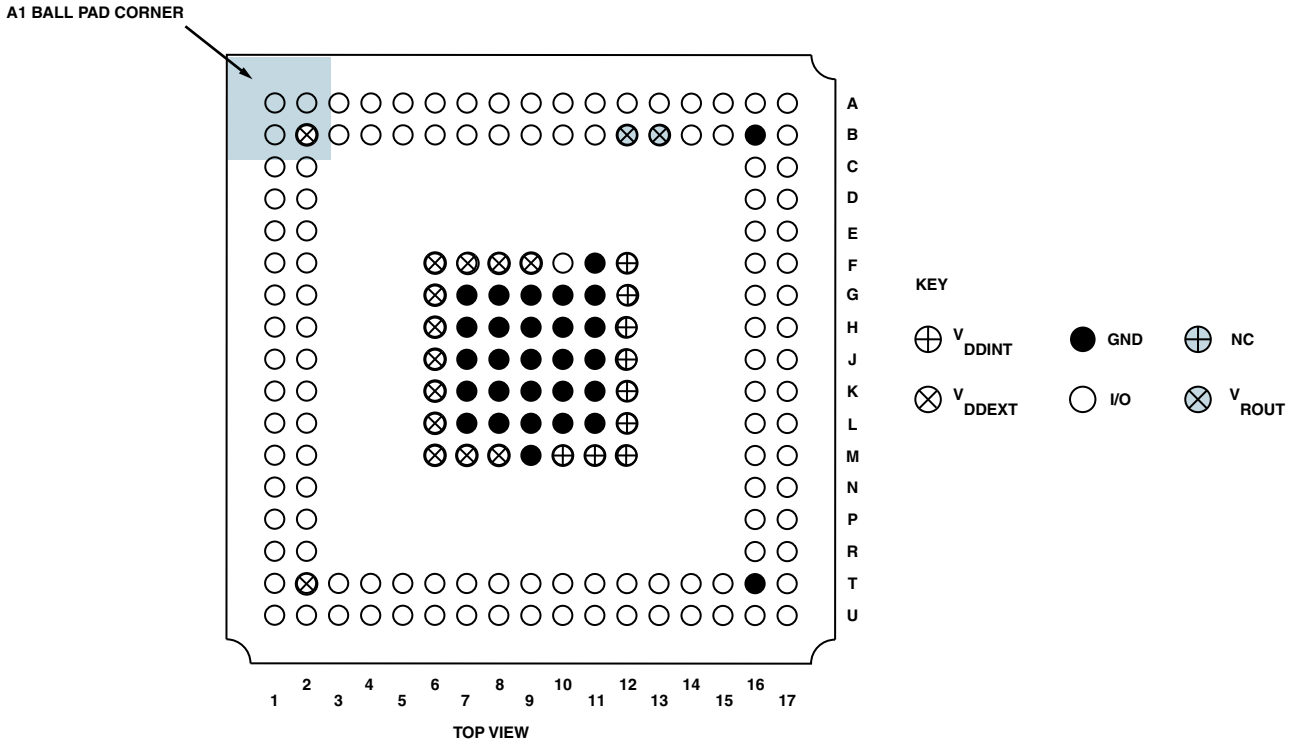


Figure 62. 169-Ball PBGA Ground Configuration (Top View)

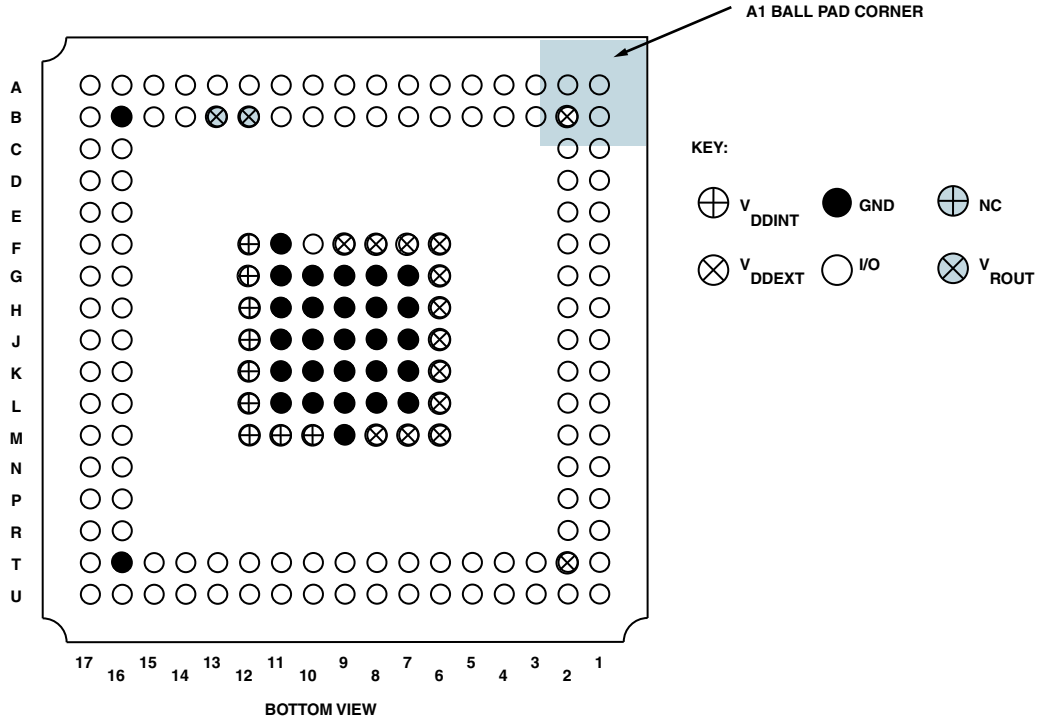
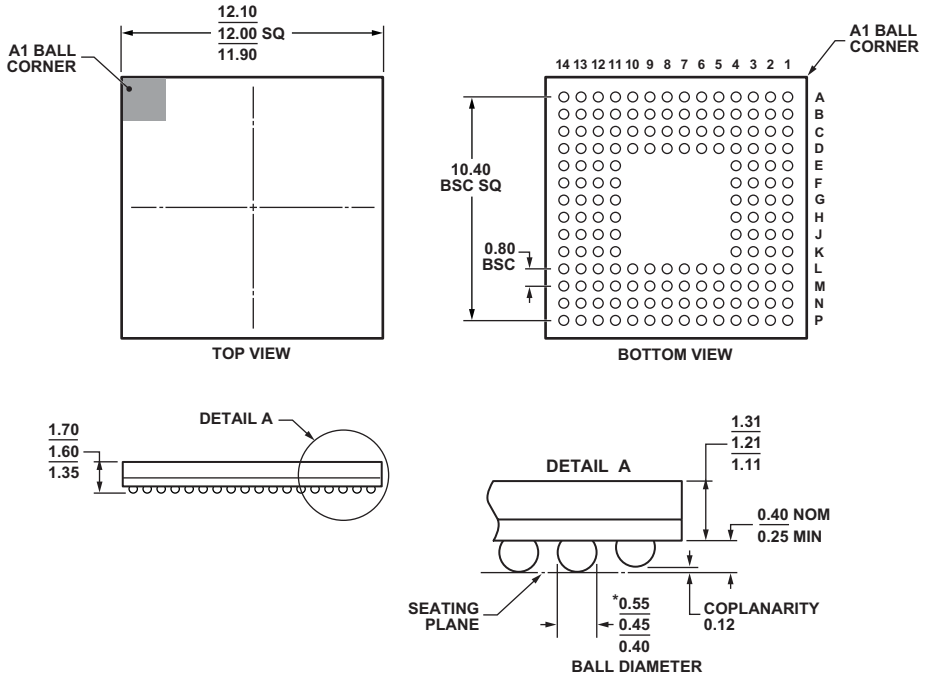


Figure 63. 169-Ball PBGA Ground Configuration (Bottom View)



*COMPLIANT TO JEDEC STANDARDS MO-205-AE WITH THE EXCEPTION TO BALL DIAMETER.

Figure 65. 160-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-160-2)
Dimensions shown in millimeters

AUTOMOTIVE PRODUCTS

The ADBF531W, ADBF532W, and ADBF533W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 48 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 48. Automotive Products

Product Family[1,2]	Temperature Range[3]	Speed Grade (Max)	Package Description	Package Option
ADBF531WBSTZ4xx	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADBF531WBBCZ4xx	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF531WYBCZ4xx	–40°C to +105°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF532WBSTZ4xx	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADBF532WBBCZ4xx	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF532WYBCZ4xx	–40°C to +105°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF533WBBCZ5xx	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADBF533WBBZ5xx	–40°C to +85°C	533 MHz	169-Ball PBGA	B-169
ADBF533WYBCZ4xx	–40°C to +105°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF533WYBBZ4xx	–40°C to +105°C	400 MHz	169-Ball PBGA	B-169

[1] Z = RoHS compliant part.
[2] xx denotes silicon revision.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 20 for junction temperature (T_J) specification which is the only temperature specification.