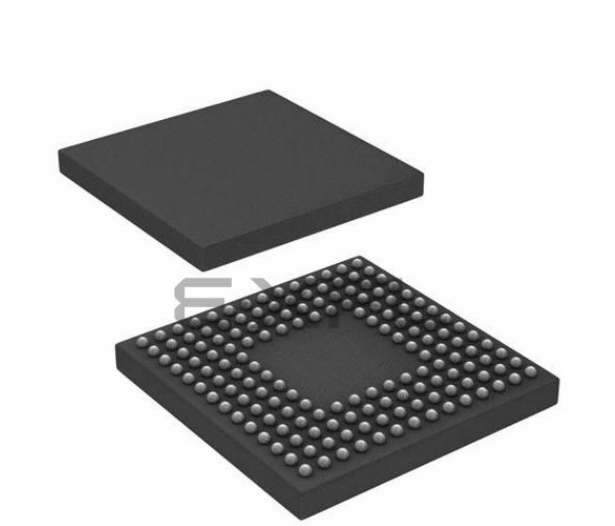

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	400MHz
Non-Volatile Memory	ROM (1kB)
On-Chip RAM	148kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LFBGA, CSPBGA
Supplier Device Package	160-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf533sbbcz400

Each event type has an associated register to hold the return address and an associated return-from-event instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors' event controller consists of two stages, the core event controller (CEC) and the system interrupt controller (SIC). The core event controller works with the system interrupt controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC, and are then routed directly into the general-purpose interrupts of the CEC.

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the processor. Table 2 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

Table 2. Core Event Controller (CEC)

Priority (0 is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	Reset	RST
2	Nonmaskable Interrupt	NMI
3	Exception	EVX
4	Reserved	
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General Interrupt 7	IVG7
8	General Interrupt 8	IVG8
9	General Interrupt 9	IVG9
10	General Interrupt 10	IVG10
11	General Interrupt 11	IVG11
12	General Interrupt 12	IVG12
13	General Interrupt 13	IVG13
14	General Interrupt 14	IVG14
15	General Interrupt 15	IVG15

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processors provide a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). Table 3 describes the inputs into the SIC and the default mappings into the CEC.

Table 3. System Interrupt Controller (SIC)

Peripheral Interrupt Event	Default Mapping
PLL Wakeup	IVG7
DMA Error	IVG7
PPI Error	IVG7
SPORT 0 Error	IVG7
SPORT 1 Error	IVG7
SPI Error	IVG7
UART Error	IVG7
Real-Time Clock	IVG8
DMA Channel 0 (PPI)	IVG8
DMA Channel 1 (SPORT 0 Receive)	IVG9
DMA Channel 2 (SPORT 0 Transmit)	IVG9
DMA Channel 3 (SPORT 1 Receive)	IVG9
DMA Channel 4 (SPORT 1 Transmit)	IVG9
DMA Channel 5 (SPI)	IVG10
DMA Channel 6 (UART Receive)	IVG10
DMA Channel 7 (UART Transmit)	IVG10
Timer 0	IVG11
Timer 1	IVG11
Timer 2	IVG11
Port F GPIO Interrupt A	IVG12
Port F GPIO Interrupt B	IVG12
Memory DMA Stream 0	IVG13
Memory DMA Stream 1	IVG13
Software Watchdog Timer	IVG13

Event Control

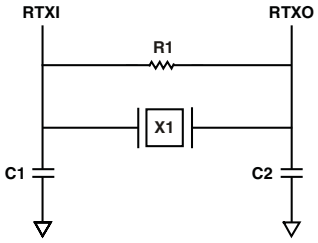
The processors provide a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 32 bits wide:

- CEC interrupt latch register (ILAT) – The ILAT register indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it can also be written to clear (cancel) latched events. This register can be read while in supervisor mode and can only be written while in supervisor mode when the corresponding IMASK bit is cleared.
- CEC interrupt mask register (IMASK) – The IMASK register controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and is processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be latched in the ILAT register. This register can be read or written while in supervisor mode. Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.

The stopwatch function counts down from a programmed value, with one second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like other peripherals, the RTC can wake up the processor from sleep mode upon generation of any RTC wakeup event. Additionally, an RTC wakeup event can wake up the processor from deep sleep mode, and wake up the on-chip internal voltage regulator from a powered-down state.

Connect RTC pins RTXI and RTXO with external components as shown in Figure 6.



SUGGESTED COMPONENTS:
X1 = ECLIPTEK EC38J (THROUGH-HOLE PACKAGE) OR
EPSON MC405 12 pF LOAD (SURFACE-MOUNT PACKAGE)
C1 = 22 pF
C2 = 22 pF
R1 = 10 MΩ

NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

Figure 6. External Components for RTC

WATCHDOG TIMER

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors include a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK), at a maximum frequency of f_{SCLK}.

TIMERS

There are four general-purpose programmable timer units in the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors. Three timers have an external pin that can be configured either as a pulse-width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the PF1 pin (TACLK), an external clock input to the PPI_CLK pin (TMRCLK), or to the internal SCLK.

The timer units can be used in conjunction with the UART to measure the width of the pulses in the data stream to provide an autobaud detect function for a serial channel.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the three general-purpose programmable timers, a fourth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

SERIAL PORTS (SPORTs)

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- I^2S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I^2S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131,070) Hz to (f_{SCLK}/2) Hz.
- Word length – Each SPORT supports serial data words from 3 bits to 32 bits in length, transferred most-significant-bit first or least-significant-bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.

- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data-word or after transferring an entire data buffer or buffers through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1,024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

An additional 250 mV of SPORT input hysteresis can be enabled by setting Bit 15 of the PLL_CTL register. When this bit is set, all SPORT input pins have the increased hysteresis.

SERIAL PERIPHERAL INTERFACE (SPI) PORT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have an SPI-compatible port that enables the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins (master output-slave input, MOSI, and master input-slave output, MISO) and a clock pin (serial clock, SCK). An SPI chip select input pin ($\overline{\text{SPISS}}$) lets other SPI devices select the processor, and seven SPI chip select output pins ($\overline{\text{SPISEL7–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface which supports both master/slave modes and multimaster environments.

The baud rate and clock phase/polarities for the SPI port are programmable, and it has an integrated DMA controller, configurable to support transmit or receive data streams. The SPI DMA controller can only service unidirectional accesses at any given time.

The SPI port clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provide a full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART port includes support for 5 data bits to 8 data bits, 1 stop bit or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The baud rate, serial data format, error code generation and status, and interrupts for the UART port are programmable.

The UART programmable features include:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) bits per second to (f_{SCLK}/16) bits per second.
- Supporting data formats from seven bits to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as:

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16 \times UART\_Divisor}$$

where the 16-bit UART_Divisor comes from the UART_DLH register (most significant 8 bits) and UART_DLL register (least significant 8 bits).

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The capabilities of the UART are further extended with support for the Infrared Data Association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

GENERAL-PURPOSE I/O PORT F

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have 16 bidirectional, general-purpose I/O pins on Port F (PF15–0). Each general-purpose I/O pin can be individually controlled by manipulation of the GPIO control, status and interrupt registers:

- GPIO direction control register – Specifies the direction of each individual PFx pin as input or output.
- GPIO control and status registers – The processor employs a "write one to modify" mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins. Four control registers are provided. One register is written in order to set GPIO pin values, one register is written in order to clear GPIO pin values, one register is written in order to toggle GPIO pin values, and one register is written in order to specify GPIO pin values. Reading the GPIO status register allows software to interrogate the sense of the GPIO pin.
- GPIO interrupt mask registers – The two GPIO interrupt mask registers allow each individual PFx pin to function as an interrupt to the processor. Similar to the two GPIO control registers that are used to set and clear individual GPIO pin values, one GPIO interrupt mask register sets bits to enable interrupt function, and the other GPIO interrupt mask register clears bits to disable interrupt function.

PFx pins defined as inputs can be configured to generate hardware interrupts, while output PFx pins can be triggered by software interrupts.

- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual PFx pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

PARALLEL PERIPHERAL INTERFACE

The processors provide a parallel peripheral interface (PPI) that can connect directly to parallel ADCs and DACs, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bi-directional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bi-directional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications.

Three distinct sub modes are supported:

- Input mode – Frame syncs and data are inputs into the PPI.
- Frame capture mode – Frame syncs are outputs from the PPI, but data are inputs.
- Output mode – Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (e.g., for frame capture). The processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct sub modes are supported:

- Active video only mode
- Vertical blanking only mode
- Entire field mode

Active Video Only Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that can be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

DYNAMIC POWER MANAGEMENT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provides four operating modes, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Power Savings

In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. DMA access is available to appropriately configured L1 memories.

In the active mode, it is possible to disable the PLL through the PLL control register (PLL_CTL). If disabled, the PLL must be re-enabled before it can transition to the full-on or sleep modes.

Table 4. Power Settings

Mode	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)	Internal Power (V_{DDINT})
Full On	Enabled	No	Enabled	Enabled	On
Active	Enabled/ Disabled	Yes	Enabled	Enabled	On
Sleep	Enabled	—	Disabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event or RTC activity will wake up the processor. When in the sleep mode, assertion of wakeup causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor will transition to the full-on mode. If BYPASS is enabled, the processor will transition to the active mode.

When in the sleep mode, system DMA access to L1 memory is not supported.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals, such as the RTC, may still be running but cannot access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. When in deep sleep mode, an RTC asynchronous interrupt causes the processor to transition to the active mode. Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full-on mode.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and to all the synchronous peripherals (SCLK). The internal voltage regulator for the processor can be shut off by writing b#00 to the FREQ bits of the VR_CTL register. In addition to disabling the clocks, this sets the internal power supply voltage (V_{DDINT}) to 0 V to provide the lowest static power dissipation. Any critical information stored internally (memory contents, register contents, etc.) must be written to a nonvolatile storage device prior to removing power if the processor state is to be preserved. Since V_{DDEXT} is still supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current. The internal supply regulator can be woken up either by a real-time clock wakeup or by asserting the $\overline{\text{RESET}}$ pin.

Power Savings

As shown in Table 5, the processors support three different power domains. The use of multiple power domains maximizes flexibility, while maintaining compliance with industry standards and conventions. By isolating the internal logic of the processor into its own power domain, separate from the RTC and other I/O, the processor can take advantage of dynamic power management without affecting the RTC or other I/O devices. There are no sequencing requirements for the various power domains.

Table 5. Power Domains

Power Domain	V_{DD} Range
All internal logic, except RTC	V_{DDINT}
RTC internal logic and crystal I/O	V_{DDRTC}
All other I/O	V_{DDEXT}

The power dissipated by a processor is largely a function of the clock frequency of the processor and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic.

The dynamic power management feature of the processor allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The savings in power dissipation can be modeled using the power savings factor and % power savings calculations.

The power savings factor is calculated as:

$$\textit{power savings factor} = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{t_{RED}}{t_{NOM}}\right)$$

where the variables in the equation are:

$f_{CCLKNOM}$ is the nominal core clock frequency

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage

$V_{DDINTRED}$ is the reduced internal supply voltage

t_{NOM} is the duration running at $f_{CCLKNOM}$

t_{RED} is the duration running at $f_{CCLKRED}$

The percent power savings is calculated as:

$$\%\ power\ savings\ =\ (1 - power\ savings\ factor) \times 100\%$$

VOLTAGE REGULATION

The Blackfin processor provides an on-chip voltage regulator that can generate appropriate V_{DDINT} voltage levels from the V_{DDEXT} supply. See Operating Conditions on Page 20 for regulator tolerances and acceptable V_{DDEXT} ranges for specific models.

Figure 7 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power (V_{DDEXT}) supplied. While in the hibernate state, I/O power is still being applied, eliminating the need for external buffers. The voltage regulator can be activated from this power-down state either through an RTC wakeup or by asserting $\overline{\text{RESET}}$, both of which initiate a boot sequence. The regulator can also be disabled and bypassed at the user's discretion.

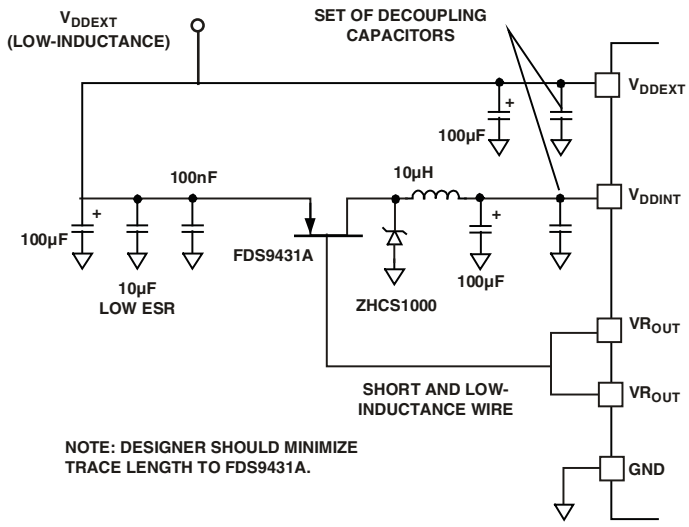


Figure 7. Voltage Regulator Circuit

Voltage Regulator Layout Guidelines

Regulator external component placement, board routing, and bypass capacitors all have a significant effect on noise injected into the other analog circuits on-chip. The VROUT1–0 traces and voltage regulator external components should be considered as noise sources when doing board layout and should not be routed or placed near sensitive circuits or components on the board. All internal and I/O power supplies should be well bypassed with bypass capacitors placed as close to the processors as possible.

For further details on the on-chip voltage regulator and related board design guidelines, see the *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228)* applications note on the Analog Devices web site (www.analog.com)—use site search on "EE-228".

CLOCK SIGNALS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the processors include an on-chip oscillator circuit, an external crystal can be used. For fundamental frequency operation, use the circuit shown in Figure 8.

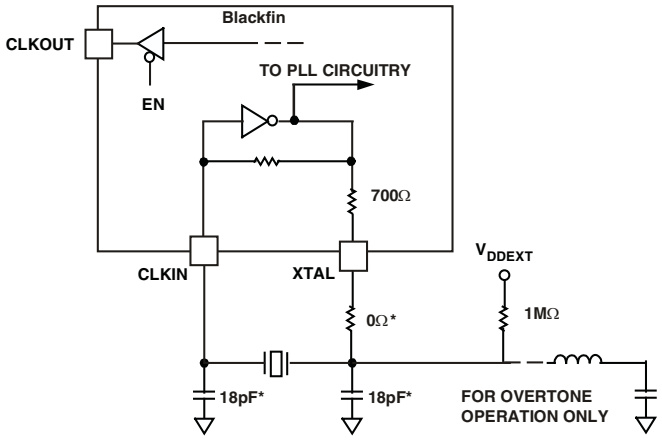


Figure 8. External Crystal Connections

A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor shown in Figure 8 fine tune the phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 8 are typical values only. The capacitor values are dependent upon the crystal manufacturer's load capacitance recommendations and the physical PCB layout. The resistor value depends on the drive level specified by the crystal manufacturer. System designs should verify the customized values based on careful investigation on multiple devices over the allowed temperature range.

A third-overtone crystal can be used at frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 8.

Table 9. Pin Descriptions (Continued)

Pin Name	Type	Function	Driver Type[1]
Port F: GPIO/Parallel Peripheral Interface Port/SPI/Timers			
PF0/*SPISS*	I/O	GPIO/*SPI Slave Select Input*	C
PF1/*SPISEL1*/*TACLK*	I/O	GPIO/*SPI Slave Select Enable 1/Timer Alternate Clock Input*	C
PF2/*SPISEL2*	I/O	GPIO/*SPI Slave Select Enable 2*	C
PF3/*SPISEL3*/*PPI_FS3*	I/O	GPIO/*SPI Slave Select Enable 3/PPI Frame Sync 3*	C
PF4/*SPISEL4*/*PPI15*	I/O	GPIO/*SPI Slave Select Enable 4/PPI 15*	C
PF5/*SPISEL5*/*PPI14*	I/O	GPIO/*SPI Slave Select Enable 5/PPI 14*	C
PF6/*SPISEL6*/*PPI13*	I/O	GPIO/*SPI Slave Select Enable 6/PPI 13*	C
PF7/*SPISEL7*/*PPI12*	I/O	GPIO/*SPI Slave Select Enable 7/PPI 12*	C
PF8/*PPI11*	I/O	GPIO/*PPI 11*	C
PF9/*PPI10*	I/O	GPIO/*PPI 10*	C
PF10/*PPI9*	I/O	GPIO/*PPI 9*	C
PF11/*PPI8*	I/O	GPIO/*PPI 8*	C
PF12/*PPI7*	I/O	GPIO/*PPI 7*	C
PF13/*PPI6*	I/O	GPIO/*PPI 6*	C
PF14/*PPI5*	I/O	GPIO/*PPI 5*	C
PF15/*PPI4*	I/O	GPIO/*PPI 4*	C
JTAG Port			
TCK	I	JTAG Clock	
TDO	O	JTAG Serial Data Out	C
TDI	I	JTAG Serial Data In	
TMS	I	JTAG Mode Select	
$\overline{\text{TRST}}$	I	JTAG Reset (This pin should be pulled low if JTAG is not used.)	
$\overline{\text{EMU}}$	O	Emulation Output	C
SPI Port			
MOSI	I/O	Master Out Slave In	C
MISO	I/O	Master In Slave Out (This pin should be pulled high through a 4.7 kΩ resistor if booting via the SPI port.)	C
SCK	I/O	SPI Clock	D
Serial Ports			
RSCLK0	I/O	SPORT0 Receive Serial Clock	D
RFS0	I/O	SPORT0 Receive Frame Sync	C
DR0PRI	I	SPORT0 Receive Data Primary	
DR0SEC	I	SPORT0 Receive Data Secondary	
TSCLK0	I/O	SPORT0 Transmit Serial Clock	D
TFS0	I/O	SPORT0 Transmit Frame Sync	C
DT0PRI	O	SPORT0 Transmit Data Primary	C
DT0SEC	O	SPORT0 Transmit Data Secondary	C
RSCLK1	I/O	SPORT1 Receive Serial Clock	D

The following three tables describe the voltage/frequency requirements for the processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock (Table 10 and Table 11) and system clock (Table 13) specifications. Table 12 describes phase-locked loop operating conditions.

Table 10. Core Clock (CCLK) Requirements—500 MHz, 533 MHz, and 600 MHz Models

Parameter		Internal Regulator Setting	Max	Unit
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.3 V Minimum)[1]	1.30 V	600	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.2 V Minimum)[2]	1.25 V	533	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.14 V Minimum)[3]	1.20 V	500	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	444	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	400	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V	333	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V	250	MHz

[1] Applies to 600 MHz models only. See Ordering Guide on Page 63.
[2] Applies to 533 MHz and 600 MHz models only. See Ordering Guide on Page 63. 533 MHz models cannot support internal regulator levels above 1.25 V.
[3] Applies to 500 MHz, 533 MHz, and 600 MHz models. See Ordering Guide on Page 63. 500 MHz models cannot support internal regulator levels above 1.20 V.

Table 11. Core Clock (CCLK) Requirements—400 MHz Models[1]

Parameter		Internal Regulator Setting	T_J = 125°C Max	All[2] Other T_J Max	Unit
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	400	400	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	333	364	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	295	333	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V		280	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V		250	MHz

[1] See Ordering Guide on Page 63.
[2] See Operating Conditions on Page 20.

Table 12. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	50	Max f_{CCLK}	MHz

Table 13. System Clock (SCLK) Requirements

Parameter[1]		V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
CSP_BGA/PBGA				
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} \geq$ 1.14 V)	100	133	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.14 V)	100	100	MHz
LQFP				
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} \geq$ 1.14 V)	100	133	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.14 V)	83	83	MHz

[1] t_{SCLK} (= $1/f_{SCLK}$) must be greater than or equal to t_{CCLK}.

Table 31. External Late Frame Sync

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Switching Characteristics								
$t_{DDTLFSE}$	Data Delay from Late External TFSx or External RFSx in multichannel mode with MCMEN = 0[1, 2]		10.5		10.0		10.0	ns
$t_{DTENLFS}$	Data Enable from Late FS or in multichannel mode with MCMEN = 0[1, 2]	0		0		0		ns

[1] In multichannel mode, TFSx enable and TFSx valid follow $t_{DTENLFS}$ and $t_{DDTLFSE}$.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$, then $t_{DDTTE/I}$ and $t_{DTENE/I}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

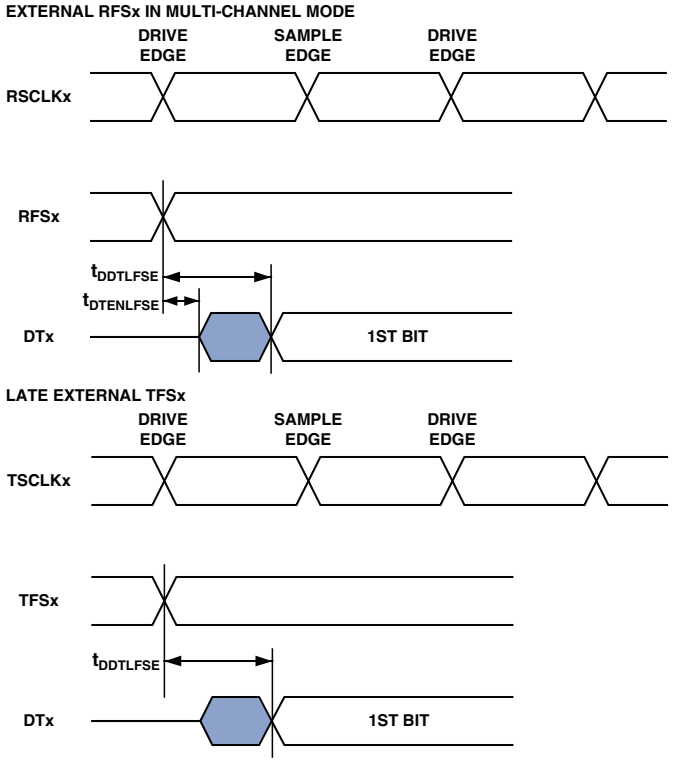


Figure 26. External Late Frame Sync

Serial Peripheral Interface (SPI) Port—Master Timing

Table 32. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Timing Requirements								
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	10.5		9		7.5		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	–1.5		–1.5		–1.5		ns
Switching Characteristics								
t_{SDSCIM}	$\overline{SPISELx}$ Low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISELx}$ High	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)		6		6		6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	–1.0		–1.0		–1.0		ns

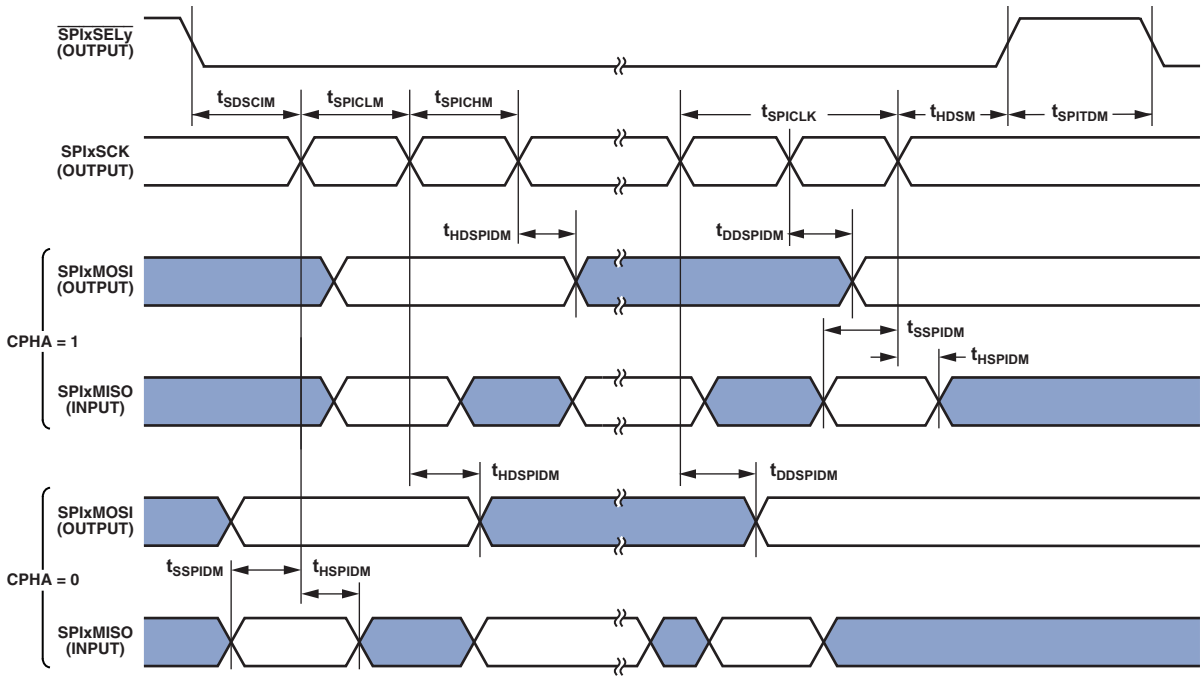


Figure 27. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 33. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Timing Requirements								
t_{SPICHS}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK}$		$4 \times t_{SCLK}$		$4 \times t_{SCLK}$		ns
t_{HDS}	Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{SPISS}$ Assertion to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		1.6		1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	1.6		1.6		1.6		ns
Switching Characteristics								
t_{DSOE}	$\overline{SPISS}$ Assertion to Data Out Active	0	10	0	9	0	8	ns
t_{DSDHI}	$\overline{SPISS}$ Deassertion to Data High Impedance	0	10	0	9	0	8	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)		10		10		10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0		0		0		ns

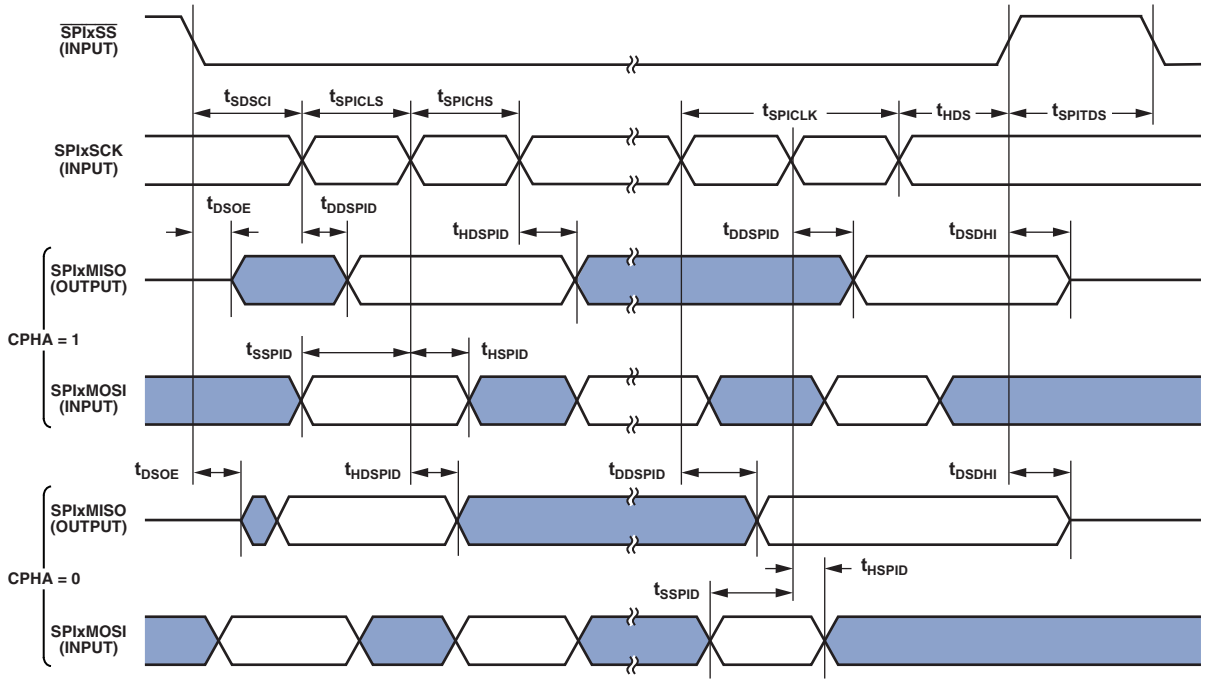


Figure 28. Serial Peripheral Interface (SPI) Port—Slave Timing

THERMAL CHARACTERISTICS

To determine the junction temperature on the application printed circuit board, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C).

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 38 through Table 40.

P_D = Power dissipation (see the power dissipation discussion and the tables on 23 for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature (°C).

In Table 38 through Table 40, airflow measurements comply with JEDEC standards JESD51–2 and JESD51–6, and the junction-to-board measurement complies with JESD51–8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Thermal resistance θ_{JA} in Table 38 through Table 40 is the figure of merit relating to performance of the package and board in a convective environment. θ_{JMA} represents the thermal resistance under two conditions of airflow. Ψ_{JT} represents the correlation between T_J and T_{CASE}.

Table 38. Thermal Characteristics for BC-160 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	27.1	°C/W
θ_{JMA}	1 Linear m/s Airflow	23.85	°C/W
θ_{JMA}	2 Linear m/s Airflow	22.7	°C/W
θ_{JC}	Not Applicable	7.26	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.14	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.26	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.35	°C/W

Table 39. Thermal Characteristics for ST-176-1 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	34.9	°C/W
θ_{JMA}	1 Linear m/s Airflow	33.0	°C/W
θ_{JMA}	2 Linear m/s Airflow	32.0	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.50	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.75	°C/W
Ψ_{JT}	2 Linear m/s Airflow	1.00	°C/W

Table 40. Thermal Characteristics for B-169 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	22.8	°C/W
θ_{JMA}	1 Linear m/s Airflow	20.3	°C/W
θ_{JMA}	2 Linear m/s Airflow	19.3	°C/W
θ_{JC}	Not Applicable	10.39	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.59	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.88	°C/W
Ψ_{JT}	2 Linear m/s Airflow	1.37	°C/W

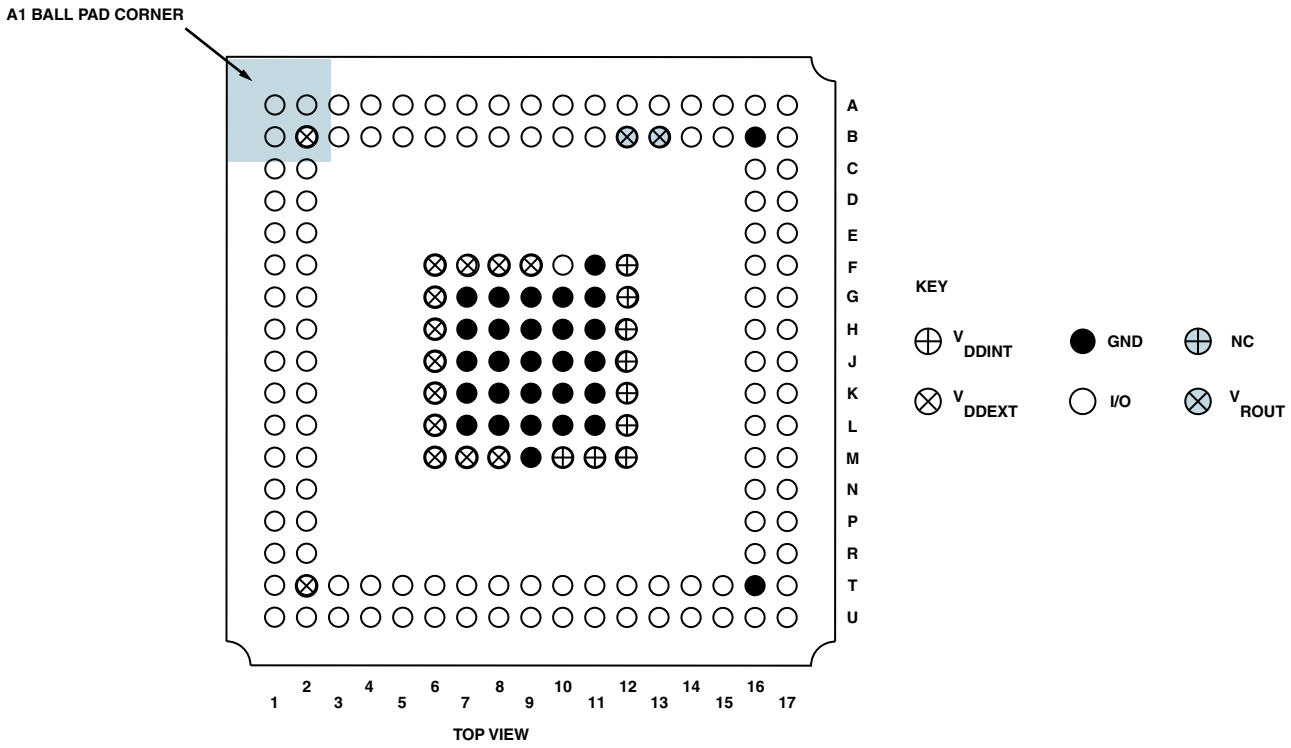


Figure 62. 169-Ball PBGA Ground Configuration (Top View)

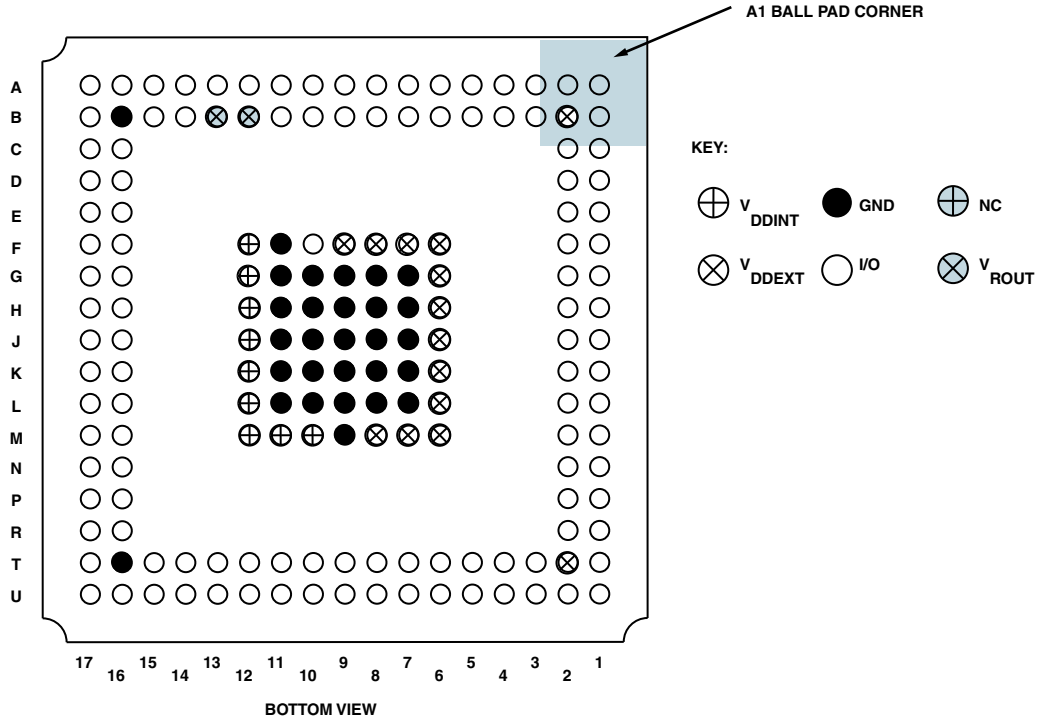


Figure 63. 169-Ball PBGA Ground Configuration (Bottom View)

Table 46. 176-Lead LQFP Pin Assignment (Numerical by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	GND	41	GND	81	TX	121	ADDR19	161	$\overline{AMS0}$
2	GND	42	GND	82	RX	122	ADDR18	162	ARDY
3	GND	43	GND	83	$\overline{EMU}$	123	ADDR17	163	$\overline{BR}$
4	VROUT1	44	GND	84	$\overline{TRST}$	124	ADDR16	164	SA10
5	VROUT0	45	V_{DDEXT}	85	TMS	125	ADDR15	165	$\overline{SWE}$
6	V_{DDEXT}	46	PF5	86	TDI	126	ADDR14	166	$\overline{SCAS}$
7	GND	47	PF4	87	TDO	127	ADDR13	167	$\overline{SRAS}$
8	GND	48	PF3	88	GND	128	GND	168	V_{DDINT}
9	GND	49	PF2	89	GND	129	GND	169	CLKOUT
10	CLKIN	50	PF1	90	GND	130	GND	170	GND
11	XTAL	51	PF0	91	GND	131	GND	171	V_{DDEXT}
12	V_{DDEXT}	52	V_{DDINT}	92	GND	132	GND	172	$\overline{SMS}$
13	$\overline{RESET}$	53	SCK	93	V_{DDEXT}	133	GND	173	SCKE
14	NMI	54	MISO	94	TCK	134	V_{DDEXT}	174	GND
15	GND	55	MOSI	95	BMODE1	135	ADDR12	175	GND
16	RTXO	56	GND	96	BMODE0	136	ADDR11	176	GND
17	RTXI	57	V_{DDEXT}	97	GND	137	ADDR10		
18	V_{DDRTC}	58	DT1SEC	98	DATA15	138	ADDR9		
19	GND	59	DT1PRI	99	DATA14	139	ADDR8		
20	V_{DDEXT}	60	TFS1	100	DATA13	140	ADDR7		
21	PPI_CLK	61	TSCLK1	101	DATA12	141	ADDR6		
22	PPI0	62	DR1SEC	102	DATA11	142	ADDR5		
23	PPI1	63	DR1PRI	103	DATA10	143	V_{DDINT}		
24	PPI2	64	RFS1	104	DATA9	144	GND		
25	V_{DDINT}	65	RSCLK1	105	DATA8	145	V_{DDEXT}		
26	PPI3	66	V_{DDINT}	106	GND	146	ADDR4		
27	PF15	67	DT0SEC	107	V_{DDEXT}	147	ADDR3		
28	PF14	68	DT0PRI	108	DATA7	148	ADDR2		
29	PF13	69	TFS0	109	DATA6	149	ADDR1		
30	GND	70	GND	110	DATA5	150	$\overline{ABE1}$		
31	V_{DDEXT}	71	V_{DDEXT}	111	V_{DDINT}	151	$\overline{ABE0}$		
32	PF12	72	TSCLK0	112	DATA4	152	$\overline{AWE}$		
33	PF11	73	DR0SEC	113	DATA3	153	$\overline{ARE}$		
34	PF10	74	DR0PRI	114	DATA2	154	$\overline{AOE}$		
35	PF9	75	RFS0	115	DATA1	155	GND		
36	PF8	76	RSCLK0	116	DATA0	156	V_{DDEXT}		
37	PF7	77	TMR2	117	GND	157	V_{DDINT}		
38	PF6	78	TMR1	118	V_{DDEXT}	158	$\overline{AMS3}$		
39	GND	79	TMR0	119	$\overline{BG}$	159	$\overline{AMS2}$		
40	GND	80	V_{DDINT}	120	$\overline{BGH}$	160	$\overline{AMS1}$		

OUTLINE DIMENSIONS

Dimensions in the outline dimension figures are shown in millimeters.

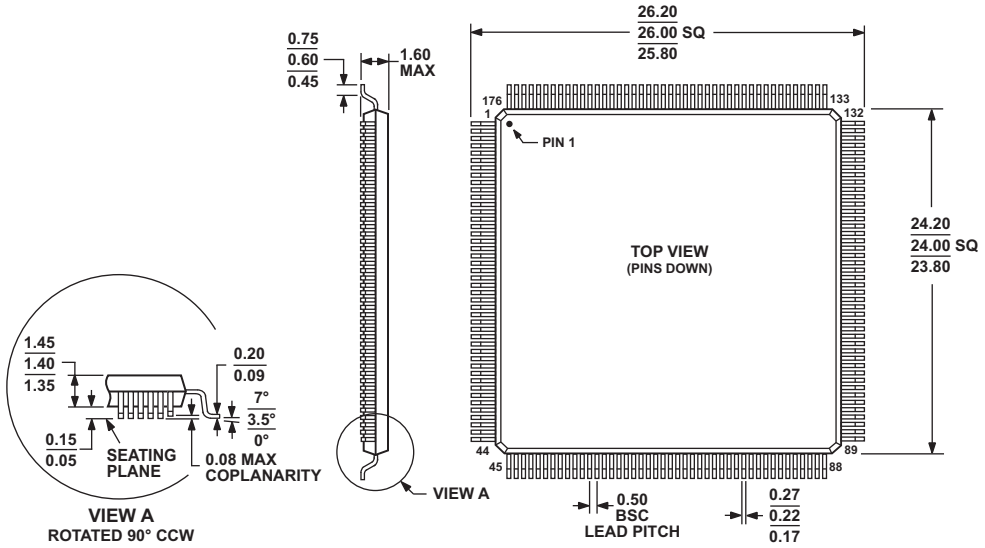
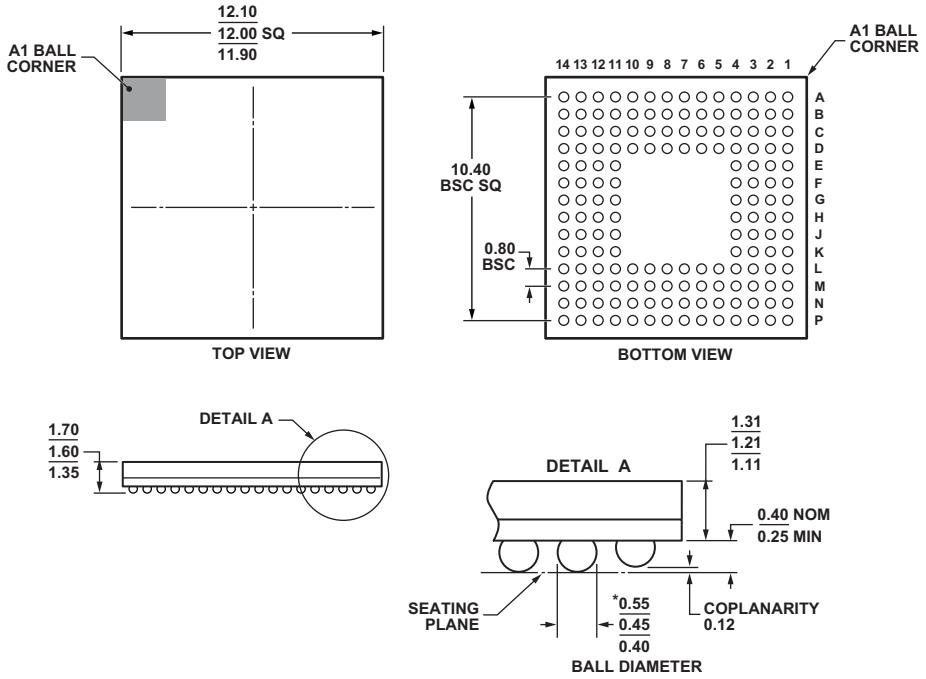


Figure 64. 176-Lead Low Profile Quad Flat Package [LQFP]
(ST-176-1)
Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-205-AE WITH THE EXCEPTION TO BALL DIAMETER.

Figure 65. 160-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-160-2)
Dimensions shown in millimeters

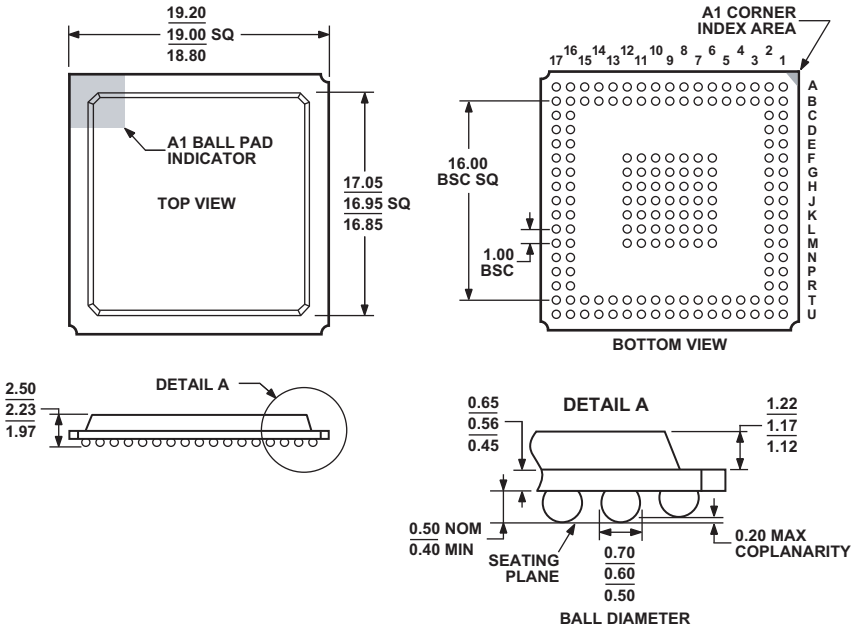


Figure 66. 169-Ball Plastic Ball Grid Array [PBGA]
(B-169)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 47 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 47. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
Chip Scale Package Ball Grid Array (CSP_BGA) BC-160-2	Solder Mask Defined	0.40 mm diameter	0.55 mm diameter
Plastic Ball Grid Array (PBGA) B-169	Solder Mask Defined	0.43 mm diameter	0.56 mm diameter

AUTOMOTIVE PRODUCTS

The ADBF531W, ADBF532W, and ADBF533W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 48 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 48. Automotive Products

Product Family[1,2]	Temperature Range[3]	Speed Grade (Max)	Package Description	Package Option
ADBF531WBSTZ4xx	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADBF531WBBCZ4xx	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF531WYBCZ4xx	–40°C to +105°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF532WBSTZ4xx	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADBF532WBBCZ4xx	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF532WYBCZ4xx	–40°C to +105°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF533WBBCZ5xx	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADBF533WBBZ5xx	–40°C to +85°C	533 MHz	169-Ball PBGA	B-169
ADBF533WYBCZ4xx	–40°C to +105°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF533WYBBZ4xx	–40°C to +105°C	400 MHz	169-Ball PBGA	B-169

[1] Z = RoHS compliant part.
[2] xx denotes silicon revision.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 20 for junction temperature (T_J) specification which is the only temperature specification.

ORDERING GUIDE

Model [1]	Temperature Range [2]	Speed Grade (Max)	Package Description	Package Option
ADSP-BF531SBB400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF531SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF531SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF531SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF531SBBCZ4RL	–40°C to +85°C	400 MHz	160-Ball CSP_BGA, 13" Tape and Reel	BC-160-2
ADSP-BF531SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF532SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF532SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF532SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF532SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF533SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF533SBB500	–40°C to +85°C	500 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBZ500	–40°C to +85°C	500 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBC500	–40°C to +85°C	500 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ500	–40°C to +85°C	500 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBC-5V	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ-5V	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKBC-6V	0°C to +70°C	600 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKBCZ-6V	0°C to +70°C	600 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKSTZ-5V	0°C to +70°C	533 MHz	176-Lead LQFP	ST-176-1

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 20 for junction temperature (T_J) specification which is the only temperature specification.