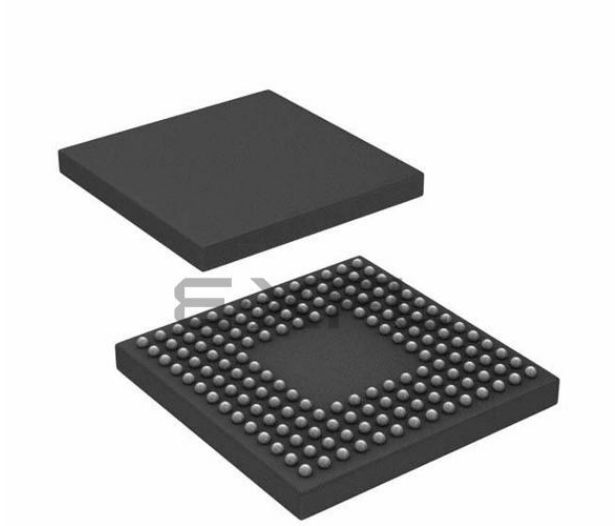

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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Active |
| Type | Fixed Point |
| Interface | SPI, SSP, UART |
| Clock Rate | 500MHz |
| Non-Volatile Memory | ROM (1kB) |
| On-Chip RAM | 148kB |
| Voltage - I/O | 3.30V |
| Voltage - Core | 1.20V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 160-LFBGA, CSPBGA |
| Supplier Device Package | 160-CSPBGA (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/adsp-bf533sbbcz500 |

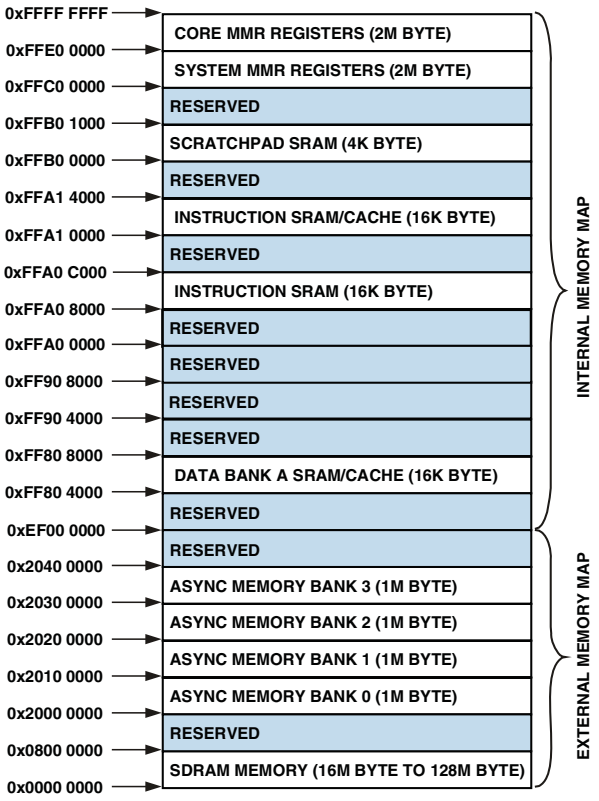



*Figure 3. ADSP-BF531 Internal/External Memory Map*

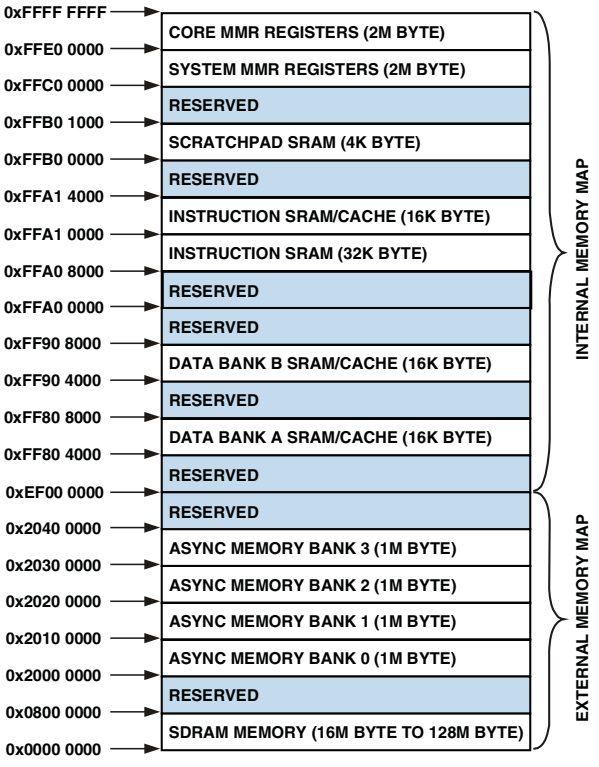



*Figure 4. ADSP-BF532 Internal/External Memory Map*

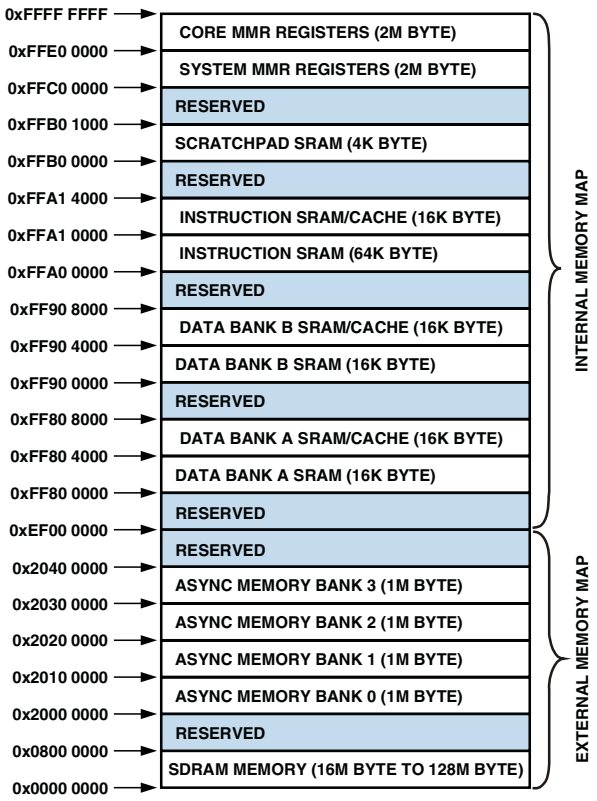



*Figure 5. ADSP-BF533 Internal/External Memory Map*

### *Event Handling*

The event controller on the processors handle all asynchronous and synchronous events to the processor. The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provide event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher priority event takes precedence over servicing of a lower priority event. The controller provides support for five different types of events:

- Emulation – An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- Reset – This event resets the processor.
- Nonmaskable Interrupt (NMI) – The NMI event can be generated by the software watchdog timer or by the NMI input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- Exceptions – Events that occur synchronously to program flow (i.e., the exception is taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts – Events that occur asynchronously to program flow. They are caused by input pins, timers, and other peripherals, as well as by an explicit software instruction.

Each event type has an associated register to hold the return address and an associated return-from-event instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors' event controller consists of two stages, the core event controller (CEC) and the system interrupt controller (SIC). The core event controller works with the system interrupt controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC, and are then routed directly into the general-purpose interrupts of the CEC.

### *Core Event Controller (CEC)*

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the processor. Table 2 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

**Table 2. Core Event Controller (CEC)**

| Priority (0 is Highest) | Event Class | EVT Entry |
|---|---|---|
| 0 | Emulation/Test Control | EMU |
| 1 | Reset | RST |
| 2 | Nonmaskable Interrupt | NMI |
| 3 | Exception | EVX |
| 4 | Reserved | |
| 5 | Hardware Error | IVHW |
| 6 | Core Timer | IVTMR |
| 7 | General Interrupt 7 | IVG7 |
| 8 | General Interrupt 8 | IVG8 |
| 9 | General Interrupt 9 | IVG9 |
| 10 | General Interrupt 10 | IVG10 |
| 11 | General Interrupt 11 | IVG11 |
| 12 | General Interrupt 12 | IVG12 |
| 13 | General Interrupt 13 | IVG13 |
| 14 | General Interrupt 14 | IVG14 |
| 15 | General Interrupt 15 | IVG15 |

### *System Interrupt Controller (SIC)*

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processors provide a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). Table 3 describes the inputs into the SIC and the default mappings into the CEC.

**Table 3. System Interrupt Controller (SIC)**

| Peripheral Interrupt Event | Default Mapping |
|---|---|
| PLL Wakeup | IVG7 |
| DMA Error | IVG7 |
| PPI Error | IVG7 |
| SPORT 0 Error | IVG7 |
| SPORT 1 Error | IVG7 |
| SPI Error | IVG7 |
| UART Error | IVG7 |
| Real-Time Clock | IVG8 |
| DMA Channel 0 (PPI) | IVG8 |
| DMA Channel 1 (SPORT 0 Receive) | IVG9 |
| DMA Channel 2 (SPORT 0 Transmit) | IVG9 |
| DMA Channel 3 (SPORT 1 Receive) | IVG9 |
| DMA Channel 4 (SPORT 1 Transmit) | IVG9 |
| DMA Channel 5 (SPI) | IVG10 |
| DMA Channel 6 (UART Receive) | IVG10 |
| DMA Channel 7 (UART Transmit) | IVG10 |
| Timer 0 | IVG11 |
| Timer 1 | IVG11 |
| Timer 2 | IVG11 |
| Port F GPIO Interrupt A | IVG12 |
| Port F GPIO Interrupt B | IVG12 |
| Memory DMA Stream 0 | IVG13 |
| Memory DMA Stream 1 | IVG13 |
| Software Watchdog Timer | IVG13 |

### *Event Control*

The processors provide a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 32 bits wide:

- CEC interrupt latch register (ILAT) – The ILAT register indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it can also be written to clear (cancel) latched events. This register can be read while in supervisor mode and can only be written while in supervisor mode when the corresponding IMASK bit is cleared.
- CEC interrupt mask register (IMASK) – The IMASK register controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and is processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be latched in the ILAT register. This register can be read or written while in supervisor mode. Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.

- CEC interrupt pending register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but can be read while in supervisor mode.

The SIC allows further control of event processing by providing three 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in Table 3.

- SIC interrupt mask register (SIC_IMASK) – This register controls the masking and unmasking of each peripheral interrupt event. When a bit is set in this register, that peripheral event is unmasked and is processed by the system when asserted. A cleared bit in this register masks the peripheral event, preventing the processor from servicing the event.
- SIC interrupt status register (SIC_ISR) – As multiple peripherals can be mapped to a single event, this register allows the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt, and a cleared bit indicates the peripheral is not asserting the event.
- SIC interrupt wakeup enable register (SIC_IWR) – By enabling the corresponding bit in this register, a peripheral can be configured to wake up the processor, should the core be idled when the event is generated. See Dynamic Power Management on Page 11.

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC recognizes and queues the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

## DMA CONTROLLERS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have multiple, independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the SPORTs, SPI port, UART, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The DMA controller supports both 1-dimensional (1-D) and 2-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, autorefreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two pairs of memory DMA channels provided for transfers between the various memories of the processor system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

## REAL-TIME CLOCK

The processor real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors. The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

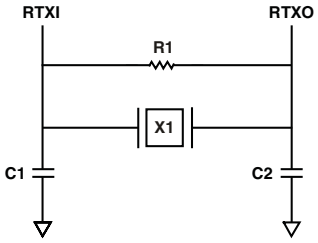
The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60 second counter, a 60 minute counter, a 24 hour counter, and a 32,768 day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. The two alarms are time of day and a day and time of that day.

The stopwatch function counts down from a programmed value, with one second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like other peripherals, the RTC can wake up the processor from sleep mode upon generation of any RTC wakeup event. Additionally, an RTC wakeup event can wake up the processor from deep sleep mode, and wake up the on-chip internal voltage regulator from a powered-down state.

Connect RTC pins RTXI and RTXO with external components as shown in Figure 6.




SUGGESTED COMPONENTS:
X1 = ECLIPTEK EC38J (THROUGH-HOLE PACKAGE) OR
EPSON MC405 12 pF LOAD (SURFACE-MOUNT PACKAGE)
C1 = 22 pF
C2 = 22 pF
R1 = 10 MΩ

NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

*Figure 6. External Components for RTC*

## WATCHDOG TIMER

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors include a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK), at a maximum frequency of $f_{SCLK}$.

## TIMERS

There are four general-purpose programmable timer units in the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors. Three timers have an external pin that can be configured either as a pulse-width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the PF1 pin (TACLK), an external clock input to the PPI_CLK pin (TMRCLK), or to the internal SCLK.

The timer units can be used in conjunction with the UART to measure the width of the pulses in the data stream to provide an autobaud detect function for a serial channel.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the three general-purpose programmable timers, a fourth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

## SERIAL PORTS (SPORTs)

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- $I^2S$ capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of $I^2S$ stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from ($f_{SCLK}$/131,070) Hz to ($f_{SCLK}$/2) Hz.
- Word length – Each SPORT supports serial data words from 3 bits to 32 bits in length, transferred most-significant-bit first or least-significant-bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.

As shown in Figure 9, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a user programmable 0.5× to 64× multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 10×, but it can be modified by a software instruction sequence. On-the-fly frequency changes can be effected by simply writing to the PLL_DIV register.

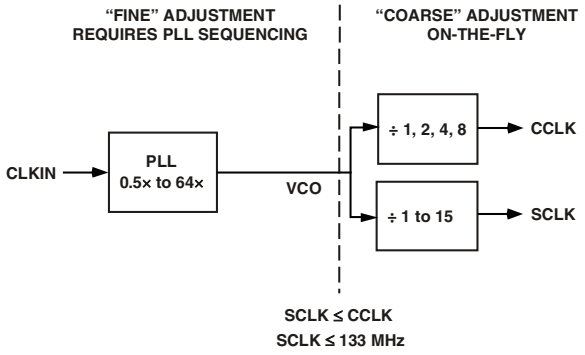



*Figure 9. Frequency Modification Methods*

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 6 illustrates typical system clock ratios.

**Table 6. Example System Clock Ratios**

| Signal Name SSEL3–0 | Divider Ratio VCO/SCLK | Example Frequency Ratios (MHz) | |
|---|---|---|---|
| | | VCO | SCLK |
| 0001 | 1:1 | 100 | 100 |
| 0101 | 5:1 | 400 | 80 |
| 1010 | 10:1 | 500 | 50 |

The maximum frequency of the system clock is $f_{SCLK}$. The divisor ratio must be chosen to limit the system clock frequency to its maximum of $f_{SCLK}$. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV). When the SSEL value is changed, it affects all of the peripherals that derive their clock signals from the SCLK signal.

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 7. This programmable core clock capability is useful for fast core frequency modifications.

**Table 7. Core Clock Ratios**

| Signal Name CSEL1–0 | Divider Ratio VCO/CCLK | Example Frequency Ratios (MHz) | |
|---|---|---|---|
| | | VCO | CCLK |
| 00 | 1:1 | 300 | 300 |
| 01 | 2:1 | 300 | 150 |
| 10 | 4:1 | 400 | 100 |
| 11 | 8:1 | 200 | 25 |

## BOOTING MODES

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have two mechanisms (listed in Table 8) for automatically loading internal L1 instruction memory after a reset. A third mode is provided to execute from external memory, bypassing the boot sequence.

**Table 8. Booting Modes**

| BMODE1–0 | Description |
|---|---|
| 00 | Execute from 16-bit external memory (bypass boot ROM) |
| 01 | Boot from 8-bit or 16-bit FLASH |
| 10 | Boot from serial master connected to SPI |
| 11 | Boot from serial slave EEPROM/flash (8-,16-, or 24-bit address range, or Atmel AT45DB041, AT45DB081, or AT45DB161serial flash) |

The BMODE pins of the reset configuration register, sampled during power-on resets and software-initiated resets, implement the following modes:

- Execute from 16-bit external memory – Execution starts from address 0x2000 0000 with 16-bit packing. The boot ROM is bypassed in this mode. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).
- Boot from 8-bit or 16-bit external flash memory – The flash boot routine located in boot ROM memory space is set up using asynchronous Memory Bank 0. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).
- Boot from SPI serial EEPROM/flash (8-, 16-, or 24-bit addressable, or Atmel AT45DB041, AT45DB081, or AT45DB161) – The SPI uses the PF2 output pin to select a single SPI EEPROM/flash device, submits a read command and successive address bytes (0x00) until a valid 8-, 16-, or 24-bit addressable EEPROM/flash device is detected, and begins clocking data into the processor at the beginning of L1 instruction memory.
- Boot from SPI serial master – The Blackfin processor operates in SPI slave mode and is configured to receive the bytes of the LDR file from an SPI host (master) agent. To hold off the host device from transmitting while the boot ROM is busy, the Blackfin processor asserts a GPIO pin, called host wait (HWAIT), to signal the host device not to send any

# SPECIFICATIONS

Component specifications are subject to change without notice.

## OPERATING CONDITIONS

| Parameter | | Conditions | Min | Nominal | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDINT}$ | Internal Supply Voltage[1] | Nonautomotive 400 MHz and 500 MHz speed grade models[2] | 0.8 | 1.2 | 1.45 | V |
| $V_{DDINT}$ | Internal Supply Voltage[1] | Nonautomotive 533 MHz speed grade models[2] | 0.8 | 1.25 | 1.45 | V |
| $V_{DDINT}$ | Internal Supply Voltage[1] | 600 MHz speed grade models[2] | 0.8 | 1.30 | 1.45 | V |
| $V_{DDINT}$ | Internal Supply Voltage[1] | Automotive 400 MHz speed grade models[2] | 0.95 | 1.2 | 1.45 | V |
| $V_{DDINT}$ | Internal Supply Voltage[1] | Automotive 533 MHz speed grade models[2] | 0.95 | 1.25 | 1.45 | V |
| $V_{DDEXT}$ | External Supply Voltage[3] | Nonautomotive grade models[2] | 1.75 | 1.8/3.3 | 3.6 | V |
| $V_{DDEXT}$ | External Supply Voltage | Automotive grade models[2] | 2.7 | 3.3 | 3.6 | V |
| $V_{DDRTC}$ | Real-Time Clock Power Supply Voltage | Nonautomotive grade models[2] | 1.75 | 1.8/3.3 | 3.6 | V |
| $V_{DDRTC}$ | Real-Time Clock Power Supply Voltage | Automotive grade models[2] | 2.7 | 3.3 | 3.6 | V |
| $V_{IH}$ | High Level Input Voltage[4, 5] | $V_{DDEXT}$ = 1.85 V | 1.3 | | | V |
| $V_{IH}$ | High Level Input Voltage[4, 5] | $V_{DDEXT}$ = Maximum | 2.0 | | | V |
| $V_{IHCLKIN}$ | High Level Input Voltage[6] | $V_{DDEXT}$ = Maximum | 2.2 | | | V |
| $V_{IL}$ | Low Level Input Voltage[7] | $V_{DDEXT}$ = 1.75 V | | | +0.3 | V |
| $V_{IL}$ | Low Level Input Voltage[7] | $V_{DDEXT}$ = 2.7 V | | | +0.6 | V |
| $T_J$ | Junction Temperature | 160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = 0°C to +70°C | 0 | | +95 | °C |
| $T_J$ | Junction Temperature | 160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +85°C | –40 | | +105 | °C |
| $T_J$ | Junction Temperature | 160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +105°C | –40 | | +125 | °C |
| $T_J$ | Junction Temperature | 169-Ball Plastic Ball Grid Array (PBGA) @ $T_{AMBIENT}$ = –40°C to +105°C | –40 | | +125 | °C |
| $T_J$ | Junction Temperature | 169-Ball Plastic Ball Grid Array (PBGA) @ $T_{AMBIENT}$ = –40°C to +85°C | –40 | | +105 | °C |
| $T_J$ | Junction Temperature | 176-Lead Quad Flatpack (LQFP) @ $T_{AMBIENT}$ = –40°C to +85°C | –40 | | +100 | °C |

[1] The regulator can generate $V_{DDINT}$ at levels of 0.85 V to 1.2 V with –5% to +10% tolerance, 1.25 V with –4% to +10% tolerance, and 1.3 V with –0% to +10% tolerance.

[2] See Ordering Guide on Page 63.

[3] When $V_{DDEXT}$ < 2.25 V, on-chip voltage regulation is not supported.

[4] Applies to all input and bidirectional pins except CLKIN.

[5] The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are 3.3 V tolerant (always accepts up to 3.6 V maximum $V_{IH}$), but voltage compliance (on outputs, $V_{OH}$) depends on the input $V_{DDEXT}$, because $V_{OH}$ (maximum) approximately equals $V_{DDEXT}$ (maximum). This 3.3 V tolerance applies to bidirectional pins (DATA15–0, TMR2–0, PF15–0, PPI3–0, RSCLK1–0, TSCLK1–0, RFS1–0, TFS1–0, MOSI, MISO, SCK) and input only pins ($\overline{BR}$, ARDY, PPI_CLK, DR0PRI, DR0SEC, DR1PRI, DR1SEC, RX, RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, NMI, and BMODE1–0).

[6] Applies to CLKIN pin only.

[7] Applies to all input and bidirectional pins.

**Table 16. Activity Scaling Factors**

| $I_{DDINT}$ Power Vector[1] | Activity Scaling Factor (ASF)[2] |
|---|---|
| $I_{DD-PEAK}$ | 1.27 |
| $I_{DD-HIGH}$ | 1.25 |
| $I_{DD-TYP}$ | 1.00 |
| $I_{DD-APP}$ | 0.86 |
| $I_{DD-NOP}$ | 0.72 |
| $I_{DD-IDLE}$ | 0.41 |

[1] See EE-229 for power vector definitions.
[2] All ASF values determined using a 10:1 CCLK:SCLK ratio.

**Table 17. Dynamic Current (mA, with ASF = 1.0)[1]**

| | Voltage ($V_{DDINT}$)[2] | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Frequency (MHz)[2] | 0.80 V | 0.85 V | 0.90 V | 0.95 V | 1.00 V | 1.05 V | 1.10 V | 1.15 V | 1.20 V | 1.25 V | 1.30 V | 1.32 V | 1.375 V | 1.43 V | 1.45 V |
| 50 | 12.7 | 13.9 | 15.3 | 16.8 | 18.1 | 19.4 | 21.0 | 22.3 | 24.0 | 25.4 | 26.4 | 27.2 | 28.7 | 30.3 | 30.7 |
| 100 | 22.6 | 24.2 | 26.2 | 28.1 | 30.1 | 31.8 | 34.7 | 36.2 | 38.4 | 40.5 | 43.0 | 43.4 | 45.7 | 47.9 | 48.9 |
| 200 | 40.8 | 44.1 | 46.9 | 50.3 | 53.3 | 56.9 | 59.9 | 63.1 | 66.7 | 70.2 | 73.8 | 75.0 | 78.7 | 82.4 | 84.6 |
| 250 | 50.1 | 53.8 | 57.2 | 61.4 | 64.7 | 68.9 | 72.9 | 76.8 | 81.0 | 85.1 | 89.3 | 90.8 | 95.2 | 99.6 | 102.0 |
| 300 | N/A | 63.5 | 67.4 | 72.4 | 76.2 | 81.0 | 85.9 | 90.6 | 95.2 | 100.0 | 104.8 | 106.6 | 111.8 | 116.9 | 119.4 |
| 375 | N/A | N/A | N/A | 88.6 | 93.5 | 99.0 | 104.6 | 110.3 | 116.0 | 122.1 | 128.0 | 130.0 | 136.2 | 142.4 | 145.5 |
| 400 | N/A | N/A | N/A | 93.9 | 99.3 | 105.0 | 110.8 | 116.8 | 123.0 | 129.4 | 135.7 | 137.9 | 144.6 | 151.2 | 154.3 |
| 425 | N/A | N/A | N/A | N/A | N/A | 111.0 | 117.3 | 123.5 | 129.9 | 136.8 | 143.2 | 145.6 | 152.6 | 159.7 | 162.8 |
| 475 | N/A | N/A | N/A | N/A | N/A | N/A | 130.3 | 136.8 | 143.8 | 151.4 | 158.1 | 161.1 | 168.9 | 176.6 | 179.7 |
| 500 | N/A | N/A | N/A | N/A | N/A | N/A | N/A | 143.5 | 150.7 | 158.7 | 165.6 | 168.8 | 177.0 | 185.2 | 188.2 |
| 533 | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | 160.4 | 168.8 | 176.5 | 179.6 | 188.2 | 196.8 | 200.5 |
| 600 | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | 196.2 | 199.6 | 209.3 | 219.0 | 222.6 |

[1] The values are not guaranteed as stand-alone maximum specifications, they must be combined with static current per the equations of Electrical Characteristics on Page 22.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 20.

## ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 18 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

**Table 18. Absolute Maximum Ratings**

| Parameter | Rating |
|---|---|
| Internal (Core) Supply Voltage ($V_{DDINT}$) | –0.3 V to +1.45 V |
| External (I/O) Supply Voltage ($V_{DDEXT}$) | –0.5 V to +3.8 V |
| Input Voltage[1, 2] | –0.5 V to +3.8 V |
| Output Voltage Swing | –0.5 V to $V_{DDEXT}$ + 0.5 V |
| Storage Temperature Range | –65°C to +150°C |
| Junction Temperature While Biased | 125°C |

[1] Applies to 100% transient duty cycle. For other duty cycles see Table 19.
[2] Applies only when $V_{DDEXT}$ is within specifications. When $V_{DDEXT}$ is outside specifications, the range is $V_{DDEXT}$ ± 0.2 V.

**Table 19. Maximum Duty Cycle for Input Transient Voltage[1]**

| $V_{IN}$ Min (V)[2] | $V_{IN}$ Max (V)[2] | Maximum Duty Cycle[3] |
|---|---|---|
| –0.50 | +3.80 | 100% |
| –0.70 | +4.00 | 40% |
| –0.80 | +4.10 | 25% |
| –0.90 | +4.20 | 15% |
| –1.00 | +4.30 | 10% |

[1] Applies to all signal pins with the exception of CLKIN, XTAL, VROUT1–0.
[2] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.
[3] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

## ESD SENSITIVITY

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

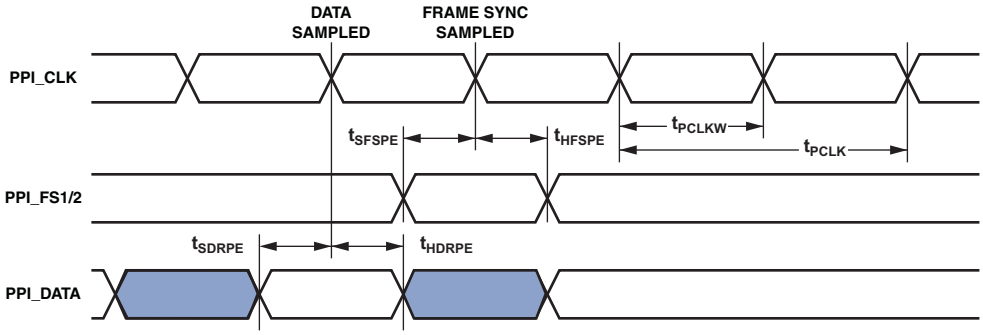



*Figure 19. PPI GP Rx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 0)*

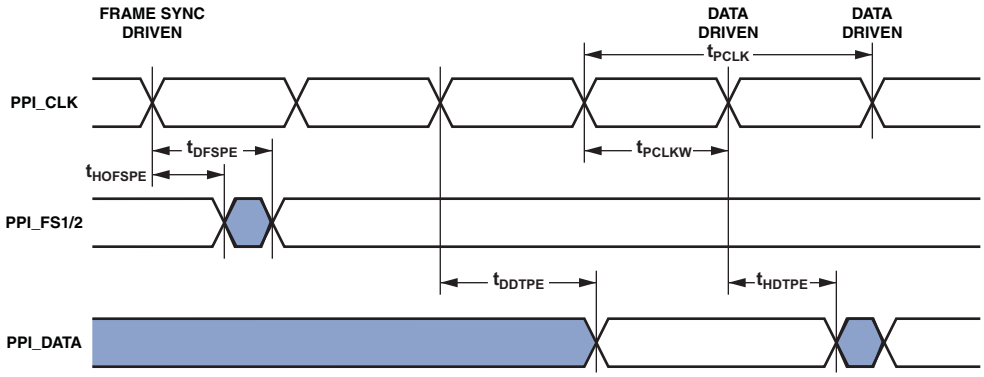



*Figure 20. PPI GP Tx Mode with Internal Frame Sync Timing*

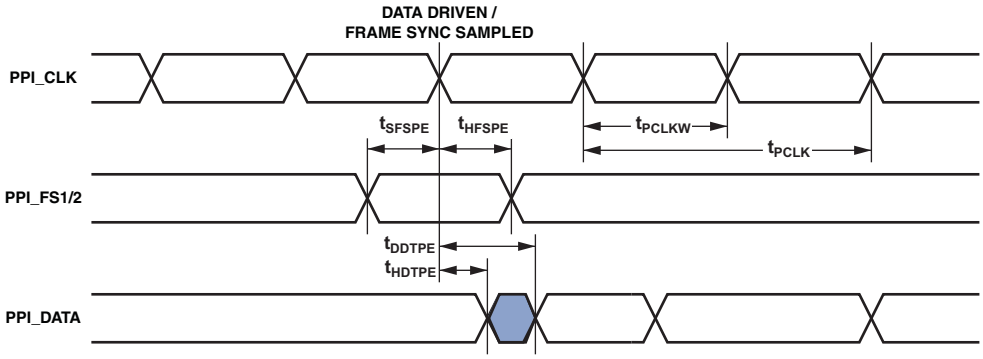



*Figure 21. PPI GP Tx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 1)*

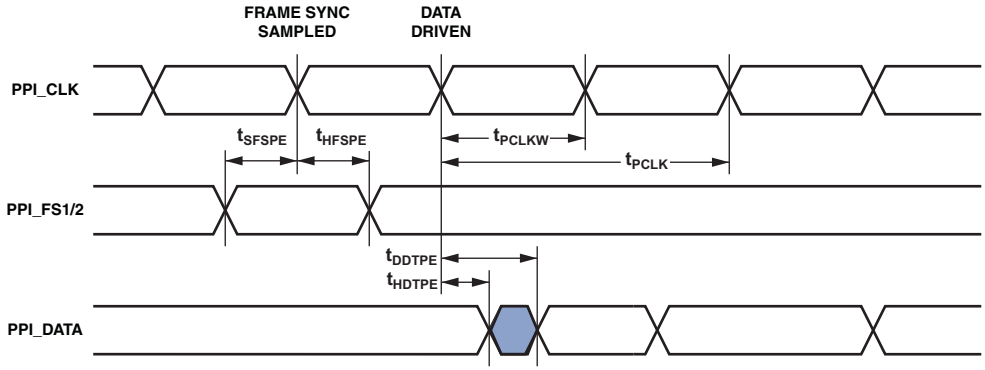



*Figure 22. PPI GP Tx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 0)*

**Table 30. Serial Ports—Enable and Three-State**

| Parameter | | $V_{DDEXT}$ = 1.8 V Min | $V_{DDEXT}$ = 1.8 V Max | $V_{DDEXT}$ = 2.5 V/3.3 V Min | $V_{DDEXT}$ = 2.5 V/3.3 V Max | Unit |
|---|---|---|---|---|---|---|
| *Switching Characteristics* | | | | | | |
| $t_{DTENE}$ | Data Enable Delay from External TSCLKx[1] | 0 | | 0 | | ns |
| $t_{DDTTE}$ | Data Disable Delay from External TSCLKx[1, 2, 3] | | 10.0 | | 10.0 | ns |
| $t_{DTENI}$ | Data Enable Delay from Internal TSCLKx[1] | −2.0 | | −2.0 | | ns |
| $t_{DDTTI}$ | Data Disable Delay from Internal TSCLKx[1, 2, 3] | | 3.0 | | 3.0 | ns |

[1] Referenced to drive edge.
[2] Applicable to multichannel mode only.
[3] TSCLKx is tied to RSCLKx.

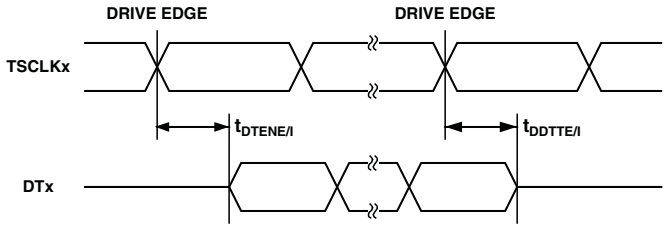



*Figure 25. Enable and Three-State*

**Table 31. External Late Frame Sync**

| Parameter | | $V_{DDEXT}$ = 1.8 V LQFP/PBGA Packages Min | Max | $V_{DDEXT}$ = 1.8 V CSP_BGA Package Min | Max | $V_{DDEXT}$ = 2.5 V/3.3 V All Packages Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| *Switching Characteristics* | | | | | | | | |
| $t_{DDTLFSE}$ | Data Delay from Late External TFSx or External RFSx in multichannel mode with MCMEN = 0[1, 2] | | 10.5 | | 10.0 | | 10.0 | ns |
| $t_{DTENLFS}$ | Data Enable from Late FS or in multichannel mode with MCMEN = 0[1, 2] | 0 | | 0 | | 0 | | ns |

[1] In multichannel mode, TFSx enable and TFSx valid follow $t_{DTENLFS}$ and $t_{DDTLFSE}$.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$, then $t_{DDTTE/I}$ and $t_{DTENE/I}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

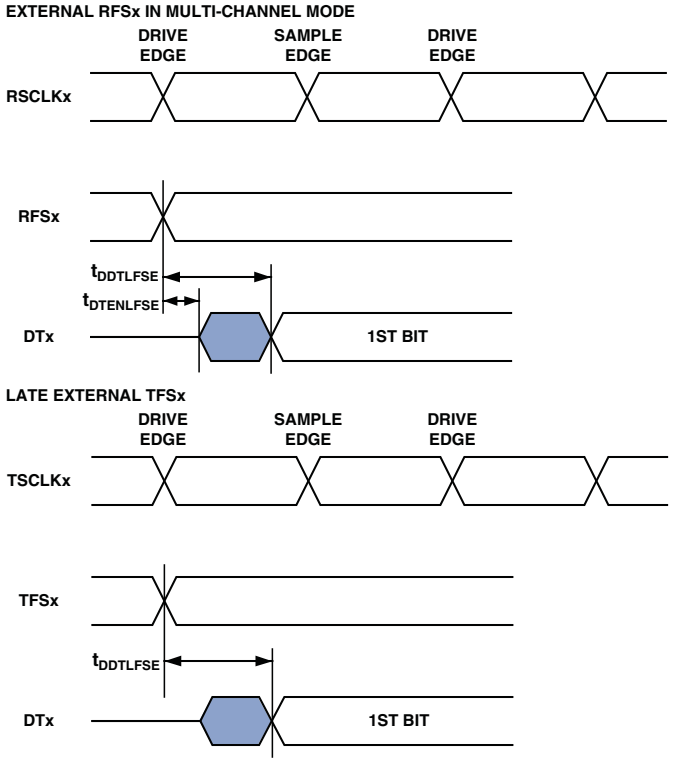



*Figure 26. External Late Frame Sync*

### *Serial Peripheral Interface (SPI) Port—Master Timing*

**Table 32. Serial Peripheral Interface (SPI) Port—Master Timing**

| Parameter | | $V_{DDEXT}$ = 1.8 V LQFP/PBGA Packages Min | Max | $V_{DDEXT}$ = 1.8 V CSP_BGA Package Min | Max | $V_{DDEXT}$ = 2.5 V/3.3 V All Packages Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | | | |
| $t_{SSPIDM}$ | Data Input Valid to SCK Edge (Data Input Setup) | 10.5 | | 9 | | 7.5 | | ns |
| $t_{HSPIDM}$ | SCK Sampling Edge to Data Input Invalid | –1.5 | | –1.5 | | –1.5 | | ns |
| *Switching Characteristics* | | | | | | | | |
| $t_{SDSCIM}$ | $\overline{SPISELx}$ Low to First SCK Edge | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPICHM}$ | Serial Clock High Period | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPICLM}$ | Serial Clock Low Period | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPICLK}$ | Serial Clock Period | $4 \times t_{SCLK} - 1.5$ | | $4 \times t_{SCLK} - 1.5$ | | $4 \times t_{SCLK} - 1.5$ | | ns |
| $t_{HDSM}$ | Last SCK Edge to $\overline{SPISELx}$ High | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPITDM}$ | Sequential Transfer Delay | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{DDSPIDM}$ | SCK Edge to Data Out Valid (Data Out Delay) | | 6 | | 6 | | 6 | ns |
| $t_{HDSPIDM}$ | SCK Edge to Data Out Invalid (Data Out Hold) | –1.0 | | –1.0 | | –1.0 | | ns |

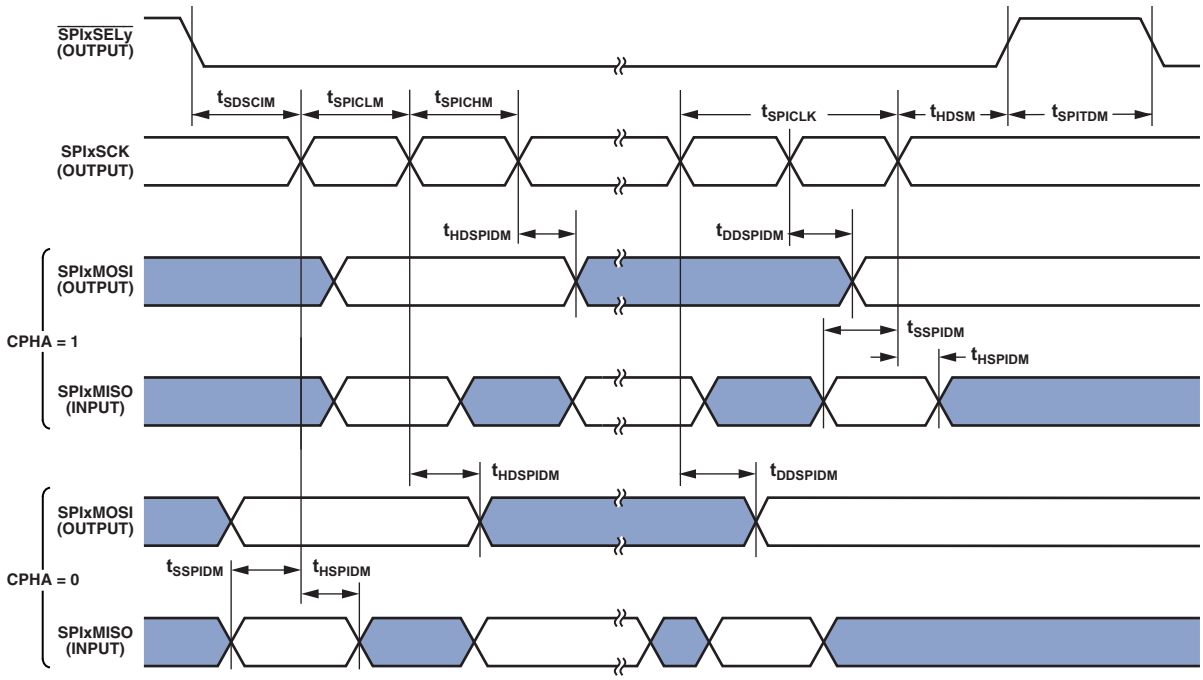



*Figure 27. Serial Peripheral Interface (SPI) Port—Master Timing*

### *Serial Peripheral Interface (SPI) Port—Slave Timing*

**Table 33. Serial Peripheral Interface (SPI) Port—Slave Timing**

| Parameter | | $V_{DDEXT}$ = 1.8 V LQFP/PBGA Packages Min | Max | $V_{DDEXT}$ = 1.8 V CSP_BGA Package Min | Max | $V_{DDEXT}$ = 2.5 V/3.3 V All Packages Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | | | |
| $t_{SPICHS}$ | Serial Clock High Period | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPICLS}$ | Serial Clock Low Period | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPICLK}$ | Serial Clock Period | $4 \times t_{SCLK}$ | | $4 \times t_{SCLK}$ | | $4 \times t_{SCLK}$ | | ns |
| $t_{HDS}$ | Last SCK Edge to $\overline{SPISS}$ Not Asserted | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPITDS}$ | Sequential Transfer Delay | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SDSCI}$ | $\overline{SPISS}$ Assertion to First SCK Edge | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SSPID}$ | Data Input Valid to SCK Edge (Data Input Setup) | 1.6 | | 1.6 | | 1.6 | | ns |
| $t_{HSPID}$ | SCK Sampling Edge to Data Input Invalid | 1.6 | | 1.6 | | 1.6 | | ns |
| *Switching Characteristics* | | | | | | | | |
| $t_{DSOE}$ | $\overline{SPISS}$ Assertion to Data Out Active | 0 | 10 | 0 | 9 | 0 | 8 | ns |
| $t_{DSDHI}$ | $\overline{SPISS}$ Deassertion to Data High Impedance | 0 | 10 | 0 | 9 | 0 | 8 | ns |
| $t_{DDSPID}$ | SCK Edge to Data Out Valid (Data Out Delay) | | 10 | | 10 | | 10 | ns |
| $t_{HDSPID}$ | SCK Edge to Data Out Invalid (Data Out Hold) | 0 | | 0 | | 0 | | ns |

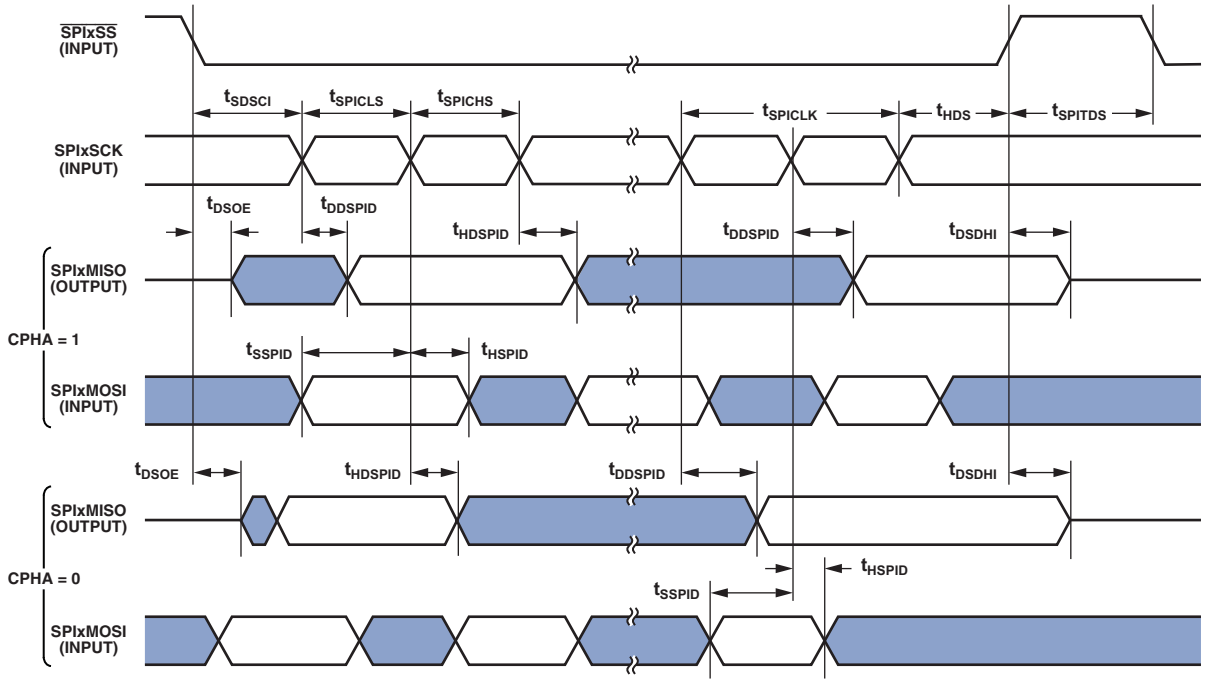



*Figure 28. Serial Peripheral Interface (SPI) Port—Slave Timing*

### Timer Clock Timing

Table 35 and Figure 30 describe timer clock timing.

**Table 35. Timer Clock Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Switching Characteristic* | | | | |
| $t_{TODP}$ | Timer Output Update Delay After PPI_CLK High | | 12 | ns |

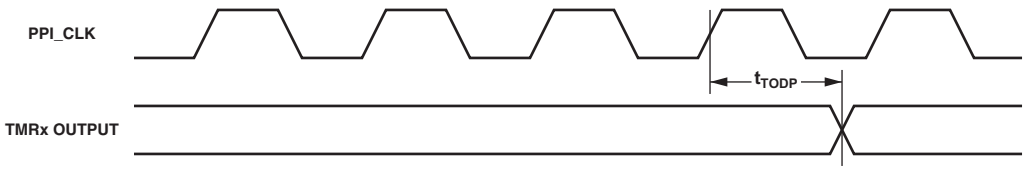



*Figure 30. Timer Clock Timing*

### Timer Cycle Timing

Table 36 and Figure 31 describe timer expired operations. The input signal is asynchronous in width capture mode and external clock mode and has an absolute maximum input frequency of $f_{SCLK}/2$ MHz.

**Table 36. Timer Cycle Timing**

| Parameter | | $V_{DDEXT}$ = 1.8 V Min | $V_{DDEXT}$ = 1.8 V Max | $V_{DDEXT}$ = 2.5 V/3.3 V Min | $V_{DDEXT}$ = 2.5 V/3.3 V Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Characteristics* | | | | | | |
| $t_{WL}$ | Timer Pulse Width Low[1] | $1 \times t_{SCLK}$ | | $1 \times t_{SCLK}$ | | ns |
| $t_{WH}$ | Timer Pulse Width High[1] | $1 \times t_{SCLK}$ | | $1 \times t_{SCLK}$ | | ns |
| $t_{TIS}$ | Timer Input Setup Time Before CLKOUT Low[2] | 8.0 | | 6.5 | | ns |
| $t_{TIH}$ | Timer Input Hold Time After CLKOUT Low[2] | 1.5 | | 1.5 | | ns |
| *Switching Characteristics* | | | | | | |
| $t_{HTO}$ | Timer Pulse Width Output | $1 \times t_{SCLK}$ | $(2^{32}-1) \times t_{SCLK}$ | $1 \times t_{SCLK}$ | $(2^{32}-1) \times t_{SCLK}$ | ns |
| $t_{TOD}$ | Timer Output Update Delay After CLKOUT High | | 7.5 | | 6.5 | ns |

[1] The minimum pulse widths apply for TMRx input pins in width capture and external clock modes. They also apply to the PF1 or PPI_CLK input pins in PWM output mode.
[2] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize programmable flag inputs.

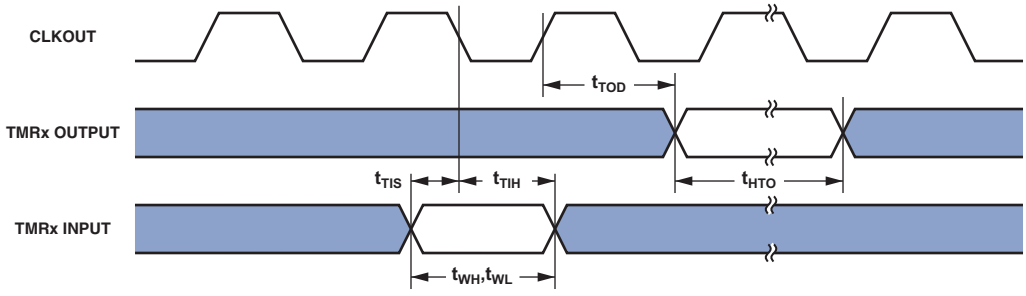



*Figure 31. Timer PWM_OUT Cycle Timing*

**Table 42. 160-Ball CSP_BGA Ball Assignment (Numerical by Ball Number)**

| Ball No. | Signal | Ball No. | Signal | Ball No. | Signal | Ball No. | Signal |
|---|---|---|---|---|---|---|---|
| A1 | $V_{DDEXT}$ | C13 | $\overline{SMS}$ | H1 | DT0PRI | M3 | TDI |
| A2 | PF8 | C14 | $\overline{SCAS}$ | H2 | DT0SEC | M4 | GND |
| A3 | PF9 | D1 | SCK | H3 | TFS0 | M5 | DATA12 |
| A4 | PF10 | D2 | PF0 | H4 | GND | M6 | DATA9 |
| A5 | PF11 | D3 | MOSI | H11 | GND | M7 | DATA6 |
| A6 | PF14 | D4 | GND | H12 | $\overline{ABE1}$ | M8 | DATA3 |
| A7 | PPI2 | D5 | $V_{DDEXT}$ | H13 | $\overline{ABE0}$ | M9 | DATA0 |
| A8 | RTXO | D6 | $V_{DDINT}$ | H14 | $\overline{AWE}$ | M10 | GND |
| A9 | RTXI | D7 | GND | J1 | TSCLK0 | M11 | ADDR15 |
| A10 | GND | D8 | GND | J2 | DR0SEC | M12 | ADDR9 |
| A11 | XTAL | D9 | $V_{DDEXT}$ | J3 | RFS0 | M13 | ADDR10 |
| A12 | CLKIN | D10 | GND | J4 | $V_{DDEXT}$ | M14 | ADDR11 |
| A13 | VROUT0 | D11 | GND | J11 | $V_{DDINT}$ | N1 | $\overline{TRST}$ |
| A14 | GND | D12 | $\overline{SWE}$ | J12 | $V_{DDEXT}$ | N2 | TMS |
| B1 | PF4 | D13 | $\overline{SRAS}$ | J13 | ADDR4 | N3 | TDO |
| B2 | PF5 | D14 | $\overline{BR}$ | J14 | ADDR1 | N4 | BMODE0 |
| B3 | PF6 | E1 | TFS1 | K1 | DR0PRI | N5 | DATA13 |
| B4 | PF7 | E2 | MISO | K2 | TMR2 | N6 | DATA10 |
| B5 | PF12 | E3 | DT1SEC | K3 | TX | N7 | DATA7 |
| B6 | PF13 | E4 | $V_{DDINT}$ | K4 | GND | N8 | DATA4 |
| B7 | PPI3 | E11 | $V_{DDINT}$ | K11 | GND | N9 | DATA1 |
| B8 | PPI1 | E12 | SA10 | K12 | ADDR7 | N10 | $\overline{BGH}$ |
| B9 | $V_{DDRTC}$ | E13 | ARDY | K13 | ADDR5 | N11 | ADDR16 |
| B10 | NMI | E14 | $\overline{AMS0}$ | K14 | ADDR2 | N12 | ADDR14 |
| B11 | GND | F1 | TSCLK1 | L1 | RSCLK0 | N13 | ADDR13 |
| B12 | VROUT1 | F2 | DT1PRI | L2 | TMR0 | N14 | ADDR12 |
| B13 | SCKE | F3 | DR1SEC | L3 | RX | P1 | $V_{DDEXT}$ |
| B14 | CLKOUT | F4 | GND | L4 | $V_{DDINT}$ | P2 | TCK |
| C1 | PF1 | F11 | GND | L5 | GND | P3 | BMODE1 |
| C2 | PF2 | F12 | $V_{DDEXT}$ | L6 | GND | P4 | DATA15 |
| C3 | PF3 | F13 | $\overline{AMS2}$ | L7 | $V_{DDEXT}$ | P5 | DATA14 |
| C4 | GND | F14 | $\overline{AMS1}$ | L8 | GND | P6 | DATA11 |
| C5 | GND | G1 | RSCLK1 | L9 | $V_{DDINT}$ | P7 | DATA8 |
| C6 | PF15 | G2 | RFS1 | L10 | GND | P8 | DATA5 |
| C7 | $V_{DDEXT}$ | G3 | DR1PRI | L11 | $V_{DDEXT}$ | P9 | DATA2 |
| C8 | PPI0 | G4 | $V_{DDEXT}$ | L12 | ADDR8 | P10 | $\overline{BG}$ |
| C9 | PPI_CLK | G11 | GND | L13 | ADDR6 | P11 | ADDR19 |
| C10 | $\overline{RESET}$ | G12 | $\overline{AMS3}$ | L14 | ADDR3 | P12 | ADDR18 |
| C11 | GND | G13 | $\overline{AOE}$ | M1 | TMR1 | P13 | ADDR17 |
| C12 | $V_{DDEXT}$ | G14 | $\overline{ARE}$ | M2 | $\overline{EMU}$ | P14 | GND |

# 169-BALL PBGA BALL ASSIGNMENT

Table 43 lists the PBGA ball assignment by signal. Table 44 on Page 54 lists the PBGA ball assignment by ball number.

**Table 43. 169-Ball PBGA Ball Assignment (Alphabetical by Signal)**

| Signal | Ball No. | Signal | Ball No. | Signal | Ball No. | Signal | Ball No. | Signal | Ball No. |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{ABE0}$ | H16 | DATA4 | U12 | GND | K9 | RTXI | A10 | $V_{DDEXT}$ | K6 |
| $\overline{ABE1}$ | H17 | DATA5 | U11 | GND | K10 | RTXO | A11 | $V_{DDEXT}$ | L6 |
| ADDR1 | J16 | DATA6 | T10 | GND | K11 | RX | T1 | $V_{DDEXT}$ | M6 |
| ADDR2 | J17 | DATA7 | U10 | GND | L7 | SA10 | B15 | $V_{DDEXT}$ | M7 |
| ADDR3 | K16 | DATA8 | T9 | GND | L8 | $\overline{SCAS}$ | A16 | $V_{DDEXT}$ | M8 |
| ADDR4 | K17 | DATA9 | U9 | GND | L9 | SCK | D1 | $V_{DDEXT}$ | T2 |
| ADDR5 | L16 | DATA10 | T8 | GND | L10 | SCKE | B14 | VROUT0 | B12 |
| ADDR6 | L17 | DATA11 | U8 | GND | L11 | $\overline{SMS}$ | A17 | VROUT1 | B13 |
| ADDR7 | M16 | DATA12 | U7 | GND | M9 | $\overline{SRAS}$ | A15 | XTAL | A13 |
| ADDR8 | M17 | DATA13 | T7 | GND | T16 | $\overline{SWE}$ | B17 | | |
| ADDR9 | N17 | DATA14 | U6 | MISO | E2 | TCK | U4 | | |
| ADDR10 | N16 | DATA15 | T6 | MOSI | E1 | TDI | U3 | | |
| ADDR11 | P17 | DR0PRI | M2 | NMI | B11 | TDO | T4 | | |
| ADDR12 | P16 | DR0SEC | M1 | PF0 | D2 | TFS0 | L1 | | |
| ADDR13 | R17 | DR1PRI | H1 | PF1 | C1 | TFS1 | G2 | | |
| ADDR14 | R16 | DR1SEC | H2 | PF2 | B1 | TMR0 | R1 | | |
| ADDR15 | T17 | DT0PRI | K2 | PF3 | C2 | TMR1 | P2 | | |
| ADDR16 | U15 | DT0SEC | K1 | PF4 | A1 | TMR2 | P1 | | |
| ADDR17 | T15 | DT1PRI | F1 | PF5 | A2 | TMS | T3 | | |
| ADDR18 | U16 | DT1SEC | F2 | PF6 | B3 | $\overline{TRST}$ | U2 | | |
| ADDR19 | T14 | $\overline{EMU}$ | U1 | PF7 | A3 | TSCLK0 | L2 | | |
| $\overline{AMS0}$ | D17 | GND | B16 | PF8 | B4 | TSCLK1 | G1 | | |
| $\overline{AMS1}$ | E16 | GND | F11 | PF9 | A4 | TX | R2 | | |
| $\overline{AMS2}$ | E17 | GND | G7 | PF10 | B5 | VDD | F12 | | |
| $\overline{AMS3}$ | F16 | GND | G8 | PF11 | A5 | VDD | G12 | | |
| $\overline{AOE}$ | F17 | GND | G9 | PF12 | A6 | VDD | H12 | | |
| ARDY | C16 | GND | G10 | PF13 | B6 | VDD | J12 | | |
| $\overline{ARE}$ | G16 | GND | G11 | PF14 | A7 | VDD | K12 | | |
| $\overline{AWE}$ | G17 | GND | H7 | PF15 | B7 | VDD | L12 | | |
| $\overline{BG}$ | T13 | GND | H8 | PPI_CLK | B10 | VDD | M10 | | |
| $\overline{BGH}$ | U17 | GND | H9 | PPI0 | B9 | VDD | M11 | | |
| BMODE0 | U5 | GND | H10 | PPI1 | A9 | VDD | M12 | | |
| BMODE1 | T5 | GND | H11 | PPI2 | B8 | $V_{DDEXT}$ | B2 | | |
| $\overline{BR}$ | C17 | GND | J7 | PPI3 | A8 | $V_{DDEXT}$ | F6 | | |
| CLKIN | A14 | GND | J8 | $\overline{RESET}$ | A12 | $V_{DDEXT}$ | F7 | | |
| CLKOUT | D16 | GND | J9 | RFS0 | N1 | $V_{DDEXT}$ | F8 | | |
| DATA0 | U14 | GND | J10 | RFS1 | J1 | $V_{DDEXT}$ | F9 | | |
| DATA1 | T12 | GND | J11 | RSCLK0 | N2 | $V_{DDEXT}$ | G6 | | |
| DATA2 | U13 | GND | K7 | RSCLK1 | J2 | $V_{DDEXT}$ | H6 | | |
| DATA3 | T11 | GND | K8 | RTCVDD | F10 | $V_{DDEXT}$ | J6 | | |

## OUTLINE DIMENSIONS

Dimensions in the outline dimension figures are shown in millimeters.

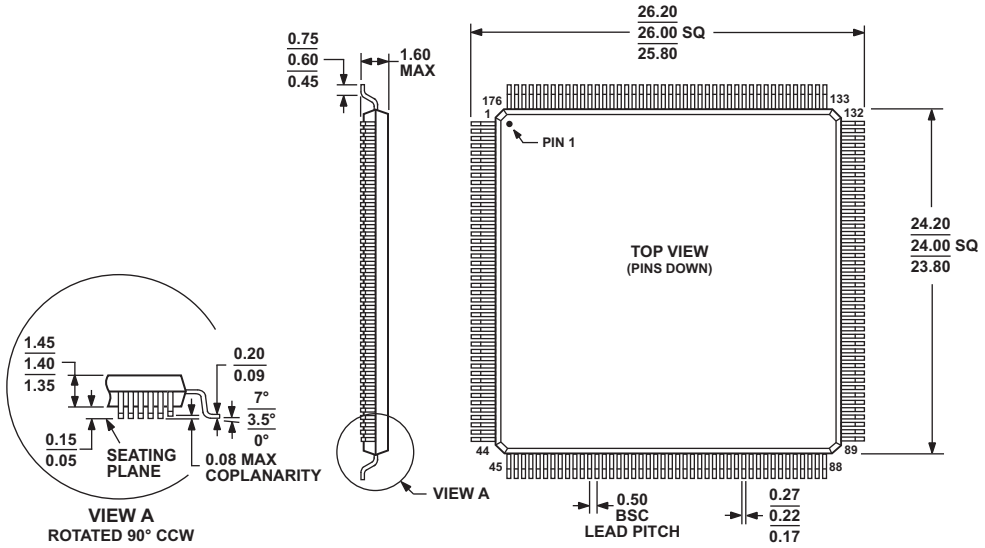
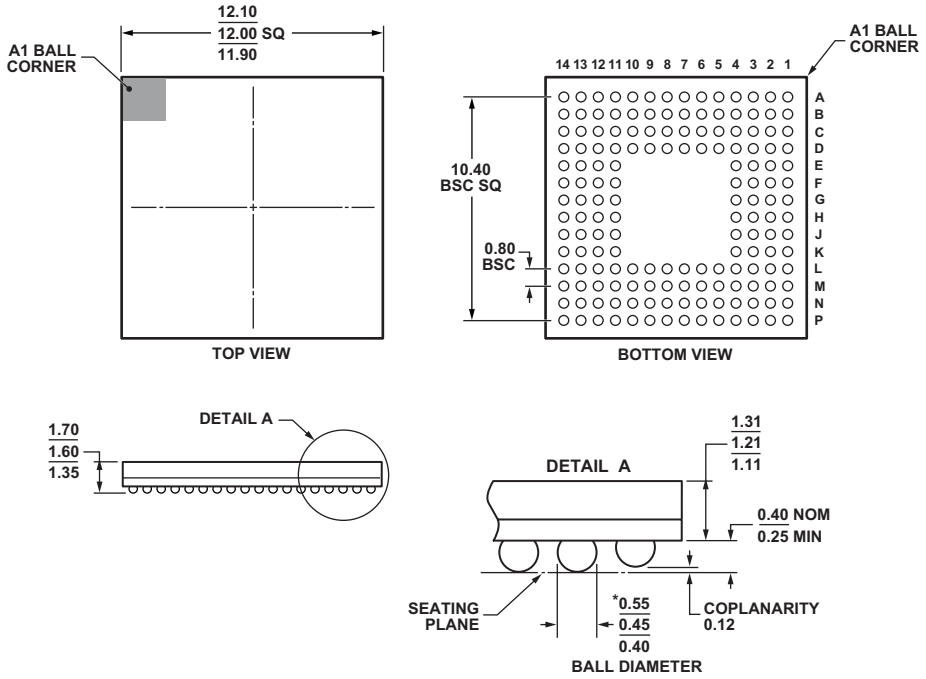



*Figure 64. 176-Lead Low Profile Quad Flat Package [LQFP]*
*(ST-176-1)*
*Dimensions shown in millimeters*




*COMPLIANT TO JEDEC STANDARDS MO-205-AE WITH THE EXCEPTION TO BALL DIAMETER.

*Figure 65. 160-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-160-2)*
*Dimensions shown in millimeters*

## AUTOMOTIVE PRODUCTS

The ADBF531W, ADBF532W, and ADBF533W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 48 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

**Table 48. Automotive Products**

| Product Family[1,2] | Temperature Range[3] | Speed Grade (Max) | Package Description | Package Option |
|---|---|---|---|---|
| ADBF531WBSTZ4xx | –40°C to +85°C | 400 MHz | 176-Lead LQFP | ST-176-1 |
| ADBF531WBBCZ4xx | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADBF531WYBCZ4xx | –40°C to +105°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADBF532WBSTZ4xx | –40°C to +85°C | 400 MHz | 176-Lead LQFP | ST-176-1 |
| ADBF532WBBCZ4xx | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADBF532WYBCZ4xx | –40°C to +105°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADBF533WBBCZ5xx | –40°C to +85°C | 533 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADBF533WBBZ5xx | –40°C to +85°C | 533 MHz | 169-Ball PBGA | B-169 |
| ADBF533WYBCZ4xx | –40°C to +105°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADBF533WYBBZ4xx | –40°C to +105°C | 400 MHz | 169-Ball PBGA | B-169 |

[1] Z = RoHS compliant part.
[2] xx denotes silicon revision.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 20 for junction temperature ($T_J$) specification which is the only temperature specification.

## ORDERING GUIDE

| Model [1] | Temperature Range [2] | Speed Grade (Max) | Package Description | Package Option |
|---|---|---|---|---|
| ADSP-BF531SBB400 | –40°C to +85°C | 400 MHz | 169-Ball PBGA | B-169 |
| ADSP-BF531SBBZ400 | –40°C to +85°C | 400 MHz | 169-Ball PBGA | B-169 |
| ADSP-BF531SBBC400 | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF531SBBCZ400 | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF531SBBCZ4RL | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA, 13" Tape and Reel | BC-160-2 |
| ADSP-BF531SBSTZ400 | –40°C to +85°C | 400 MHz | 176-Lead LQFP | ST-176-1 |
| ADSP-BF532SBBZ400 | –40°C to +85°C | 400 MHz | 169-Ball PBGA | B-169 |
| ADSP-BF532SBBC400 | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF532SBBCZ400 | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF532SBSTZ400 | –40°C to +85°C | 400 MHz | 176-Lead LQFP | ST-176-1 |
| ADSP-BF533SBBZ400 | –40°C to +85°C | 400 MHz | 169-Ball PBGA | B-169 |
| ADSP-BF533SBBC400 | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF533SBBCZ400 | –40°C to +85°C | 400 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF533SBSTZ400 | –40°C to +85°C | 400 MHz | 176-Lead LQFP | ST-176-1 |
| ADSP-BF533SBB500 | –40°C to +85°C | 500 MHz | 169-Ball PBGA | B-169 |
| ADSP-BF533SBBZ500 | –40°C to +85°C | 500 MHz | 169-Ball PBGA | B-169 |
| ADSP-BF533SBBC500 | –40°C to +85°C | 500 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF533SBBCZ500 | –40°C to +85°C | 500 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF533SBBC-5V | –40°C to +85°C | 533 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF533SBBCZ-5V | –40°C to +85°C | 533 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF533SKBC-6V | 0°C to +70°C | 600 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF533SKBCZ-6V | 0°C to +70°C | 600 MHz | 160-Ball CSP_BGA | BC-160-2 |
| ADSP-BF533SKSTZ-5V | 0°C to +70°C | 533 MHz | 176-Lead LQFP | ST-176-1 |

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 20 for junction temperature ($T_J$) specification which is the only temperature specification.