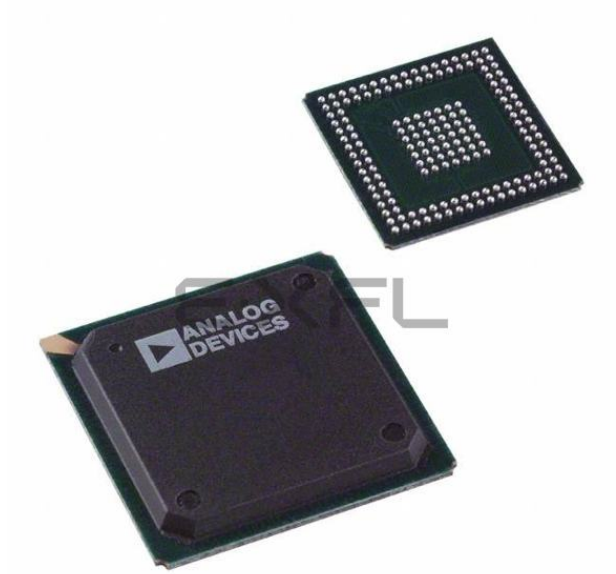

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	400MHz
Non-Volatile Memory	ROM (1kB)
On-Chip RAM	148kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-BBGA
Supplier Device Package	169-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf533sbbz400

GENERAL DESCRIPTION

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are members of the Blackfin® family of products, incorporating the Analog Devices, Inc./Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single instruction, multiple data (SIMD) multimedia capabilities into a single instruction set architecture.

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are completely code and pin-compatible, differing only with respect to their performance and on-chip memory. Specific performance and memory configurations are shown in Table 1.

Table 1. Processor Comparison

Features		ADSP-BF531	ADSP-BF532	ADSP-BF533
SPORTs		2	2	2
UART		1	1	1
SPI		1	1	1
GP Timers		3	3	3
Watchdog Timers		1	1	1
RTC		1	1	1
Parallel Peripheral Interface		1	1	1
GPIOs		16	16	16
Memory Configuration	L1 Instruction SRAM/Cache	16K bytes	16K bytes	16K bytes
	L1 Instruction SRAM	16K bytes	32K bytes	64K bytes
	L1 Data SRAM/Cache	16K bytes	32K bytes	32K bytes
	L1 Data SRAM			32K bytes
	L1 Scratchpad	4K bytes	4K bytes	4K bytes
	L3 Boot ROM	1K bytes	1K bytes	1K bytes
Maximum Speed Grade		400 MHz	400 MHz	600 MHz
Package Options: CSP_BGA Plastic BGA LQFP		 160-Ball 169-Ball 176-Lead	 160-Ball 169-Ball 176-Lead	 160-Ball 169-Ball 176-Lead

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

PORTABLE LOW POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. Blackfin processors are designed in a low power and low voltage design methodology and feature dynamic power management—the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. Varying the voltage and frequency can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This translates into longer battery life for portable appliances.

SYSTEM INTEGRATION

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are highly integrated system-on-a-chip solutions for the next generation of digital communication and consumer multimedia applications. By combining industry-standard interfaces with a high performance signal processing core, users can develop cost-effective solutions quickly without the need for costly external components. The system peripherals include a UART port, an SPI port, two serial ports (SPORTs), four general-purpose timers (three with PWM capability), a real-time clock, a watchdog timer, and a parallel peripheral interface.

PROCESSOR PERIPHERALS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors contain a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the functional block diagram in Figure 1 on Page 1). The general-purpose peripherals include functions such as UART, timers with PWM (pulse-width modulation) and pulse measurement capability, general-purpose I/O pins, a real-time clock, and a watchdog timer. This set of functions satisfies a wide variety of typical system support needs and is augmented by the system expansion capabilities of the part. In addition to these general-purpose peripherals, the processors contain high speed serial and parallel ports for interfacing to a variety of audio, video, and modem codec functions; an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources; and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

All of the peripherals, except for general-purpose I/O, real-time clock, and timers, are supported by a flexible DMA structure. There is also a separate memory DMA channel dedicated to data transfers between the processor's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses running at up to 133 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The processors include an on-chip voltage regulator in support of the processor's dynamic power management capability. The voltage regulator provides a range of core voltage levels from V_{DDEXT}. The voltage regulator can be bypassed at the user's discretion.

BLACKFIN PROCESSOR CORE

As shown in Figure 2 on Page 5, the Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-bit, 16-bit, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo 2^{32} multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions includes byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). Quad 16-bit operations are possible using the second ALU.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

MEMORY ARCHITECTURE

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors view memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low latency on-chip memory as cache or SRAM, and larger, lower cost and performance off-chip memory systems. See Figure 3, Figure 4, and Figure 5 on Page 6.

The L1 memory system is the primary highest performance memory available to the Blackfin processor. The off-chip memory system, accessed through the external bus interface unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing up to 132M bytes of physical memory.

The memory DMA controller provides high bandwidth data-movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

Internal (On-Chip) Memory

The processors have three blocks of on-chip memory that provide high bandwidth access to the core.

The first block is the L1 instruction memory, consisting of up to 80K bytes SRAM, of which 16K bytes can be configured as a four way set-associative cache. This memory is accessed at full processor speed.

PFx pins defined as inputs can be configured to generate hardware interrupts, while output PFx pins can be triggered by software interrupts.

- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual PFx pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

PARALLEL PERIPHERAL INTERFACE

The processors provide a parallel peripheral interface (PPI) that can connect directly to parallel ADCs and DACs, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bi-directional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bi-directional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications.

Three distinct sub modes are supported:

- Input mode – Frame syncs and data are inputs into the PPI.
- Frame capture mode – Frame syncs are outputs from the PPI, but data are inputs.
- Output mode – Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (e.g., for frame capture). The processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct sub modes are supported:

- Active video only mode
- Vertical blanking only mode
- Entire field mode

Active Video Only Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that can be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

DYNAMIC POWER MANAGEMENT

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors provides four operating modes, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

SPECIFICATIONS

Component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 400 MHz and 500 MHz speed grade models[2]	0.8	1.2	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 533 MHz speed grade models[2]	0.8	1.25	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	600 MHz speed grade models[2]	0.8	1.30	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	Automotive 400 MHz speed grade models[2]	0.95	1.2	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	Automotive 533 MHz speed grade models[2]	0.95	1.25	1.45	V
V_{DDEXT}	External Supply Voltage[3]	Nonautomotive grade models[2]	1.75	1.8/3.3	3.6	V
V_{DDEXT}	External Supply Voltage	Automotive grade models[2]	2.7	3.3	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage	Nonautomotive grade models[2]	1.75	1.8/3.3	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage	Automotive grade models[2]	2.7	3.3	3.6	V
V_{IH}	High Level Input Voltage[4, 5]	V_{DDEXT} = 1.85 V	1.3			V
V_{IH}	High Level Input Voltage[4, 5]	V_{DDEXT} = Maximum	2.0			V
$V_{IHCLKIN}$	High Level Input Voltage[6]	V_{DDEXT} = Maximum	2.2			V
V_{IL}	Low Level Input Voltage[7]	V_{DDEXT} = 1.75 V			+0.3	V
V_{IL}	Low Level Input Voltage[7]	V_{DDEXT} = 2.7 V			+0.6	V
T_J	Junction Temperature	160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = 0°C to +70°C	0		+95	°C
T_J	Junction Temperature	160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C
T_J	Junction Temperature	169-Ball Plastic Ball Grid Array (PBGA) @ $T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C
T_J	Junction Temperature	169-Ball Plastic Ball Grid Array (PBGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	176-Lead Quad Flatpack (LQFP) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+100	°C

[1] The regulator can generate V_{DDINT} at levels of 0.85 V to 1.2 V with –5% to +10% tolerance, 1.25 V with –4% to +10% tolerance, and 1.3 V with –0% to +10% tolerance.

[2] See Ordering Guide on Page 63.

[3] When V_{DDEXT} < 2.25 V, on-chip voltage regulation is not supported.

[4] Applies to all input and bidirectional pins except CLKIN.

[5] The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are 3.3 V tolerant (always accepts up to 3.6 V maximum V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}, because V_{OH} (maximum) approximately equals V_{DDEXT} (maximum). This 3.3 V tolerance applies to bidirectional pins (DATA15–0, TMR2–0, PF15–0, PPI3–0, RSCLK1–0, TSCLK1–0, RFS1–0, TFS1–0, MOSI, MISO, SCK) and input only pins ($\overline{BR}$, ARDY, PPI_CLK, DR0PRI, DR0SEC, DR1PRI, DR1SEC, RX, RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, NMI, and BMODE1–0).

[6] Applies to CLKIN pin only.

[7] Applies to all input and bidirectional pins.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	400 MHz[1] Min	400 MHz[1] Typical	400 MHz[1] Max	500 MHz/533 MHz/600 MHz[2] Min	500 MHz/533 MHz/600 MHz[2] Typical	500 MHz/533 MHz/600 MHz[2] Max	Unit
V_{OH}	High Level Output Voltage[3]	V_{DDEXT} = 1.75 V, I_{OH} = –0.5 mA V_{DDEXT} = 2.25 V, I_{OH} = –0.5 mA V_{DDEXT} = 3.0 V, I_{OH} = –0.5 mA	1.5 1.9 2.4			1.5 1.9 2.4			V V V
V_{OL}	Low Level Output Voltage[3]	V_{DDEXT} = 1.75 V, I_{OL} = 2.0 mA V_{DDEXT} = 2.25 V/3.0 V, I_{OL} = 2.0 mA			0.2 0.4			0.2 0.4	V V
I_{IH}	High Level Input Current[4]	V_{DDEXT} = Max, V_{IN} = V_{DD} Max			10.0			10.0	µA
I_{IHP}	High Level Input Current JTAG[5]	V_{DDEXT} = Max, V_{IN} = V_{DD} Max			50.0			50.0	µA
I_{IL}[6]	Low Level Input Current[4]	V_{DDEXT} = Max, V_{IN} = 0 V			10.0			10.0	µA
I_{OZH}	Three-State Leakage Current[7]	V_{DDEXT} = Max, V_{IN} = V_{DD} Max			10.0			10.0	µA
I_{OZL}[6]	Three-State Leakage Current[7]	V_{DDEXT} = Max, V_{IN} = 0 V			10.0			10.0	µA
C_{IN}	Input Capacitance[8]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		4	8[9]		4	8[9]	pF
$I_{DDDEEPSLEEP}$[10]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.0 V, f_{CCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		7.5			32.5		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 0.8 V, T_J = 25°C, SCLK = 25 MHz			10			37.5	mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.14 V, f_{CCLK} = 400 MHz, T_J = 25°C		125			152		mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.2 V, f_{CCLK} = 500 MHz, T_J = 25°C					190		mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.2 V, f_{CCLK} = 533 MHz, T_J = 25°C					200		mA
I_{DD-TYP}[11]	V_{DDINT} Current	V_{DDINT} = 1.3 V, f_{CCLK} = 600 MHz, T_J = 25°C					245		mA
$I_{DDHIBERNATE}$[10]	V_{DDEXT} Current in Hibernate State	V_{DDEXT} = 3.6 V, CLKIN = 0 MHz, T_J = Max, voltage regulator off (V_{DDINT} = 0 V)		50	100		50	100	µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J = 25°C		20			20		µA
$I_{DDDEEPSLEEP}$[10]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz		6	Table 15		16	Table 14	mA
I_{DD-INT}	V_{DDINT} Current	f_{CCLK} > 0 MHz			$I_{DDDEEPSLEEP}$ + (Table 17 × ASF)			$I_{DDDEEPSLEEP}$ + (Table 17 × ASF)	mA

[1] Applies to all 400 MHz speed grade models. See Ordering Guide on Page 63.
[2] Applies to all 500 MHz, 533 MHz, and 600 MHz speed grade models. See Ordering Guide on Page 63.
[3] Applies to output and bidirectional pins.
[4] Applies to input pins except JTAG inputs.

Table 16. Activity Scaling Factors

I_{DDINT} Power Vector[1]	Activity Scaling Factor (ASF)[2]
$I_{DD-PEAK}$	1.27
$I_{DD-HIGH}$	1.25
I_{DD-TYP}	1.00
I_{DD-APP}	0.86
I_{DD-NOP}	0.72
$I_{DD-IDLE}$	0.41

[1] See EE-229 for power vector definitions.
[2] All ASF values determined using a 10:1 CCLK:SCLK ratio.

Table 17. Dynamic Current (mA, with ASF = 1.0)[1]

	Voltage (V_{DDINT})[2]														
Frequency (MHz)[2]	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V	1.45 V
50	12.7	13.9	15.3	16.8	18.1	19.4	21.0	22.3	24.0	25.4	26.4	27.2	28.7	30.3	30.7
100	22.6	24.2	26.2	28.1	30.1	31.8	34.7	36.2	38.4	40.5	43.0	43.4	45.7	47.9	48.9
200	40.8	44.1	46.9	50.3	53.3	56.9	59.9	63.1	66.7	70.2	73.8	75.0	78.7	82.4	84.6
250	50.1	53.8	57.2	61.4	64.7	68.9	72.9	76.8	81.0	85.1	89.3	90.8	95.2	99.6	102.0
300	N/A	63.5	67.4	72.4	76.2	81.0	85.9	90.6	95.2	100.0	104.8	106.6	111.8	116.9	119.4
375	N/A	N/A	N/A	88.6	93.5	99.0	104.6	110.3	116.0	122.1	128.0	130.0	136.2	142.4	145.5
400	N/A	N/A	N/A	93.9	99.3	105.0	110.8	116.8	123.0	129.4	135.7	137.9	144.6	151.2	154.3
425	N/A	N/A	N/A	N/A	N/A	111.0	117.3	123.5	129.9	136.8	143.2	145.6	152.6	159.7	162.8
475	N/A	N/A	N/A	N/A	N/A	N/A	130.3	136.8	143.8	151.4	158.1	161.1	168.9	176.6	179.7
500	N/A	N/A	N/A	N/A	N/A	N/A	N/A	143.5	150.7	158.7	165.6	168.8	177.0	185.2	188.2
533	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	160.4	168.8	176.5	179.6	188.2	196.8	200.5
600	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	196.2	199.6	209.3	219.0	222.6

[1] The values are not guaranteed as stand-alone maximum specifications, they must be combined with static current per the equations of Electrical Characteristics on Page 22.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 20.

PACKAGE INFORMATION

The information presented in Figure 10 and Table 20 provides details about the package branding for the Blackfin processors. For a complete listing of product availability, see the Ordering Guide on Page 63.

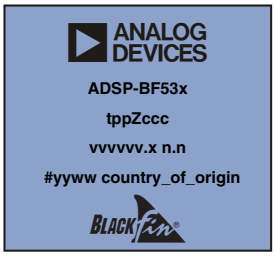


Figure 10. Product Information on Package

Table 20. Package Brand Information[1]

Brand Key	Field Description
ADSP-BF53x	Either ADSP-BF531, ADSP-BF532, or ADSP-BF533
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

[1] Non Automotive only. For branding information specific to Automotive products, contact Analog Devices Inc.

Asynchronous Memory Read Cycle Timing

Table 23. Asynchronous Memory Read Cycle Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{SDAT}	DATA15–0 Setup Before CLKOUT	2.1		2.1		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	1.0		0.8		ns
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	1.0		0.0		ns
Switching Characteristics						
t_{DO}	Output Delay After CLKOUT[1]		6.0		6.0	ns
t_{HO}	Output Hold After CLKOUT [1]	1.0		0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, DATA15–0, $\overline{AOE}$, $\overline{ARE}$.

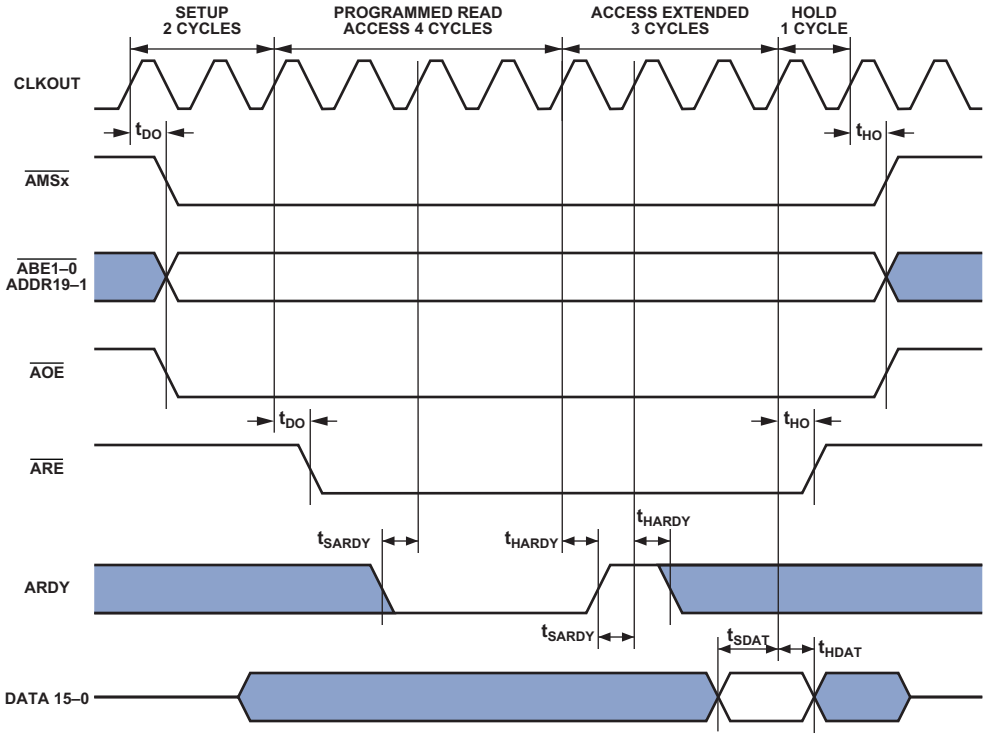


Figure 13. Asynchronous Memory Read Cycle Timing

SDRAM Interface Timing

Table 25. SDRAM Interface Timing[1]

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{SSDAT}	DATA Setup Before CLKOUT	2.1		1.5		ns
t_{HSDAT}	DATA Hold After CLKOUT	0.8		0.8		ns
Switching Characteristics						
t_{DCAD}	Command, ADDR, Data Delay After CLKOUT[2]		6.0		4.0	ns
t_{HCAD}	Command, ADDR, Data Hold After CLKOUT[2]	1.0		1.0		ns
t_{DSDAT}	Data Disable After CLKOUT		6.0		4.0	ns
t_{ENSDAT}	Data Enable After CLKOUT	1.0		1.0		ns
t_{SCLK}	CLKOUT Period[3]	10.0		7.5		ns
t_{SCLKH}	CLKOUT Width High	2.5		2.5		ns
t_{SCLKL}	CLKOUT Width Low	2.5		2.5		ns

[1] SDRAM timing for T_J > 105°C is limited to 100 MHz.
[2] Command pins include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS}$, SA10, SCKE.
[3] Refer to Table 13 on Page 21 for maximum f_{SCLK} at various V_{DDINT}.

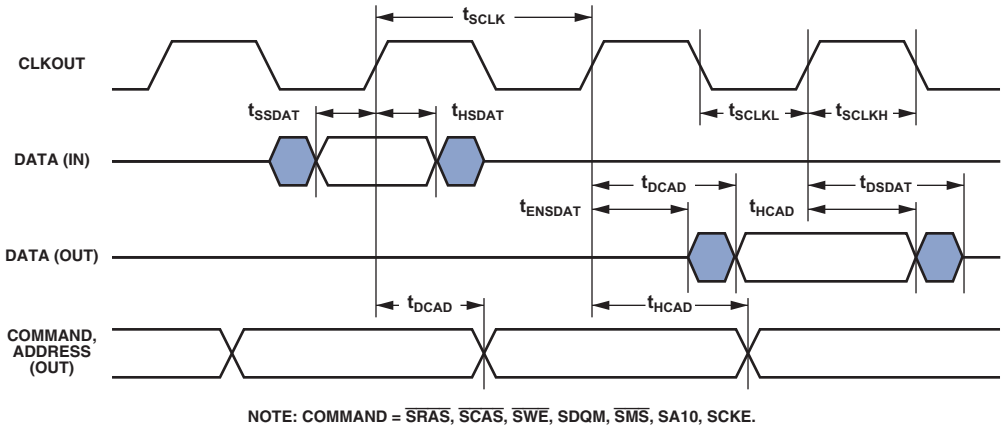


Figure 15. SDRAM Interface Timing

External Port Bus Request and Grant Cycle Timing

Table 26 and Figure 16 describe external port bus request and bus grant operations.

Table 26. External Port Bus Request and Grant Cycle Timing

Parameter	V_{DDEXT} = 1.8 V LQFP/PBGA Packages		V_{DDEXT} = 1.8 V CSP_BGA Package		V_{DDEXT} = 2.5 V/3.3 V All Packages		Unit
	Min	Max	Min	Max	Min	Max	
Timing Requirements							
t_{BS} $\overline{BR}$ Asserted to CLKOUT High Setup	4.6		4.6		4.6		ns
t_{BH} CLKOUT High to $\overline{BR}$ Deasserted Hold Time	1.0		1.0		0.0		ns
Switching Characteristics							
t_{SD} CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Disable		4.5		4.5		4.5	ns
t_{SE} CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Enable		4.5		4.5		4.5	ns
t_{DBG} CLKOUT High to $\overline{BG}$ High Setup		6.0		5.5		3.6	ns
t_{EBG} CLKOUT High to $\overline{BG}$ Deasserted Hold Time		6.0		4.6		3.6	ns
t_{DBH} CLKOUT High to $\overline{BGH}$ High Setup		6.0		5.5		3.6	ns
t_{EBH} CLKOUT High to $\overline{BGH}$ Deasserted Hold Time		6.0		4.6		3.6	ns

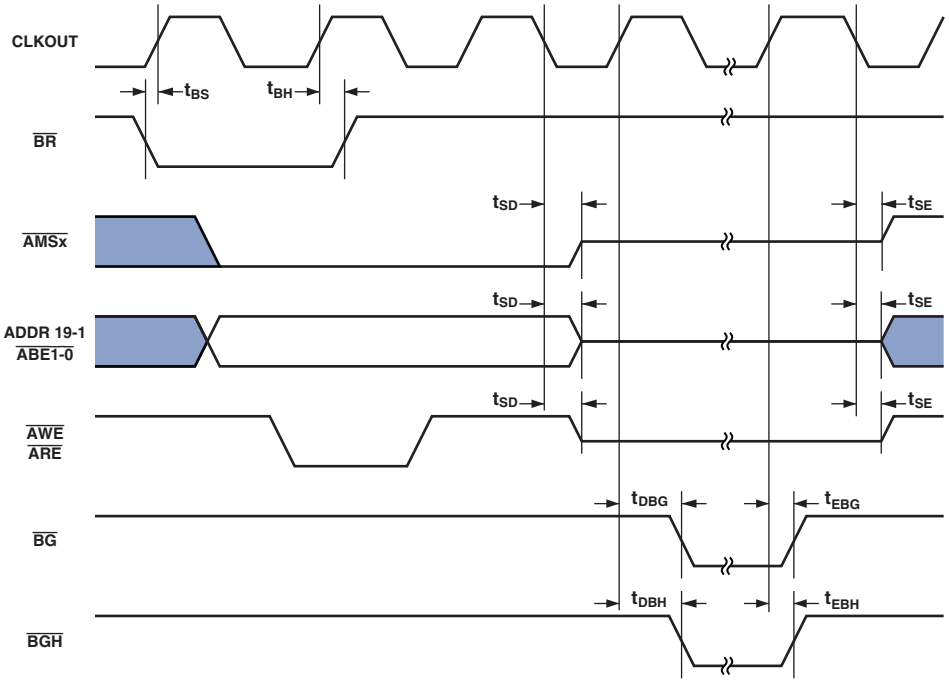


Figure 16. External Port Bus Request and Grant Cycle Timing

Parallel Peripheral Interface Timing

Table 27 and Figure 17 through Figure 22 describe parallel peripheral interface operations.

Table 27. Parallel Peripheral Interface Timing

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Timing Requirements								
t_{PCLKW}	PPI_CLK Width	8.0		8.0		6.0		ns
t_{PCLK}	PPI_CLK Period[1]	20.0		20.0		15.0		ns
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK Edge (Nonsampling Edge for Rx, Sampling Edge for Tx)	6.0		6.0		4.0[2]		ns ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.0[2]		1.0[2]		1.0[2]		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	3.5		3.5		3.5		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	1.5		1.5		1.5		ns
Switching Characteristics—GP Output and Frame Capture Modes								
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		11.0		8.0		8.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	1.7		1.7		1.7		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		11.0		9.0		9.0	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	1.8		1.8		1.8		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$.
[2] Applies when PPI_CONTROL Bit 8 is cleared. See Figure 19 and Figure 22.

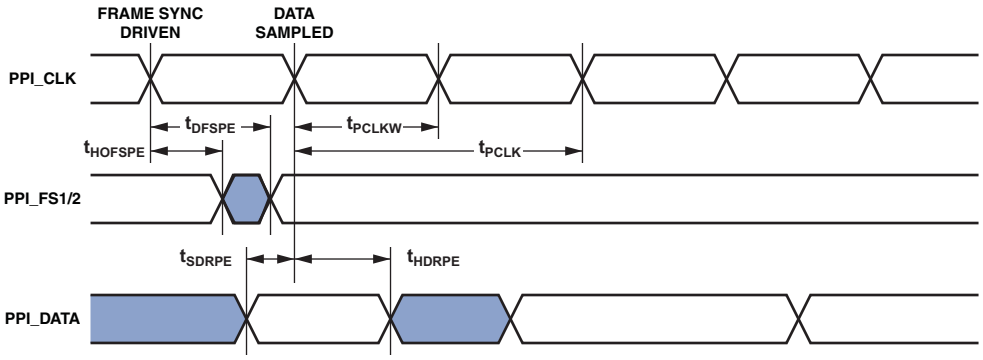


Figure 17. PPI GP Rx Mode with Internal Frame Sync Timing

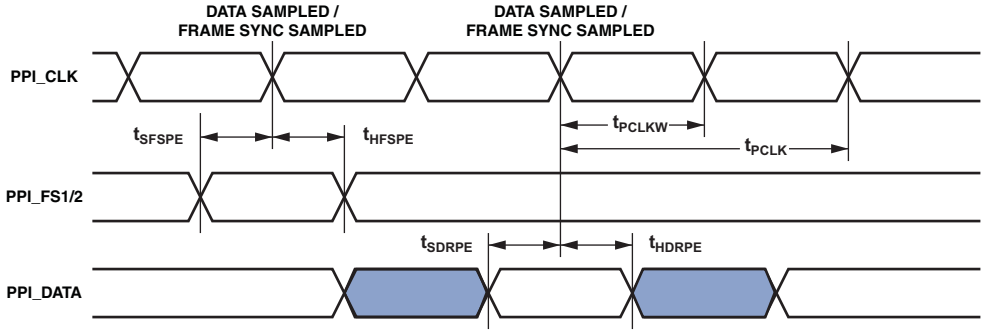


Figure 18. PPI GP Rx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 1)

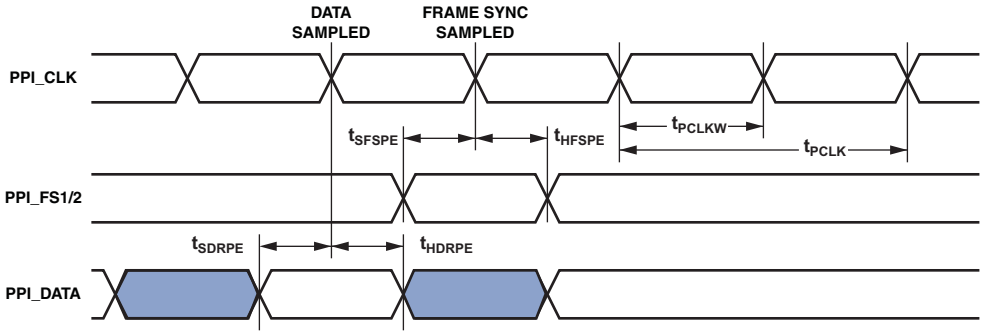


Figure 19. PPI GP Rx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 0)

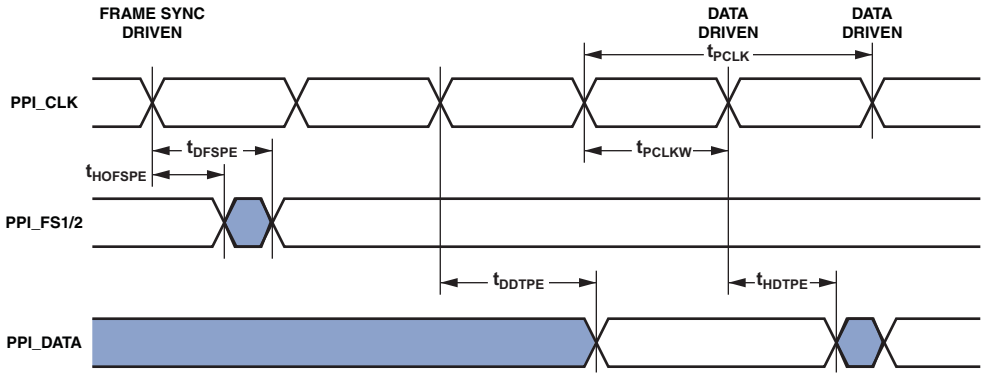


Figure 20. PPI GP Tx Mode with Internal Frame Sync Timing

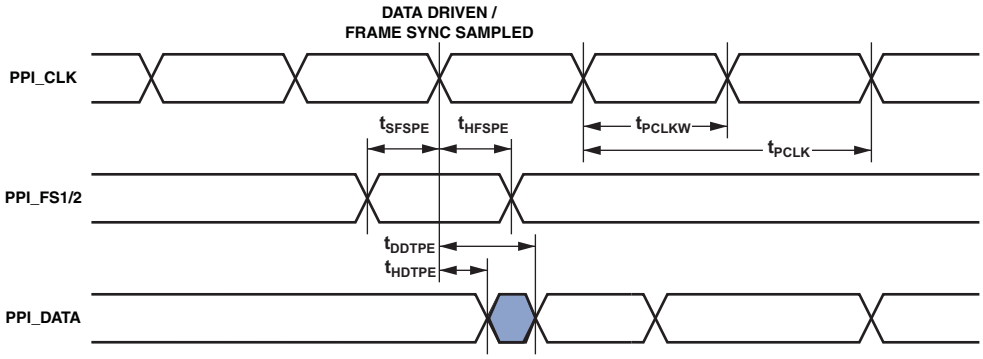


Figure 21. PPI GP Tx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 1)

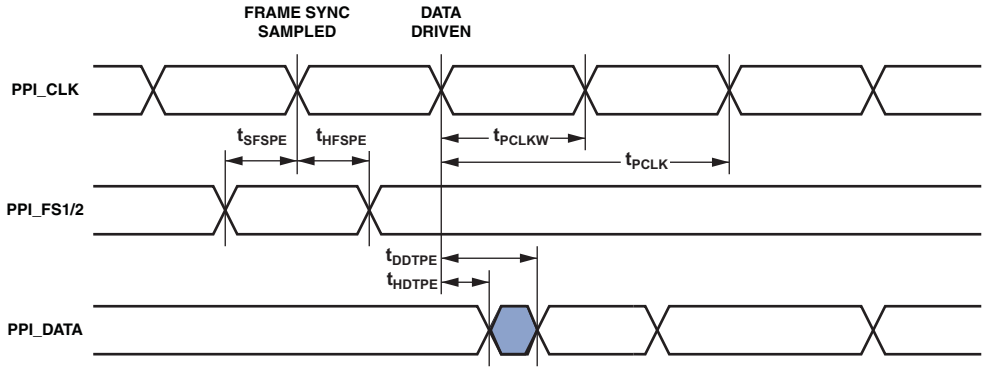


Figure 22. PPI GP Tx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 0)

Serial Peripheral Interface (SPI) Port—Master Timing

Table 32. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Timing Requirements								
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	10.5		9		7.5		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	–1.5		–1.5		–1.5		ns
Switching Characteristics								
t_{SDSCIM}	$\overline{SPISELx}$ Low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISELx}$ High	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)		6		6		6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	–1.0		–1.0		–1.0		ns

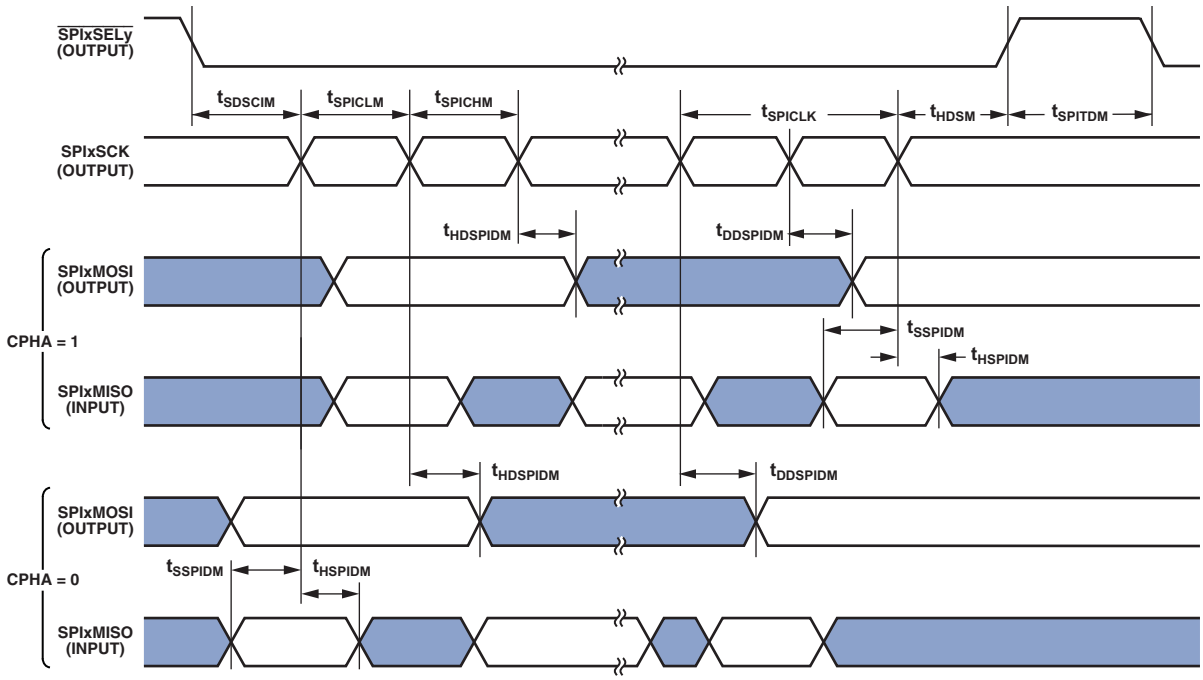


Figure 27. Serial Peripheral Interface (SPI) Port—Master Timing

Timer Clock Timing

Table 35 and Figure 30 describe timer clock timing.

Table 35. Timer Clock Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TODP}	Timer Output Update Delay After PPI_CLK High		12	ns

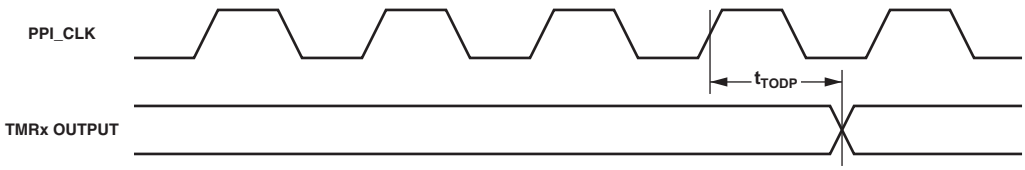


Figure 30. Timer Clock Timing

Timer Cycle Timing

Table 36 and Figure 31 describe timer expired operations. The input signal is asynchronous in width capture mode and external clock mode and has an absolute maximum input frequency of $f_{SCLK}/2$ MHz.

Table 36. Timer Cycle Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Characteristics						
t_{WL}	Timer Pulse Width Low[1]	$1 \times t_{SCLK}$		$1 \times t_{SCLK}$		ns
t_{WH}	Timer Pulse Width High[1]	$1 \times t_{SCLK}$		$1 \times t_{SCLK}$		ns
t_{TIS}	Timer Input Setup Time Before CLKOUT Low[2]	8.0		6.5		ns
t_{TIH}	Timer Input Hold Time After CLKOUT Low[2]	1.5		1.5		ns
Switching Characteristics						
t_{HTO}	Timer Pulse Width Output	$1 \times t_{SCLK}$	$(2^{32}-1) \times t_{SCLK}$	$1 \times t_{SCLK}$	$(2^{32}-1) \times t_{SCLK}$	ns
t_{TOD}	Timer Output Update Delay After CLKOUT High		7.5		6.5	ns

[1] The minimum pulse widths apply for TMRx input pins in width capture and external clock modes. They also apply to the PF1 or PPI_CLK input pins in PWM output mode.
[2] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize programmable flag inputs.

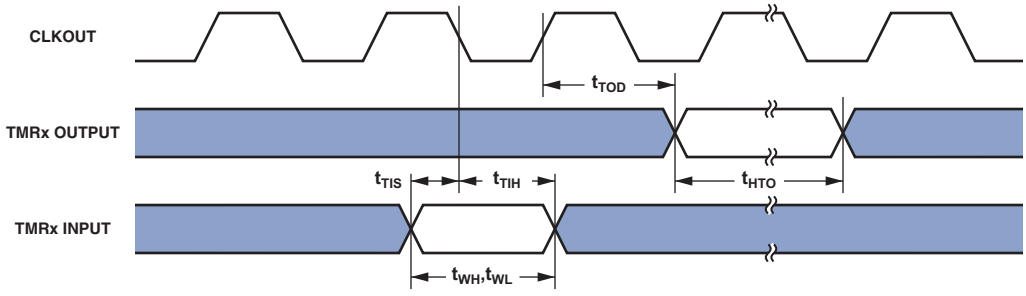


Figure 31. Timer PWM_OUT Cycle Timing

JTAG Test and Emulation Port Timing

Table 37. JTAG Port Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{TCK}	TCK Period	20		20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		4		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	5		5		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width[2] (Measured in TCK Cycles)	4		4		TCK
Switching Characteristics						
t_{DTDO}	TDO Delay from TCK Low		10		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0	12	0	12	ns

[1] System Inputs = DATA15–0, ARDY, TMR2–0, PF15–0, PPI_CLK, RSCLK0–1, RFS0–1, DR0PRI, DR0SEC, TSCLK0–1, TFS0–1, DR1PRI, DR1SEC, MOSI, MISO, SCK, RX, $\overline{RESET}$, NMI, BMODE1–0, $\overline{BR}$, PPI3–0.

[2] 50 MHz maximum.

[3] System Outputs = DATA15–0, ADDR19–1, $\overline{ABE1–0}$, $\overline{AOE}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AMS3–0}$, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SCKE, CLKOUT, SA10, $\overline{SMS}$, TMR2–0, PF15–0, RSCLK0–1, RFS0–1, TSCLK0–1, TFS0–1, DT0PRI, DT0SEC, DT1PRI, DT1SEC, MOSI, MISO, SCK, TX, $\overline{BG}$, $\overline{BGH}$, PPI3–0.

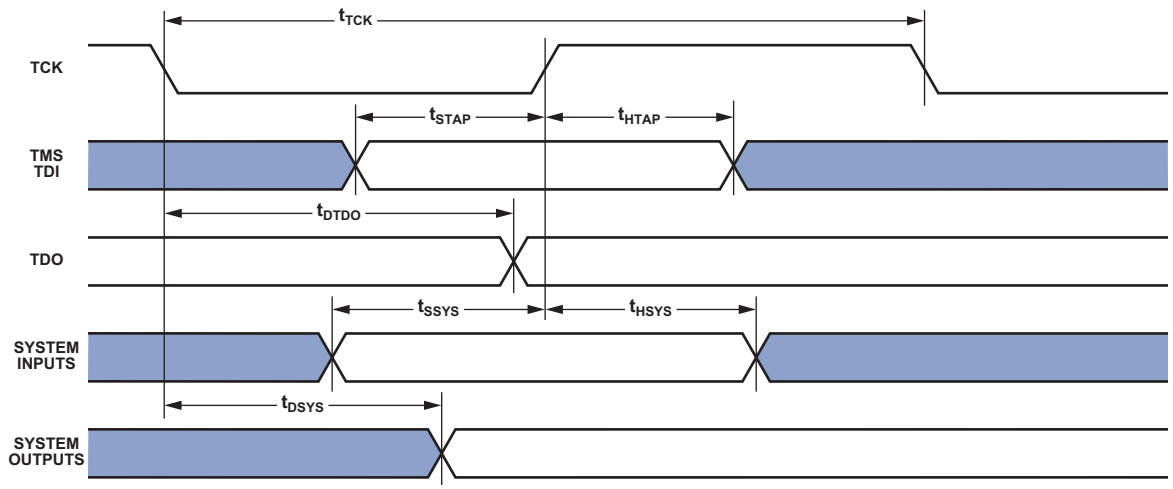


Figure 32. JTAG Port Timing

OUTPUT DRIVE CURRENTS

Figure 33 through Figure 44 show typical current-voltage characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

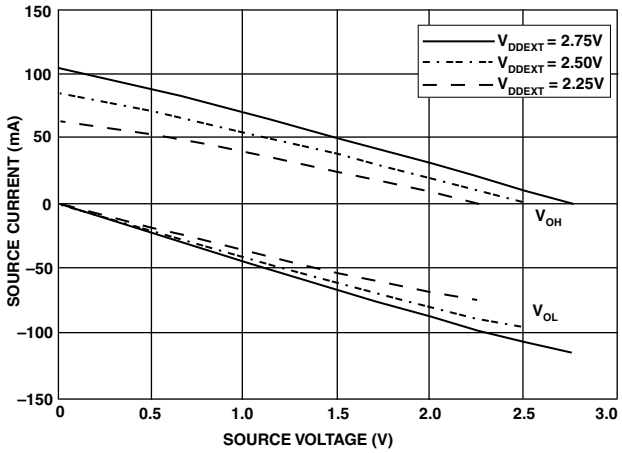


Figure 33. Drive Current A (V_{DDEXT} = 2.5 V)

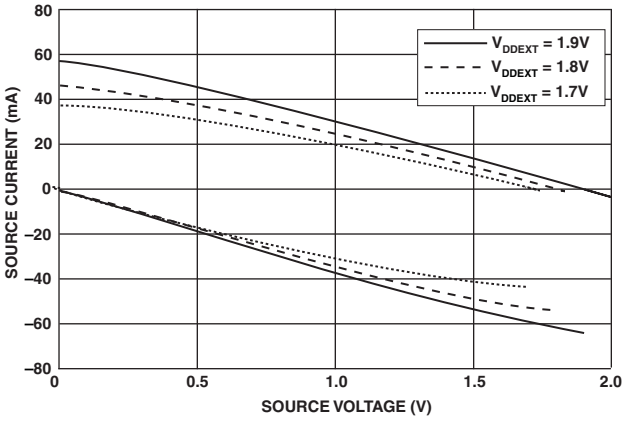


Figure 34. Drive Current A (V_{DDEXT} = 1.8 V)

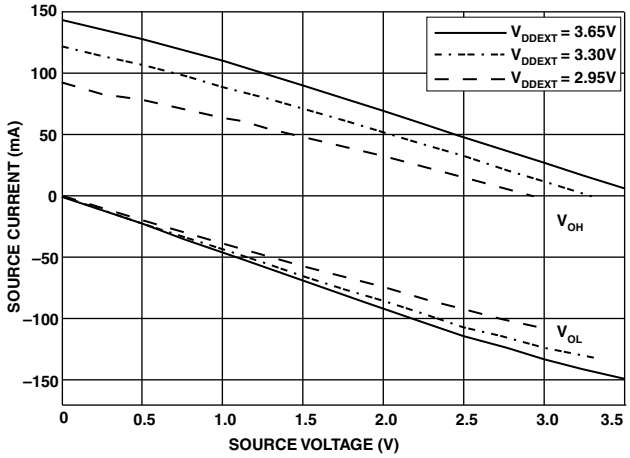


Figure 35. Drive Current A (V_{DDEXT} = 3.3 V)

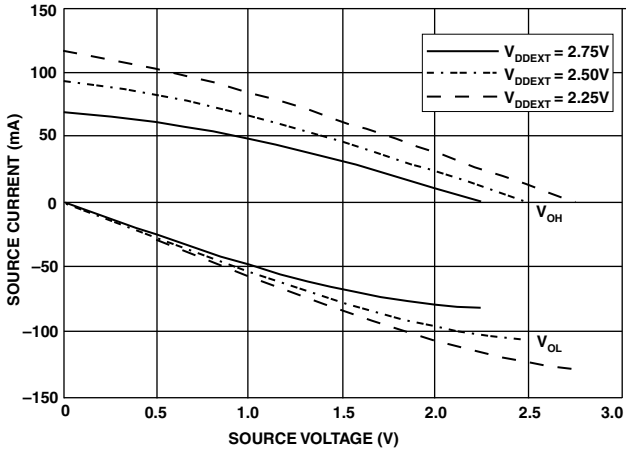


Figure 36. Drive Current B (V_{DDEXT} = 2.5 V)

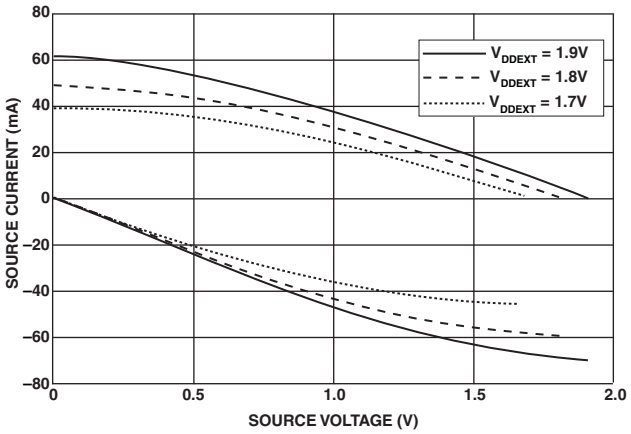


Figure 37. Drive Current B (V_{DDEXT} = 1.8 V)

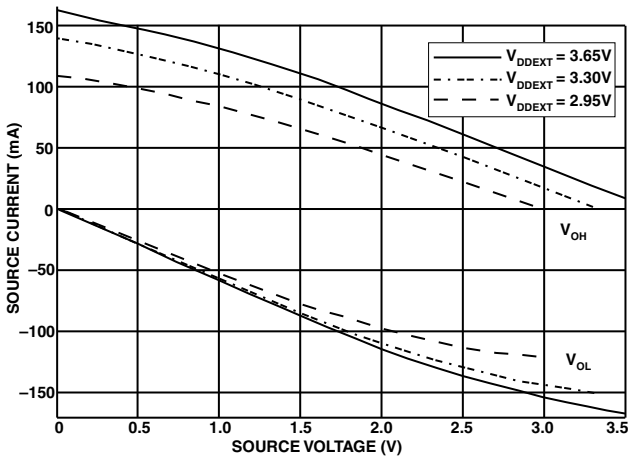
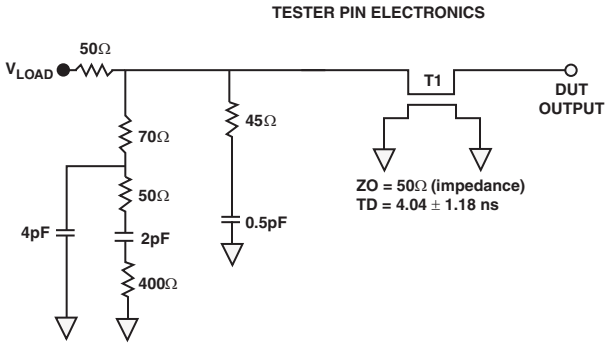


Figure 38. Drive Current B (V_{DDEXT} = 3.3 V)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 47). V_{LOAD} is 0.95 V for V_{DDEXT} (nominal) = 1.8 V or 1.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V. Figure 48 through Figure 59 on Page 48 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 47. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

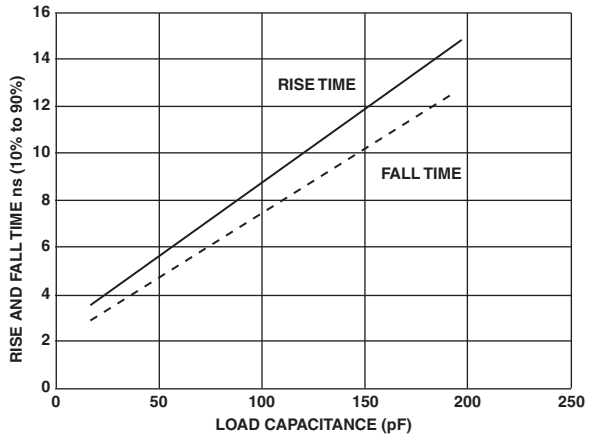


Figure 48. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 1.75 V

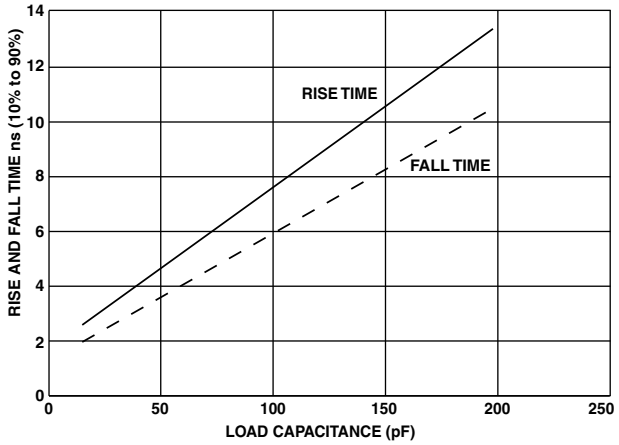


Figure 49. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 2.25 V

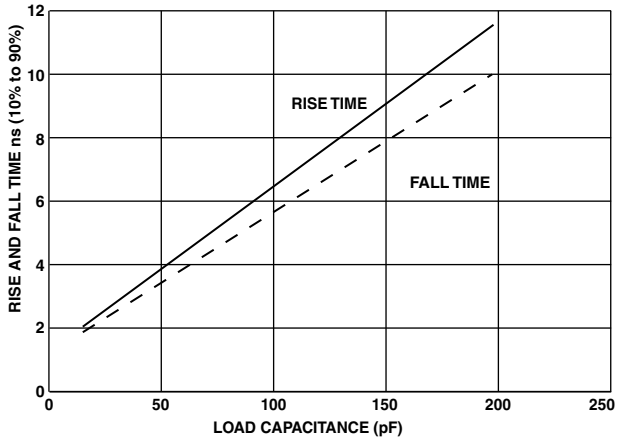


Figure 50. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 3.65 V

Table 46. 176-Lead LQFP Pin Assignment (Numerical by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	GND	41	GND	81	TX	121	ADDR19	161	$\overline{AMS0}$
2	GND	42	GND	82	RX	122	ADDR18	162	ARDY
3	GND	43	GND	83	$\overline{EMU}$	123	ADDR17	163	$\overline{BR}$
4	VROUT1	44	GND	84	$\overline{TRST}$	124	ADDR16	164	SA10
5	VROUT0	45	V_{DDEXT}	85	TMS	125	ADDR15	165	$\overline{SWE}$
6	V_{DDEXT}	46	PF5	86	TDI	126	ADDR14	166	$\overline{SCAS}$
7	GND	47	PF4	87	TDO	127	ADDR13	167	$\overline{SRAS}$
8	GND	48	PF3	88	GND	128	GND	168	V_{DDINT}
9	GND	49	PF2	89	GND	129	GND	169	CLKOUT
10	CLKIN	50	PF1	90	GND	130	GND	170	GND
11	XTAL	51	PF0	91	GND	131	GND	171	V_{DDEXT}
12	V_{DDEXT}	52	V_{DDINT}	92	GND	132	GND	172	$\overline{SMS}$
13	$\overline{RESET}$	53	SCK	93	V_{DDEXT}	133	GND	173	SCKE
14	NMI	54	MISO	94	TCK	134	V_{DDEXT}	174	GND
15	GND	55	MOSI	95	BMODE1	135	ADDR12	175	GND
16	RTXO	56	GND	96	BMODE0	136	ADDR11	176	GND
17	RTXI	57	V_{DDEXT}	97	GND	137	ADDR10		
18	V_{DDRTC}	58	DT1SEC	98	DATA15	138	ADDR9		
19	GND	59	DT1PRI	99	DATA14	139	ADDR8		
20	V_{DDEXT}	60	TFS1	100	DATA13	140	ADDR7		
21	PPI_CLK	61	TSCLK1	101	DATA12	141	ADDR6		
22	PPI0	62	DR1SEC	102	DATA11	142	ADDR5		
23	PPI1	63	DR1PRI	103	DATA10	143	V_{DDINT}		
24	PPI2	64	RFS1	104	DATA9	144	GND		
25	V_{DDINT}	65	RSCLK1	105	DATA8	145	V_{DDEXT}		
26	PPI3	66	V_{DDINT}	106	GND	146	ADDR4		
27	PF15	67	DT0SEC	107	V_{DDEXT}	147	ADDR3		
28	PF14	68	DT0PRI	108	DATA7	148	ADDR2		
29	PF13	69	TFS0	109	DATA6	149	ADDR1		
30	GND	70	GND	110	DATA5	150	$\overline{ABE1}$		
31	V_{DDEXT}	71	V_{DDEXT}	111	V_{DDINT}	151	$\overline{ABE0}$		
32	PF12	72	TSCLK0	112	DATA4	152	$\overline{AWE}$		
33	PF11	73	DR0SEC	113	DATA3	153	$\overline{ARE}$		
34	PF10	74	DR0PRI	114	DATA2	154	$\overline{AOE}$		
35	PF9	75	RFS0	115	DATA1	155	GND		
36	PF8	76	RSCLK0	116	DATA0	156	V_{DDEXT}		
37	PF7	77	TMR2	117	GND	157	V_{DDINT}		
38	PF6	78	TMR1	118	V_{DDEXT}	158	$\overline{AMS3}$		
39	GND	79	TMR0	119	$\overline{BG}$	159	$\overline{AMS2}$		
40	GND	80	V_{DDINT}	120	$\overline{BGH}$	160	$\overline{AMS1}$		

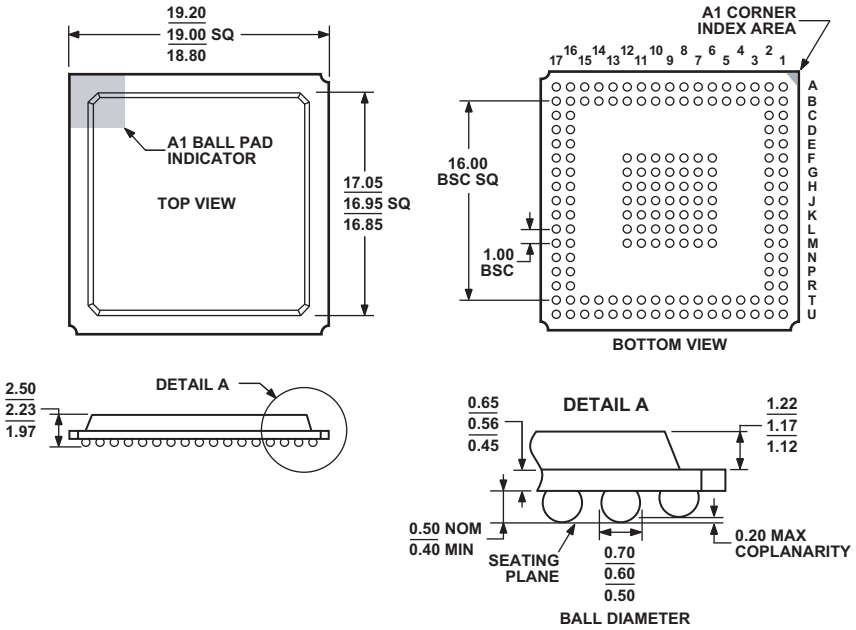


Figure 66. 169-Ball Plastic Ball Grid Array [PBGA]
(B-169)
Dimensions shown in millimeters

AUTOMOTIVE PRODUCTS

The ADBF531W, ADBF532W, and ADBF533W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 48 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 48. Automotive Products

Product Family[1,2]	Temperature Range[3]	Speed Grade (Max)	Package Description	Package Option
ADBF531WBSTZ4xx	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADBF531WBBCZ4xx	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF531WYBCZ4xx	–40°C to +105°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF532WBSTZ4xx	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADBF532WBBCZ4xx	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF532WYBCZ4xx	–40°C to +105°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF533WBBCZ5xx	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADBF533WBBZ5xx	–40°C to +85°C	533 MHz	169-Ball PBGA	B-169
ADBF533WYBCZ4xx	–40°C to +105°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADBF533WYBBZ4xx	–40°C to +105°C	400 MHz	169-Ball PBGA	B-169

[1] Z = RoHS compliant part.
[2] xx denotes silicon revision.
[3] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 20 for junction temperature (T_J) specification which is the only temperature specification.