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Understanding <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

Details

Product Status	Active
Туре	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	500MHz
Non-Volatile Memory	ROM (1kB)
On-Chip RAM	148kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-BBGA
Supplier Device Package	169-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf533sbbz500

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

GENERAL DESCRIPTION

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are members of the Blackfin[®] family of products, incorporating the Analog Devices, Inc./Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISClike microprocessor instruction set, and single instruction, multiple data (SIMD) multimedia capabilities into a single instruction set architecture.

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are completely code and pin-compatible, differing only with respect to their performance and on-chip memory. Specific performance and memory configurations are shown in Table 1.

Table 1. Processor Comparison

Features		ADSP-BF531	ADSP-BF532	ADSP-BF533
SP	ORTs	2	2	2
UA	RT	1	1	1
SP		1	1	1
GP	Timers	3	3	3
Wa	atchdog Timers	1	1	1
RTC		1	1	1
Parallel Peripheral Interface		1	1	1
GP	lOs	16	16	16
ion	L1 Instruction SRAM/Cache	16K bytes	16K bytes	16K bytes
urat	L1 Instruction SRAM	16K bytes	32K bytes	64K bytes
fig	L1 Data SRAM/Cache	16K bytes	32K bytes	32K bytes
õ	L1 Data SRAM			32K bytes
ory	L1 Scratchpad	4K bytes	4K bytes	4K bytes
Memo	L3 Boot ROM	1K bytes	1K bytes	1K bytes
Maximum Speed Grade		400 MHz	400 MHz	600 MHz
Package Options: CSP_BGA Plastic BGA		160-Ball 169-Ball 176-Lead	160-Ball 169-Ball 176-Lead	160-Ball 169-Ball 176-Lead
	11			

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

PORTABLE LOW POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. Blackfin processors are designed in a low power and low voltage design methodology and feature dynamic power management—the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. Varying the voltage and frequency can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This translates into longer battery life for portable appliances.

SYSTEM INTEGRATION

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are highly integrated system-on-a-chip solutions for the next generation of digital communication and consumer multimedia applications. By combining industry-standard interfaces with a high performance signal processing core, users can develop cost-effective solutions quickly without the need for costly external components. The system peripherals include a UART port, an SPI port, two serial ports (SPORTs), four general-purpose timers (three with PWM capability), a real-time clock, a watchdog timer, and a parallel peripheral interface.

PROCESSOR PERIPHERALS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors contain a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the functional block diagram in Figure 1 on Page 1). The generalpurpose peripherals include functions such as UART, timers with PWM (pulse-width modulation) and pulse measurement capability, general-purpose I/O pins, a real-time clock, and a watchdog timer. This set of functions satisfies a wide variety of typical system support needs and is augmented by the system expansion capabilities of the part. In addition to these generalpurpose peripherals, the processors contain high speed serial and parallel ports for interfacing to a variety of audio, video, and modem codec functions; an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources; and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

All of the peripherals, except for general-purpose I/O, real-time clock, and timers, are supported by a flexible DMA structure. There is also a separate memory DMA channel dedicated to data transfers between the processor's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses running at up to 133 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The processors include an on-chip voltage regulator in support of the processor's dynamic power management capability. The voltage regulator provides a range of core voltage levels from V_{DDEXT} . The voltage regulator can be bypassed at the user's discretion.

 CEC interrupt pending register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but can be read while in supervisor mode.

The SIC allows further control of event processing by providing three 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in Table 3.

- SIC interrupt mask register (SIC_IMASK) This register controls the masking and unmasking of each peripheral interrupt event. When a bit is set in this register, that peripheral event is unmasked and is processed by the system when asserted. A cleared bit in this register masks the peripheral event, preventing the processor from servicing the event.
- SIC interrupt status register (SIC_ISR) As multiple peripherals can be mapped to a single event, this register allows the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt, and a cleared bit indicates the peripheral is not asserting the event.
- SIC interrupt wakeup enable register (SIC_IWR) By enabling the corresponding bit in this register, a peripheral can be configured to wake up the processor, should the core be idled when the event is generated. See Dynamic Power Management on Page 11.

Because multiple interrupt sources can map to a single generalpurpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC recognizes and queues the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

DMA CONTROLLERS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have multiple, independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the SPORTs, SPI port, UART, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The DMA controller supports both 1-dimensional (1-D) and 2dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ± 32 K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, autorefreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two pairs of memory DMA channels provided for transfers between the various memories of the processor system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

REAL-TIME CLOCK

The processor real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors. The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60 second counter, a 60 minute counter, a 24 hour counter, and a 32,768 day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. The two alarms are time of day and a day and time of that day.

The stopwatch function counts down from a programmed value, with one second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like other peripherals, the RTC can wake up the processor from sleep mode upon generation of any RTC wakeup event. Additionally, an RTC wakeup event can wake up the processor from deep sleep mode, and wake up the on-chip internal voltage regulator from a powered-down state.

Connect RTC pins RTXI and RTXO with external components as shown in Figure 6.



SUGGESTED COMPONENTS: X1 = ECLIPTEK EC38J (THROUGH-HOLE PACKAGE) OR EPSON MC405 12 pF LOAD (SURFACE-MOUNT PACKAGE) C1 = 22 pF C2 = 22 pF R1 = 10 MΩ

NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

Figure 6. External Components for RTC

WATCHDOG TIMER

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors include a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK), at a maximum frequency of f_{SCLK} .

TIMERS

There are four general-purpose programmable timer units in the ADSP-BF531/ADSP-BF532/ADSP-BF533 processors. Three timers have an external pin that can be configured either as a pulse-width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the PF1 pin (TACLK), an external clock input to the PP1_CLK pin (TMRCLK), or to the internal SCLK.

The timer units can be used in conjunction with the UART to measure the width of the pulses in the data stream to provide an autobaud detect function for a serial channel.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the three general-purpose programmable timers, a fourth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

SERIAL PORTS (SPORTs)

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- I²S capable operation.
- Bidirectional operation Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I²S stereo audio.
- Buffered (8-deep) transmit and receive ports Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from ($f_{SCLK}/131,070$) Hz to ($f_{SCLK}/2$) Hz.
- Word length Each SPORT supports serial data words from 3 bits to 32 bits in length, transferred most-significant-bit first or least-significant-bit first.
- Framing Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.

As shown in Figure 9, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a user programmable 0.5× to 64× multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 10×, but it can be modified by a software instruction sequence. On-the-fly frequency changes can be effected by simply writing to the PLL_DIV register.



Figure 9. Frequency Modification Methods

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 6 illustrates typical system clock ratios.

Table 6.	Example System	Clock Ratios
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Signal Name	Divider Ratio	Example Frequency Ratios (MHz)		
SSEL3-0	VCO/SCLK	VCO	SCLK	
0001	1:1	100	100	
0101	5:1	400	80	
1010	10:1	500	50	

The maximum frequency of the system clock is f_{SCLK} . The divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK} . The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV). When the SSEL value is changed, it affects all of the peripherals that derive their clock signals from the SCLK signal.

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 7. This programmable core clock capability is useful for fast core frequency modifications.

Table 7. Core Clock Ratios

Signal Name	Divider Ratio	Example Frequency Ratios (MHz) VCO CCLK		
CSEL1-0	VCO/CCLK			
00	1:1	300	300	
01	2:1	300	150	
10	4:1	400	100	
11	8:1	200	25	

BOOTING MODES

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors have two mechanisms (listed in Table 8) for automatically loading internal L1 instruction memory after a reset. A third mode is provided to execute from external memory, bypassing the boot sequence.

Table 8. Booting Modes

BMODE1-0	Description
00	Execute from 16-bit external memory (bypass boot ROM)
01	Boot from 8-bit or 16-bit FLASH
10	Boot from serial master connected to SPI
11	Boot from serial slave EEPROM/flash (8-,16-, or 24- bit address range, or Atmel AT45DB041, AT45DB081, or AT45DB161serial flash)

The BMODE pins of the reset configuration register, sampled during power-on resets and software-initiated resets, implement the following modes:

- Execute from 16-bit external memory Execution starts from address 0x2000 0000 with 16-bit packing. The boot ROM is bypassed in this mode. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).
- Boot from 8-bit or 16-bit external flash memory The flash boot routine located in boot ROM memory space is set up using asynchronous Memory Bank 0. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).
- Boot from SPI serial EEPROM/flash (8-, 16-, or 24-bit addressable, or Atmel AT45DB041, AT45DB081, or AT45DB161) The SPI uses the PF2 output pin to select a single SPI EEPROM/flash device, submits a read command and successive address bytes (0x00) until a valid 8-, 16-, or 24-bit addressable EEPROM/flash device is detected, and begins clocking data into the processor at the beginning of L1 instruction memory.
- Boot from SPI serial master The Blackfin processor operates in SPI slave mode and is configured to receive the bytes of the LDR file from an SPI host (master) agent. To hold off the host device from transmitting while the boot ROM is busy, the Blackfin processor asserts a GPIO pin, called host wait (HWAIT), to signal the host device not to send any

more bytes until the flag is deasserted. The GPIO pin is chosen by the user and this information is transferred to the Blackfin processor via bits[10:5] of the FLAG header in the LDR image.

For each of the boot modes, a 10-byte header is first read from an external memory device. The header specifies the number of bytes to be transferred and the memory destination address. Multiple memory blocks can be loaded by any boot sequence. Once all blocks are loaded, program execution commences from the start of L1 instruction SRAM.

In addition, Bit 4 of the reset configuration register can be set by application code to bypass the normal boot sequence during a software reset. For this case, the processor jumps directly to the beginning of L1 instruction memory.

INSTRUCTION SET DESCRIPTION

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both user (algorithm/application code) and supervisor (O/S kernel, device drivers, debuggers, ISRs) modes of operation, allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/CPU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU + two load/store + two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4G byte memory space, providing a simplified programming model.
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data types; and separate user and supervisor stack pointers.
- Code density enhancements, which include intermixing of 16-bit and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded in 16 bits.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore[®] Embedded Studio and/or VisualDSP++[®]), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse[™] framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/ cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite[®] evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders[®], which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of Cross-Core Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Table 9. Pin Descriptions (Continued)

Pin Name	Туре	Function	Driver Type ¹
RFS1	I/O	SPORT1 Receive Frame Sync	С
DR1PRI	I	SPORT1 Receive Data Primary	
DR1SEC	I	SPORT1 Receive Data Secondary	
TSCLK1	I/O	SPORT1 Transmit Serial Clock	D
TFS1	I/O	SPORT1 Transmit Frame Sync	с
DT1PRI	0	SPORT1 Transmit Data Primary	С
DT1SEC	0	SPORT1 Transmit Data Secondary	С
UART Port			
RX	I	UART Receive	
ТХ	0	UART Transmit	с
Real-Time Clock			
RTXI	I	RTC Crystal Input (This pin should be pulled low when not used.)	
RTXO	0	RTC Crystal Output (Does not three-state in hibernate.)	
Clock			
CLKIN	I	Clock/Crystal Input (This pin needs to be at a level or clocking.)	
XTAL	0	Crystal Output	
Mode Controls			
RESET	I	Reset (This pin is always active during core power-on.)	
NMI	I	Nonmaskable Interrupt (This pin should be pulled low when not used.)	
BMODE1-0	I	Boot Mode Strap (These pins must be pulled to the state required for the desired boot mode.)	
Voltage Regulator			
VROUT1-0	0	External FET Drive (These pins should be left unconnected when unused and are driven high during hibernate.)	
Supplies			
V _{DDEXT}	Р	I/O Power Supply	
V _{DDINT}	Р	Core Power Supply	
V _{DDRTC}	Р	Real-Time Clock Power Supply (This pin should be connected to $V_{\mbox{DDEXT}}$ when not used and should remain powered at all times.)	
GND	G	External Ground	

¹Refer to Figure 33 on Page 43 to Figure 44 on Page 44.

ELECTRICAL CHARACTERISTICS

				400 MHz¹		500 MH:	z/533 MHz/	500 MHz ²	
Parameter		Test Conditions	Min	Typical	Max	Min	Typical	Max	Unit
V _{OH}	High Level Output Voltage ³	$V_{DDEXT} = 1.75 V, I_{OH} = -0.5 mA$ $V_{DDEXT} = 2.25 V, I_{OH} = -0.5 mA$ $V_{DDEXT} = 3.0 V, I_{OH} = -0.5 mA$	1.5 1.9 2.4			1.5 1.9 2.4			V V V
V _{OL}	Low Level Output Voltage ³	$V_{DDEXT} = 1.75 \text{ V}, I_{OL} = 2.0 \text{ mA}$ $V_{DDEXT} = 2.25 \text{ V}/3.0 \text{ V},$ $I_{OL} = 2.0 \text{ mA}$			0.2 0.4			0.2 0.4	V V
I _{IH}	High Level Input Current ⁴	$V_{DDEXT} = Max, V_{IN} = V_{DD} Max$			10.0			10.0	μA
I _{IHP}	High Level Input Current JTAG⁵	$V_{DDEXT} = Max, V_{IN} = V_{DD} Max$			50.0			50.0	μA
I _{IL} ⁶	Low Level Input Current ⁴	$V_{DDEXT} = Max, V_{IN} = 0 V$			10.0			10.0	μA
I _{OZH}	Three-State Leakage Current ⁷	$V_{DDEXT} = Max, V_{IN} = V_{DD} Max$			10.0			10.0	μΑ
I _{OZL} ⁶	Three-State Leakage Current ⁷	$V_{DDEXT} = Max, V_{IN} = 0 V$			10.0			10.0	μΑ
C _{IN}	Input Capacitance ⁸	$f_{IN} = 1 \text{ MHz}, T_{AMBIENT} = 25^{\circ}\text{C},$ $V_{IN} = 2.5 \text{ V}$		4	8 ⁹		4	8 ⁹	pF
I _{DDDEEPSLEEP} ¹⁰	V _{DDINT} Current in Deep Sleep Mode	$V_{DDINT} = 1.0 V, f_{CCLK} = 0 MHz,$ T _J = 25°C, ASF = 0.00		7.5			32.5		mA
IDDSLEEP	V _{DDINT} Current in Sleep Mode	V _{DDINT} = 0.8 V, T _J = 25°C, SCLK = 25 MHz			10			37.5	mA
I _{DD-TYP} ¹¹	V _{DDINT} Current	$V_{DDINT} = 1.14 V, f_{CCLK} = 400 MHz, T_{J} = 25^{\circ}C$		125			152		mA
I _{DD-TYP} ¹¹	V _{DDINT} Current	$V_{DDINT} = 1.2 \text{ V}, f_{CCLK} = 500 \text{ MHz},$ $T_J = 25^{\circ}\text{C}$					190		mA
I _{DD-TYP} ¹¹	V _{DDINT} Current	$V_{DDINT} = 1.2 \text{ V}, f_{CCLK} = 533 \text{ MHz},$ $T_J = 25^{\circ}\text{C}$					200		mA
I _{DD-TYP} ¹¹	V _{DDINT} Current	$V_{DDINT} = 1.3 V$, $f_{CCLK} = 600 MHz$, $T_{J} = 25^{\circ}C$					245		mA
I _{DDHIBERNATE} ¹⁰	V _{DDEXT} Current in Hibernate State	$V_{DDEXT} = 3.6 V$, CLKIN = 0 MHz, T _J = Max, voltage regulator off ($V_{DDINT} = 0 V$)		50	100		50	100	μΑ
I _{DDRTC}	V _{DDRTC} Current	$V_{DDRTC} = 3.3 V, T_J = 25^{\circ}C$		20			20		μA
I _{DDDEEPSLEEP} ¹⁰	V _{DDINT} Current in Deep Sleep Mode	$f_{CCLK} = 0 MHz$		6	Table 15		16	Table 14	mA
I _{DD-INT}	V _{DDINT} Current	f _{CCLK} > 0 MHz			I _{DDDEEPSLEEP} +(Table 17 × ASF)			I _{DDDEEPSLEEP} + (Table 17 × ASF)	mA

¹ Applies to all 400 MHz speed grade models. See Ordering Guide on Page 63.
 ² Applies to all 500 MHz, 533 MHz, and 600 MHz speed grade models. See Ordering Guide on Page 63.

³ Applies to output and bidirectional pins.

⁴Applies to input pins except JTAG inputs.

SDRAM Interface Timing

Table 25. SDRAM Interface Timing¹

		VDDEXT	-= 1.8 V	V _{DDEXT} = 2	2.5 V/3.3 V	
Paramet	Parameter		Max	Min	Max	Unit
Timing R	equirements					
t _{SSDAT}	DATA Setup Before CLKOUT	2.1		1.5		ns
t _{HSDAT}	DATA Hold After CLKOUT	0.8		0.8		ns
Switching	g Characteristics					
t _{DCAD}	Command, ADDR, Data Delay After CLKOUT ²		6.0		4.0	ns
t _{HCAD}	Command, ADDR, Data Hold After CLKOUT ²	1.0		1.0		ns
t _{DSDAT}	Data Disable After CLKOUT		6.0		4.0	ns
t _{ensdat}	Data Enable After CLKOUT	1.0		1.0		ns
t _{SCLK}	CLKOUT Period ³	10.0		7.5		ns
t _{SCLKH}	CLKOUT Width High	2.5		2.5		ns
t _{SCLKL}	CLKOUT Width Low	2.5		2.5		ns

 1 SDRAM timing for T_J > 105°C is limited to 100 MHz.

² Command pins include: SRAS, SCAS, SWE, SDQM, SMS, SA10, SCKE.

 3 Refer to Table 13 on Page 21 for maximum f_{SCLK} at various $V_{DDINT}.$



NOTE: COMMAND = SRAS, SCAS, SWE, SDQM, SMS, SA10, SCKE.

Figure 15. SDRAM Interface Timing

JTAG Test and Emulation Port Timing

Table 37. JTAG Port Timing

		V _{DD}	_{EXT} = 1.8 V	V _{DDEXT} = 2	2.5 V/3.3 V	
Parameter		Min	Max	Min	Max	Unit
Timing	Requirements					
t _{TCK}	TCK Period	20		20		ns
t _{STAP}	TDI, TMS Setup Before TCK High	4		4		ns
t _{HTAP}	TDI, TMS Hold After TCK High	4		4		ns
t _{ssys}	System Inputs Setup Before TCK High ¹	4		4		ns
t _{HSYS}	System Inputs Hold After TCK High ¹	5		5		ns
t _{TRSTW}	TRST Pulse Width ² (Measured in TCK Cycles)	4		4		ТСК
Switching Characteristics						
t _{DTDO}	TDO Delay from TCK Low		10		10	ns
t _{DSYS}	System Outputs Delay After TCK Low ³	0	12	0	12	ns

¹ System Inputs = DATA15-0, ARDY, TMR2-0, PF15-0, PPI_CLK, RSCLK0-1, RFS0-1, DR0PRI, DR0SEC, TSCLK0-1, TFS0-1, DR1PRI, DR1SEC, MOSI, MISO, SCK, RX, RESET, NMI, BMODE1-0, BR, PPI3-0.

² 50 MHz maximum.

³ System Outputs = DATA15-0, ADDR19-1, ABE1-0, AOE, ARE, AWE, AMS3-0, SRAS, SCAS, SWE, SCKE, CLKOUT, SA10, SMS, TMR2-0, PF15-0, RSCLK0-1, RFS0-1, TSCLK0-1, TFS0-1, DT0PRI, DT0SEC, DT1PRI, DT1SEC, MOSI, MISO, SCK, TX, BG, BGH, PPI3-0.



Figure 32. JTAG Port Timing







Figure 40. Drive Current C ($V_{DDEXT} = 1.8 V$)



Figure 41. Drive Current C ($V_{DDEXT} = 3.3 V$)



Figure 42. Drive Current D ($V_{DDEXT} = 2.5 V$)







Figure 44. Drive Current D ($V_{DDEXT} = 3.3 V$)

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 45 shows the measurement point for ac measurements (except output enable/disable). The measurement point V_{MEAS} is 0.95 V for V_{DDEXT} (nominal) = 1.8 V or 1.5 V for V_{DDEXT} (nominal) = 2.5 V/ 3.3 V.



Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 46.

The time $t_{ENA_MEASURED}$ is the interval, from when the reference signal switches, to when the output voltage reaches V_{TRIP} (high) or V_{TRIP} (low).

For V_{DDEXT} (nominal) = 1.8 V—V_{TRIP} (high) is 1.3 V and V_{TRIP} (low) is 0.7 V.

For V_{DDEXT} (nominal) = 2.5 V/3.3 V—V_{TRIP} (high) is 2.0 V and V_{TRIP} (low) is 1.0 V.

Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the V_{TRIP} (high) or V_{TRIP} (low) trip voltage.

Time t_{ENA} is calculated as shown in the equation:

 $t_{ENA} = t_{ENA_MEASURED} - t_{TRIP}$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 45.

$$t_{DIS} = t_{DIS_MEASURED} - t_{DECAY}$$

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load C_L and the load current I_I . This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V) / I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L , and with ΔV equal to 0.1 V for V_{DDEXT} (nominal) = 1.8 V or 0.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V.

The time $t_{DIS_MEASURED}$ is the interval from when the reference signal switches, to when the output voltage decays ΔV from the measured output high or output low voltage.



Figure 46. Output Enable/Disable

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the processor's output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time is t_{DECAY} plus the various output disable times as specified in the Timing Specifications on Page 27 (for example t_{DSDAT} for an SDRAM write cycle as shown in SDRAM Interface Timing on Page 30).



Figure 51. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 1.75 V



Figure 52. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 2.25 V



Figure 53. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 3.65 V



Figure 54. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 1.75 V



Figure 55. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 2.25 V



Figure 56. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 3.65 V



Figure 57. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at $V_{DDEXT} = 1.75 V$



Figure 58. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at V_{DDEXT} = 2.25 V



Figure 59. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at V_{DDEXT} = 3.65 V

THERMAL CHARACTERISTICS

To determine the junction temperature on the application printed circuit board, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

 T_J = Junction temperature (°C).

 T_{CASE} = Case temperature (°C) measured by customer at top center of package.

 Ψ_{JT} = From Table 38 through Table 40.

 P_D = Power dissipation (see the power dissipation discussion and the tables on 23 for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_I by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

 T_A = ambient temperature (°C).

In Table 38 through Table 40, airflow measurements comply with JEDEC standards JESD51–2 and JESD51–6, and the junction-to-board measurement complies with JESD51–8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Thermal resistance θ_{JA} in Table 38 through Table 40 is the figure of merit relating to performance of the package and board in a convective environment. θ_{JMA} represents the thermal resistance under two conditions of airflow. Ψ_{JT} represents the correlation between T_J and T_{CASE} .

Table 38. Thermal Characteristics for BC-160 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	27.1	°C/W
θ_{JMA}	1 Linear m/s Airflow	23.85	°C/W
θ_{JMA}	2 Linear m/s Airflow	22.7	°C/W
θ_{JC}	Not Applicable	7.26	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.14	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.26	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.35	°C/W

Table 39. Thermal Characteristics for ST-176-1 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	34.9	°C/W
θ_{JMA}	1 Linear m/s Airflow	33.0	°C/W
θ_{JMA}	2 Linear m/s Airflow	32.0	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.50	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.75	°C/W
$\Psi_{ m JT}$	2 Linear m/s Airflow	1.00	°C/W

Table 40. Thermal Characteristics for B-169 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	22.8	°C/W
θ_{JMA}	1 Linear m/s Airflow	20.3	°C/W
θ_{JMA}	2 Linear m/s Airflow	19.3	°C/W
θ_{JC}	Not Applicable	10.39	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.59	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.88	°C/W
Ψ_{JT}	2 Linear m/s Airflow	1.37	°C/W

169-BALL PBGA BALL ASSIGNMENT

Table 43 lists the PBGA ball assignment by signal. Table 44 onPage 54 lists the PBGA ball assignment by ball number.

Table 43	169-Ball PBGA Ba	ll Assignment (Al	phabetical by Signal)
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Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
ABEO	H16	DATA4	U12	GND	К9	RTXI	A10	V _{DDEXT}	K6
ABE1	H17	DATA5	U11	GND	K10	RTXO	A11	V _{DDEXT}	L6
ADDR1	J16	DATA6	T10	GND	K11	RX	T1	V _{DDEXT}	M6
ADDR2	J17	DATA7	U10	GND	L7	SA10	B15	V _{DDEXT}	M7
ADDR3	K16	DATA8	Т9	GND	L8	SCAS	A16	V _{DDEXT}	M8
ADDR4	K17	DATA9	U9	GND	L9	SCK	D1	V _{DDEXT}	T2
ADDR5	L16	DATA10	Т8	GND	L10	SCKE	B14	VROUT0	B12
ADDR6	L17	DATA11	U8	GND	L11	SMS	A17	VROUT1	B13
ADDR7	M16	DATA12	U7	GND	M9	SRAS	A15	XTAL	A13
ADDR8	M17	DATA13	T7	GND	T16	SWE	B17		
ADDR9	N17	DATA14	U6	MISO	E2	тск	U4		
ADDR10	N16	DATA15	T6	MOSI	E1	TDI	U3		
ADDR11	P17	DR0PRI	M2	NMI	B11	TDO	T4		
ADDR12	P16	DR0SEC	M1	PF0	D2	TFS0	L1		
ADDR13	R17	DR1PRI	H1	PF1	C1	TFS1	G2		
ADDR14	R16	DR1SEC	H2	PF2	B1	TMR0	R1		
ADDR15	T17	DTOPRI	K2	PF3	C2	TMR1	P2		
ADDR16	U15	DT0SEC	K1	PF4	A1	TMR2	P1		
ADDR17	T15	DT1PRI	F1	PF5	A2	TMS	T3		
ADDR18	U16	DT1SEC	F2	PF6	B3	TRST	U2		
ADDR19	T14	EMU	U1	PF7	A3	TSCLK0	L2		
AMS0	D17	GND	B16	PF8	B4	TSCLK1	G1		
AMS1	E16	GND	F11	PF9	A4	тх	R2		
AMS2	E17	GND	G7	PF10	B5	VDD	F12		
AMS3	F16	GND	G8	PF11	A5	VDD	G12		
AOE	F17	GND	G9	PF12	A6	VDD	H12		
ARDY	C16	GND	G10	PF13	B6	VDD	J12		
ARE	G16	GND	G11	PF14	A7	VDD	K12		
AWE	G17	GND	H7	PF15	B7	VDD	L12		
BG	T13	GND	H8	PPI_CLK	B10	VDD	M10		
BGH	U17	GND	H9	PPIO	B9	VDD	M11		
BMODE0	U5	GND	H10	PPI1	A9	VDD	M12		
BMODE1	T5	GND	H11	PPI2	B8	V _{DDEXT}	B2		
BR	C17	GND	J7	PPI3	A8	V _{DDEXT}	F6		
CLKIN	A14	GND	J8	RESET	A12	V _{DDEXT}	F7		
CLKOUT	D16	GND	J9	RFS0	N1	V _{DDEXT}	F8		
DATA0	U14	GND	J10	RFS1	J1	V _{DDEXT}	F9		
DATA1	T12	GND	J11	RSCLK0	N2	V _{DDEXT}	G6		
DATA2	U13	GND	K7	RSCLK1	J2	V _{DDEXT}	H6		
DATA3	T11	GND	K8	RTCVDD	F10	V _{DDEXT}	J6		

Lead No.	Signal								
1	GND	41	GND	81	ТХ	121	ADDR19	161	AMS0
2	GND	42	GND	82	RX	122	ADDR18	162	ARDY
3	GND	43	GND	83	EMU	123	ADDR17	163	BR
4	VROUT1	44	GND	84	TRST	124	ADDR16	164	SA10
5	VROUT0	45	V _{DDEXT}	85	TMS	125	ADDR15	165	SWE
6	V _{DDEXT}	46	PF5	86	TDI	126	ADDR14	166	SCAS
7	GND	47	PF4	87	TDO	127	ADDR13	167	SRAS
8	GND	48	PF3	88	GND	128	GND	168	V _{DDINT}
9	GND	49	PF2	89	GND	129	GND	169	CLKOUT
10	CLKIN	50	PF1	90	GND	130	GND	170	GND
11	XTAL	51	PF0	91	GND	131	GND	171	V _{DDEXT}
12	V _{DDEXT}	52	V _{DDINT}	92	GND	132	GND	172	SMS
13	RESET	53	SCK	93	V _{DDEXT}	133	GND	173	SCKE
14	NMI	54	MISO	94	ТСК	134	V _{DDEXT}	174	GND
15	GND	55	MOSI	95	BMODE1	135	ADDR12	175	GND
16	RTXO	56	GND	96	BMODE0	136	ADDR11	176	GND
17	RTXI	57	V _{DDEXT}	97	GND	137	ADDR10		
18	V _{DDRTC}	58	DT1SEC	98	DATA15	138	ADDR9		
19	GND	59	DT1PRI	99	DATA14	139	ADDR8		
20	V _{DDEXT}	60	TFS1	100	DATA13	140	ADDR7		
21	PPI_CLK	61	TSCLK1	101	DATA12	141	ADDR6		
22	PPI0	62	DR1SEC	102	DATA11	142	ADDR5		
23	PPI1	63	DR1PRI	103	DATA10	143	V _{DDINT}		
24	PPI2	64	RFS1	104	DATA9	144	GND		
25	V _{DDINT}	65	RSCLK1	105	DATA8	145	V _{DDEXT}		
26	PPI3	66	V _{DDINT}	106	GND	146	ADDR4		
27	PF15	67	DT0SEC	107	V _{DDEXT}	147	ADDR3		
28	PF14	68	DTOPRI	108	DATA7	148	ADDR2		
29	PF13	69	TFS0	109	DATA6	149	ADDR1		
30	GND	70	GND	110	DATA5	150	ABE1		
31	V _{DDEXT}	71	V _{DDEXT}	111	V _{DDINT}	151	ABE0		
32	PF12	72	TSCLK0	112	DATA4	152	AWE		
33	PF11	73	DR0SEC	113	DATA3	153	ARE		
34	PF10	74	DROPRI	114	DATA2	154	AOE		
35	PF9	75	RFS0	115	DATA1	155	GND		
36	PF8	76	RSCLK0	116	DATA0	156	V _{DDEXT}		
37	PF7	77	TMR2	117	GND	157	V _{DDINT}		
38	PF6	78	TMR1	118	V _{DDEXT}	158	AMS3		
39	GND	79	TMR0	119	BG	159	AMS2		
40	GND	80	V _{DDINT}	120	BGH	160	AMS1		

Table 46. 176-Lead LQFP Pin Assignment (Numerical by Lead Number)



Figure 66. 169-Ball Plastic Ball Grid Array [PBGA] (B-169) Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 47 is provided as an aid to PCB design. For industry-
standard design recommendations, refer to IPC-7351,
Generic Requirements for Surface-Mount Design and Land Pat-
tern Standard.

Table 47. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
Chip Scale Package Ball Grid Array (CSP_BGA) BC-160-2	Solder Mask Defined	0.40 mm diameter	0.55 mm diameter
Plastic Ball Grid Array (PBGA) B-169	Solder Mask Defined	0.43 mm diameter	0.56 mm diameter

ORDERING GUIDE

	Temperature	Speed Grade		Package
Model	Range	(Max)	Package Description	Option
ADSP-BF531SBB400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF531SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF531SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF531SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF531SBBCZ4RL	–40°C to +85°C	400 MHz	160-Ball CSP_BGA, 13" Tape and Reel	BC-160-2
ADSP-BF531SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF532SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF532SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF532SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF532SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF533SBBZ400	–40°C to +85°C	400 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBC400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ400	–40°C to +85°C	400 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBSTZ400	–40°C to +85°C	400 MHz	176-Lead LQFP	ST-176-1
ADSP-BF533SBB500	–40°C to +85°C	500 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBZ500	–40°C to +85°C	500 MHz	169-Ball PBGA	B-169
ADSP-BF533SBBC500	–40°C to +85°C	500 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ500	–40°C to +85°C	500 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBC-5V	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SBBCZ-5V	–40°C to +85°C	533 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKBC-6V	0°C to +70°C	600 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKBCZ-6V	0°C to +70°C	600 MHz	160-Ball CSP_BGA	BC-160-2
ADSP-BF533SKSTZ-5V	0°C to +70°C	533 MHz	176-Lead LQFP	ST-176-1

 1 Z = RoHS compliant part.

² Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 20 for junction temperature (T_j) specification which is the only temperature specification.



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