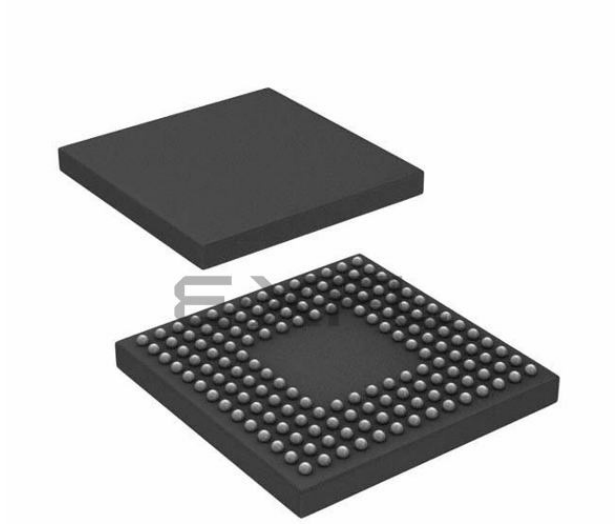

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	600MHz
Non-Volatile Memory	ROM (1kB)
On-Chip RAM	148kB
Voltage - I/O	1.8V, 3.3V
Voltage - Core	1.30V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LFBGA, CSPBGA
Supplier Device Package	160-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf533skbc-6v

PIN DESCRIPTIONS

The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors pin definitions are listed in Table 9.

All pins are three-stated during and immediately after reset, except the memory interface, asynchronous memory control, and synchronous memory control pins. These pins are all driven high, with the exception of CLKOUT, which toggles at the system clock rate. During hibernate, all outputs are three-stated unless otherwise noted in Table 9.

If $\overline{BR}$ is active (whether or not $\overline{RESET}$ is asserted), the memory pins are also three-stated. All unused I/O pins have their input buffers disabled with the exception of the pins that need pull-ups or pull-downs as noted in the table.

In order to maintain maximum functionality and reduce package size and pin count, some pins have dual, multiplexed functionality. In cases where pin functionality is reconfigurable, the default state is shown in plain text, while alternate functionality is shown in italics.

Table 9. Pin Descriptions

Pin Name	Type	Function	Driver Type[1]
Memory Interface			
ADDR19–1	O	Address Bus for Async/Sync Access	A
DATA15–0	I/O	Data Bus for Async/Sync Access	A
$\overline{ABE1–0}$/SDQM1–0	O	Byte Enables/Data Masks for Async/Sync Access	A
$\overline{BR}$	I	Bus Request (This pin should be pulled high if not used.)	
$\overline{BG}$	O	Bus Grant	A
$\overline{BGH}$	O	Bus Grant Hang	A
Asynchronous Memory Control			
$\overline{AMS3–0}$	O	Bank Select (Require pull-ups if hibernate is used.)	A
ARDY	I	Hardware Ready Control (This pin should be pulled high if not used.)	
$\overline{AOE}$	O	Output Enable	A
$\overline{ARE}$	O	Read Enable	A
$\overline{AWE}$	O	Write Enable	A
Synchronous Memory Control			
$\overline{SRAS}$	O	Row Address Strobe	A
$\overline{SCAS}$	O	Column Address Strobe	A
$\overline{SWE}$	O	Write Enable	A
SCKE	O	Clock Enable (Requires pull-down if hibernate is used.)	A
CLKOUT	O	Clock Output	B
SA10	O	A10 Pin	A
$\overline{SMS}$	O	Bank Select	A
Timers			
TMR0	I/O	Timer 0	C
TMR1/*PPI_FS1*	I/O	Timer 1/*PPI Frame Sync1*	C
TMR2/*PPI_FS2*	I/O	Timer 2/*PPI Frame Sync2*	C
PPI Port			
PPI3–0	I/O	PPI3–0	C
PPI_CLK/*TMRCLK*	I	PPI Clock/*External Timer Reference*	

SPECIFICATIONS

Component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 400 MHz and 500 MHz speed grade models[2]	0.8	1.2	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 533 MHz speed grade models[2]	0.8	1.25	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	600 MHz speed grade models[2]	0.8	1.30	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	Automotive 400 MHz speed grade models[2]	0.95	1.2	1.45	V
V_{DDINT}	Internal Supply Voltage[1]	Automotive 533 MHz speed grade models[2]	0.95	1.25	1.45	V
V_{DDEXT}	External Supply Voltage[3]	Nonautomotive grade models[2]	1.75	1.8/3.3	3.6	V
V_{DDEXT}	External Supply Voltage	Automotive grade models[2]	2.7	3.3	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage	Nonautomotive grade models[2]	1.75	1.8/3.3	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage	Automotive grade models[2]	2.7	3.3	3.6	V
V_{IH}	High Level Input Voltage[4, 5]	V_{DDEXT} = 1.85 V	1.3			V
V_{IH}	High Level Input Voltage[4, 5]	V_{DDEXT} = Maximum	2.0			V
$V_{IHCLKIN}$	High Level Input Voltage[6]	V_{DDEXT} = Maximum	2.2			V
V_{IL}	Low Level Input Voltage[7]	V_{DDEXT} = 1.75 V			+0.3	V
V_{IL}	Low Level Input Voltage[7]	V_{DDEXT} = 2.7 V			+0.6	V
T_J	Junction Temperature	160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = 0°C to +70°C	0		+95	°C
T_J	Junction Temperature	160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	160-Ball Chip Scale Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C
T_J	Junction Temperature	169-Ball Plastic Ball Grid Array (PBGA) @ $T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C
T_J	Junction Temperature	169-Ball Plastic Ball Grid Array (PBGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	176-Lead Quad Flatpack (LQFP) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+100	°C

[1] The regulator can generate V_{DDINT} at levels of 0.85 V to 1.2 V with –5% to +10% tolerance, 1.25 V with –4% to +10% tolerance, and 1.3 V with –0% to +10% tolerance.

[2] See Ordering Guide on Page 63.

[3] When V_{DDEXT} < 2.25 V, on-chip voltage regulation is not supported.

[4] Applies to all input and bidirectional pins except CLKIN.

[5] The ADSP-BF531/ADSP-BF532/ADSP-BF533 processors are 3.3 V tolerant (always accepts up to 3.6 V maximum V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}, because V_{OH} (maximum) approximately equals V_{DDEXT} (maximum). This 3.3 V tolerance applies to bidirectional pins (DATA15–0, TMR2–0, PF15–0, PPI3–0, RSCLK1–0, TSCLK1–0, RFS1–0, TFS1–0, MOSI, MISO, SCK) and input only pins ($\overline{BR}$, ARDY, PPI_CLK, DR0PRI, DR0SEC, DR1PRI, DR1SEC, RX, RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, NMI, and BMODE1–0).

[6] Applies to CLKIN pin only.

[7] Applies to all input and bidirectional pins.

Table 16. Activity Scaling Factors

I_{DDINT} Power Vector[1]	Activity Scaling Factor (ASF)[2]
$I_{DD-PEAK}$	1.27
$I_{DD-HIGH}$	1.25
I_{DD-TYP}	1.00
I_{DD-APP}	0.86
I_{DD-NOP}	0.72
$I_{DD-IDLE}$	0.41

[1] See EE-229 for power vector definitions.
[2] All ASF values determined using a 10:1 CCLK:SCLK ratio.

Table 17. Dynamic Current (mA, with ASF = 1.0)[1]

	Voltage (V_{DDINT})[2]														
Frequency (MHz)[2]	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V	1.45 V
50	12.7	13.9	15.3	16.8	18.1	19.4	21.0	22.3	24.0	25.4	26.4	27.2	28.7	30.3	30.7
100	22.6	24.2	26.2	28.1	30.1	31.8	34.7	36.2	38.4	40.5	43.0	43.4	45.7	47.9	48.9
200	40.8	44.1	46.9	50.3	53.3	56.9	59.9	63.1	66.7	70.2	73.8	75.0	78.7	82.4	84.6
250	50.1	53.8	57.2	61.4	64.7	68.9	72.9	76.8	81.0	85.1	89.3	90.8	95.2	99.6	102.0
300	N/A	63.5	67.4	72.4	76.2	81.0	85.9	90.6	95.2	100.0	104.8	106.6	111.8	116.9	119.4
375	N/A	N/A	N/A	88.6	93.5	99.0	104.6	110.3	116.0	122.1	128.0	130.0	136.2	142.4	145.5
400	N/A	N/A	N/A	93.9	99.3	105.0	110.8	116.8	123.0	129.4	135.7	137.9	144.6	151.2	154.3
425	N/A	N/A	N/A	N/A	N/A	111.0	117.3	123.5	129.9	136.8	143.2	145.6	152.6	159.7	162.8
475	N/A	N/A	N/A	N/A	N/A	N/A	130.3	136.8	143.8	151.4	158.1	161.1	168.9	176.6	179.7
500	N/A	N/A	N/A	N/A	N/A	N/A	N/A	143.5	150.7	158.7	165.6	168.8	177.0	185.2	188.2
533	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	160.4	168.8	176.5	179.6	188.2	196.8	200.5
600	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	196.2	199.6	209.3	219.0	222.6

[1] The values are not guaranteed as stand-alone maximum specifications, they must be combined with static current per the equations of Electrical Characteristics on Page 22.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 20.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 18 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Table 18. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.45 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.5 V to +3.8 V
Input Voltage[1, 2]	–0.5 V to +3.8 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	125°C

[1] Applies to 100% transient duty cycle. For other duty cycles see Table 19.
[2] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2 V.

Table 19. Maximum Duty Cycle for Input Transient Voltage[1]

V_{IN} Min (V)[2]	V_{IN} Max (V)[2]	Maximum Duty Cycle[3]
–0.50	+3.80	100%
–0.70	+4.00	40%
–0.80	+4.10	25%
–0.90	+4.20	15%
–1.00	+4.30	10%

[1] Applies to all signal pins with the exception of CLKIN, XTAL, VROUT1–0.
[2] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.
[3] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 10 and Table 20 provides details about the package branding for the Blackfin processors. For a complete listing of product availability, see the Ordering Guide on Page 63.

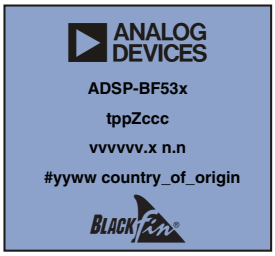


Figure 10. Product Information on Package

Table 20. Package Brand Information[1]

Brand Key	Field Description
ADSP-BF53x	Either ADSP-BF531, ADSP-BF532, or ADSP-BF533
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

[1] Non Automotive only. For branding information specific to Automotive products, contact Analog Devices Inc.

TIMING SPECIFICATIONS

Clock and Reset Timing

Table 21 and Figure 11 describe clock and reset operations. Per Absolute Maximum Ratings on Page 25, combinations of CLKIN and clock multipliers/divisors must not result in core/system clocks exceeding the maximum limits allowed for the processor, including system clock restrictions related to supply voltage.

Table 21. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN Period[1, 2, 3, 4]	25.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse	10.0		ns
t_{CKINH}	CLKIN High Pulse	10.0		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[5]	11 × t_{CKIN}		ns
t_{NOBOOT}	$\overline{\text{RESET}}$ Deassertion to First External Access Delay[6]	3 × t_{CKIN}	5 × t_{CKIN}	ns

[1] Applies to PLL bypass mode and PLL non bypass mode.
[2] CLKIN frequency must not change on the fly.
[3] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 11 on Page 21 through Table 13 on Page 21. Since the default behavior of the PLL is to multiply the CLKIN frequency by 10, the 400 MHz speed grade parts cannot use the full CLKIN period range.
[4] If the DF bit in the PLL_CTL register is set, then the maximum t_{CKIN} period is 50 ns.
[5] Applies after power-up sequence is complete. See Table 22 and Figure 12 for power-up reset timing.
[6] Applies when processor is configured in No Boot Mode (BMODE1-0 = b#00).

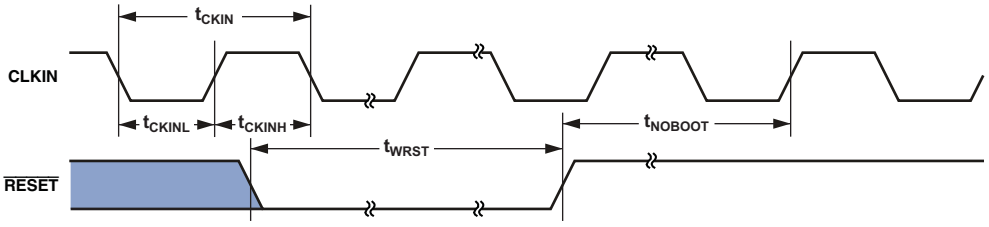
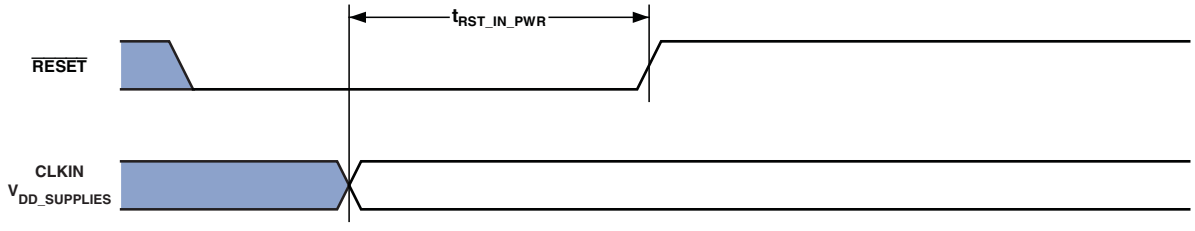


Figure 11. Clock and Reset Timing

Table 22. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted After the V_{DDINT}, V_{DDEXT}, V_{DDRTC}, and CLKIN Pins Are Stable and Within Specification	3500 × t_{CKIN}		ns



In Figure 12, $V_{DD\_SUPPLIES}$ is V_{DDINT}, V_{DDEXT}, V_{DDRTC}

Figure 12. Power-Up Reset Timing

SDRAM Interface Timing

Table 25. SDRAM Interface Timing[1]

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{SSDAT}	DATA Setup Before CLKOUT	2.1		1.5		ns
t_{HSDAT}	DATA Hold After CLKOUT	0.8		0.8		ns
Switching Characteristics						
t_{DCAD}	Command, ADDR, Data Delay After CLKOUT[2]		6.0		4.0	ns
t_{HCAD}	Command, ADDR, Data Hold After CLKOUT[2]	1.0		1.0		ns
t_{DSDAT}	Data Disable After CLKOUT		6.0		4.0	ns
t_{ENSDAT}	Data Enable After CLKOUT	1.0		1.0		ns
t_{SCLK}	CLKOUT Period[3]	10.0		7.5		ns
t_{SCLKH}	CLKOUT Width High	2.5		2.5		ns
t_{SCLKL}	CLKOUT Width Low	2.5		2.5		ns

[1] SDRAM timing for T_J > 105°C is limited to 100 MHz.
[2] Command pins include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS}$, SA10, SCKE.
[3] Refer to Table 13 on Page 21 for maximum f_{SCLK} at various V_{DDINT}.

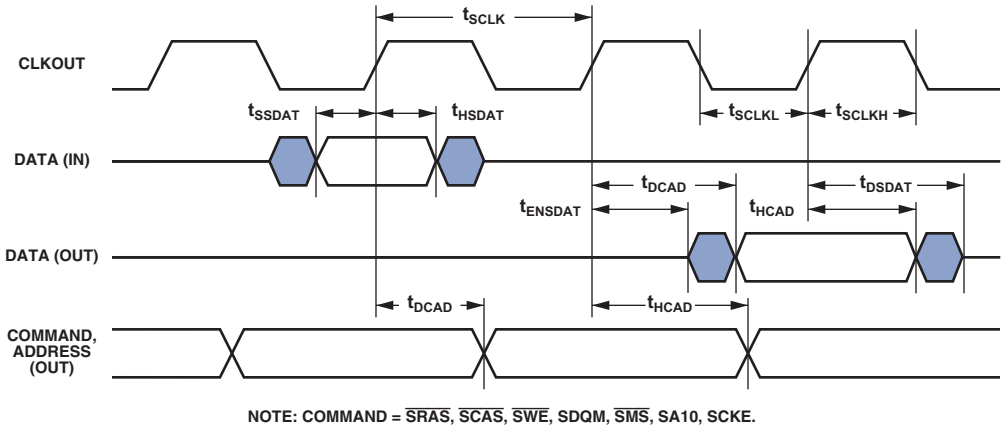


Figure 15. SDRAM Interface Timing

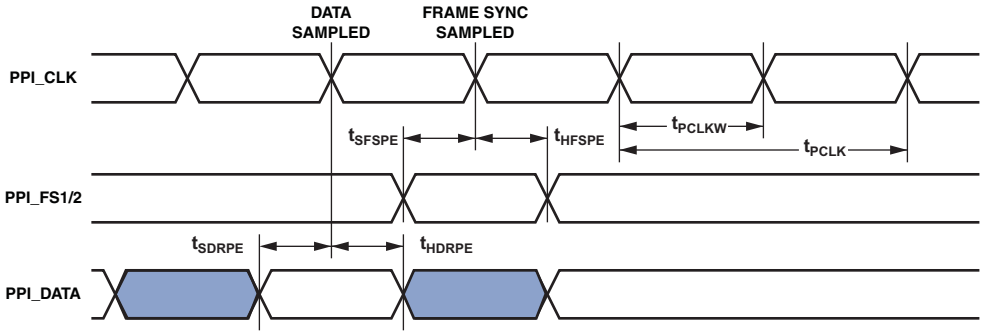


Figure 19. PPI GP Rx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 0)

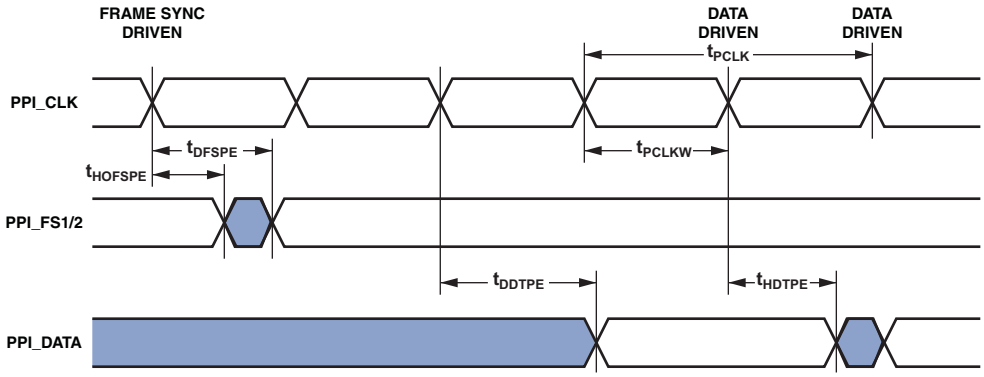


Figure 20. PPI GP Tx Mode with Internal Frame Sync Timing

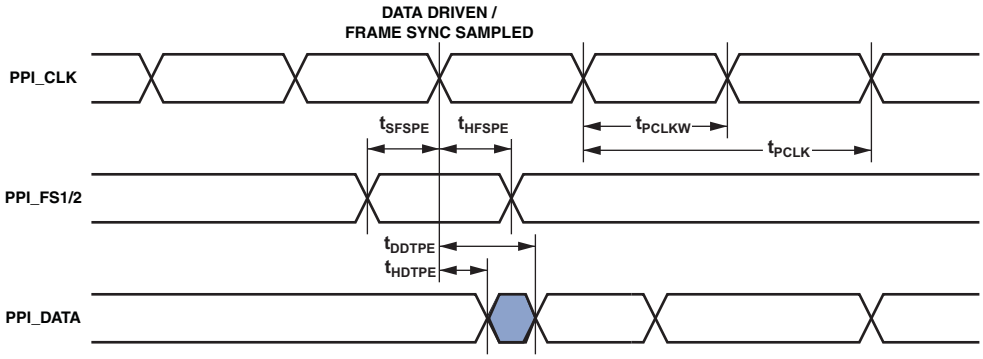


Figure 21. PPI GP Tx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 1)

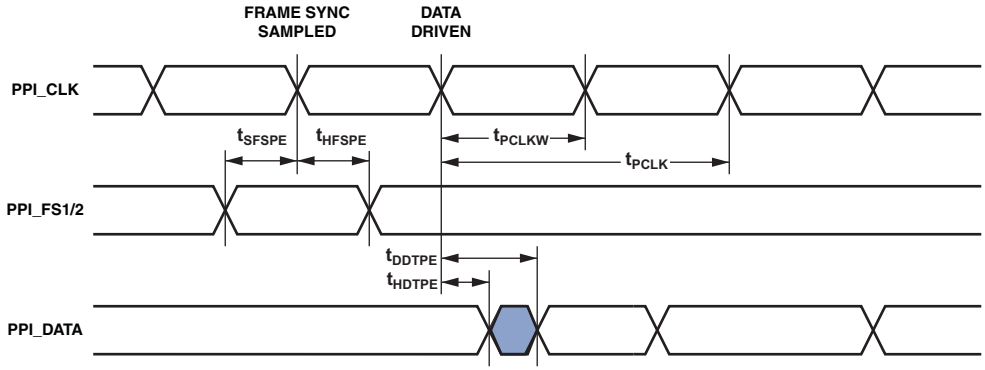


Figure 22. PPI GP Tx Mode with External Frame Sync Timing (PPI_CONTROL Bit 8 = 0)

Table 30. Serial Ports—Enable and Three-State

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Switching Characteristics						
t_{DTENE}	Data Enable Delay from External TSCLKx[1]	0		0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx[1, 2, 3]		10.0		10.0	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx[1]	−2.0		−2.0		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx[1, 2, 3]		3.0		3.0	ns

[1] Referenced to drive edge.
[2] Applicable to multichannel mode only.
[3] TSCLKx is tied to RSCLKx.

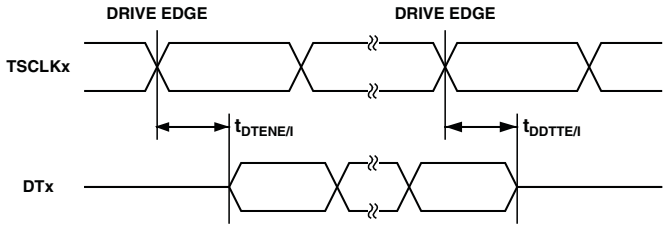


Figure 25. Enable and Three-State

Table 31. External Late Frame Sync

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Switching Characteristics								
$t_{DDTLFSE}$	Data Delay from Late External TFSx or External RFSx in multichannel mode with MCMEN = 0[1, 2]		10.5		10.0		10.0	ns
$t_{DTENLFS}$	Data Enable from Late FS or in multichannel mode with MCMEN = 0[1, 2]	0		0		0		ns

[1] In multichannel mode, TFSx enable and TFSx valid follow $t_{DTENLFS}$ and $t_{DDTLFSE}$.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$, then $t_{DDTTE/I}$ and $t_{DTENE/I}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

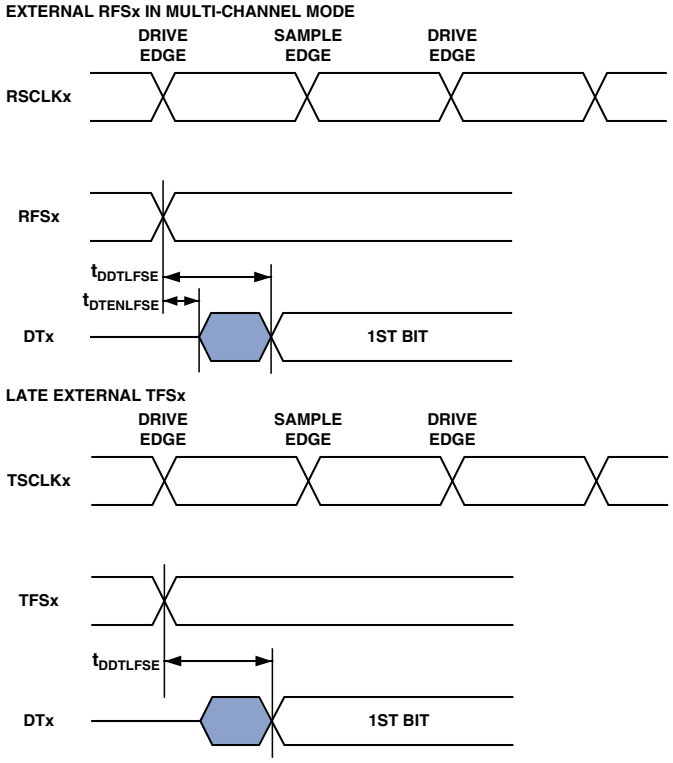


Figure 26. External Late Frame Sync

Serial Peripheral Interface (SPI) Port—Master Timing

Table 32. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V CSP_BGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Timing Requirements								
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	10.5		9		7.5		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	–1.5		–1.5		–1.5		ns
Switching Characteristics								
t_{SDSCIM}	$\overline{SPISELx}$ Low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISELx}$ High	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)		6		6		6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	–1.0		–1.0		–1.0		ns

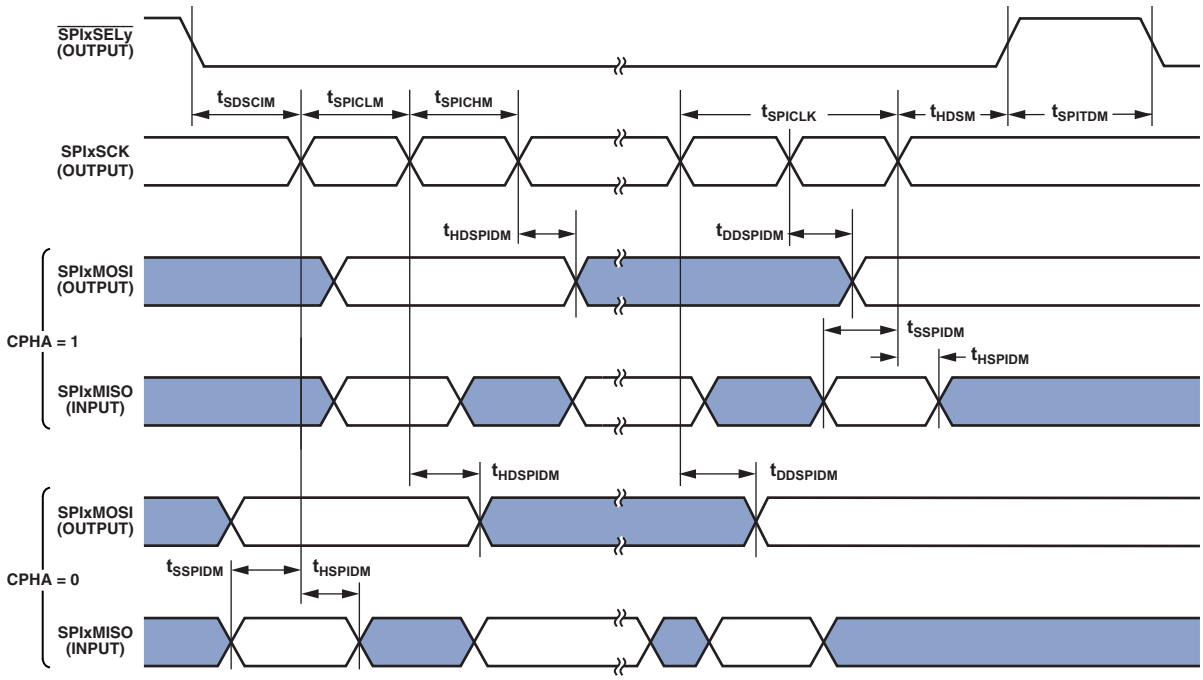


Figure 27. Serial Peripheral Interface (SPI) Port—Master Timing

JTAG Test and Emulation Port Timing

Table 37. JTAG Port Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5 V/3.3 V Min	V_{DDEXT} = 2.5 V/3.3 V Max	Unit
Timing Requirements						
t_{TCK}	TCK Period	20		20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		4		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	5		5		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width[2] (Measured in TCK Cycles)	4		4		TCK
Switching Characteristics						
t_{DTDO}	TDO Delay from TCK Low		10		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0	12	0	12	ns

[1] System Inputs = DATA15–0, ARDY, TMR2–0, PF15–0, PPI_CLK, RSCLK0–1, RFS0–1, DR0PRI, DR0SEC, TSCLK0–1, TFS0–1, DR1PRI, DR1SEC, MOSI, MISO, SCK, RX, $\overline{RESET}$, NMI, BMODE1–0, $\overline{BR}$, PPI3–0.

[2] 50 MHz maximum.

[3] System Outputs = DATA15–0, ADDR19–1, $\overline{ABE1–0}$, $\overline{AOE}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AMS3–0}$, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SCKE, CLKOUT, SA10, $\overline{SMS}$, TMR2–0, PF15–0, RSCLK0–1, RFS0–1, TSCLK0–1, TFS0–1, DT0PRI, DT0SEC, DT1PRI, DT1SEC, MOSI, MISO, SCK, TX, $\overline{BG}$, $\overline{BGH}$, PPI3–0.

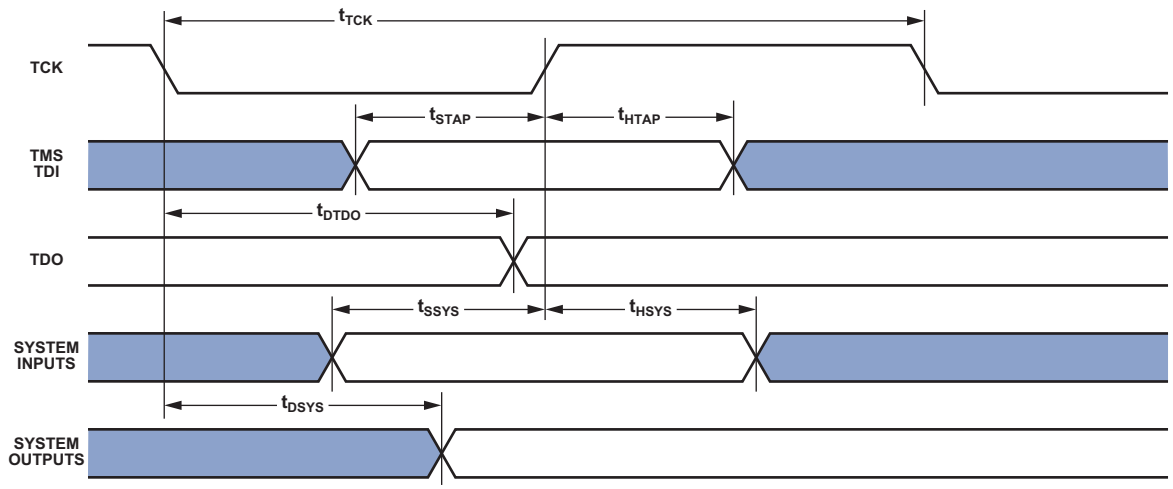


Figure 32. JTAG Port Timing

OUTPUT DRIVE CURRENTS

Figure 33 through Figure 44 show typical current-voltage characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

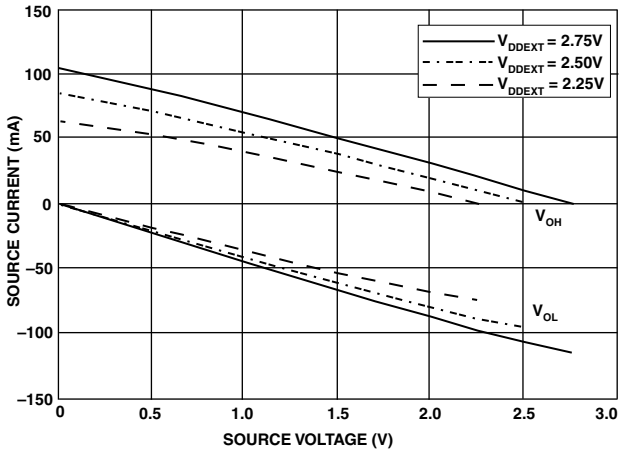


Figure 33. Drive Current A (V_{DDEXT} = 2.5 V)

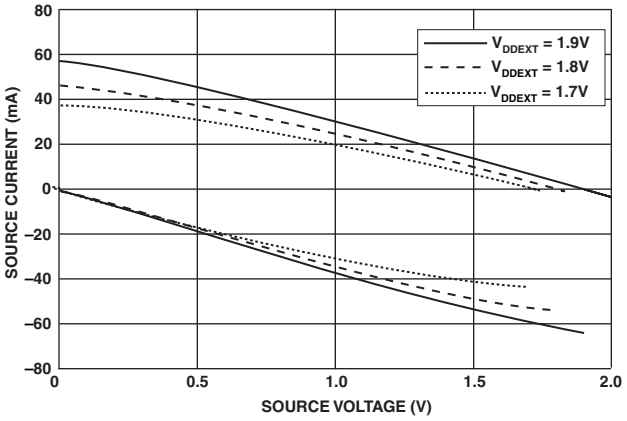


Figure 34. Drive Current A (V_{DDEXT} = 1.8 V)

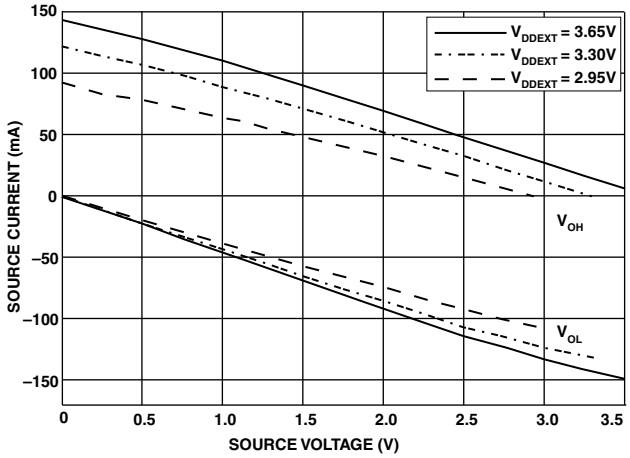


Figure 35. Drive Current A (V_{DDEXT} = 3.3 V)

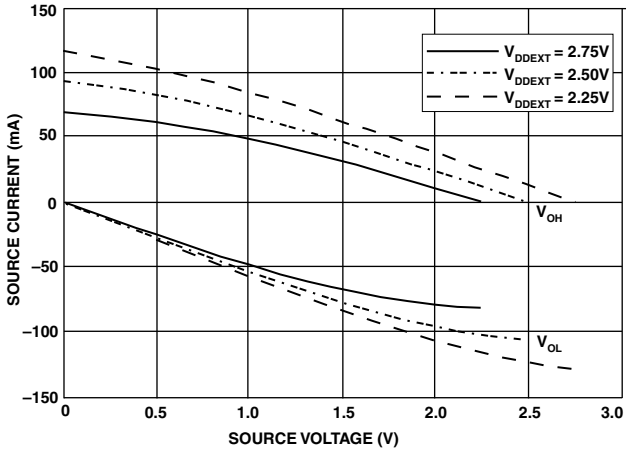


Figure 36. Drive Current B (V_{DDEXT} = 2.5 V)

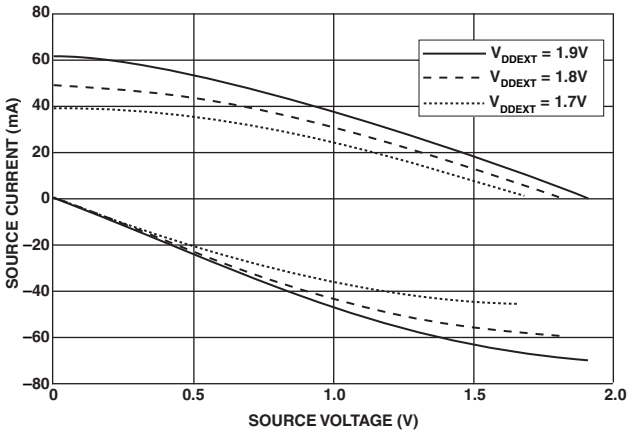


Figure 37. Drive Current B (V_{DDEXT} = 1.8 V)

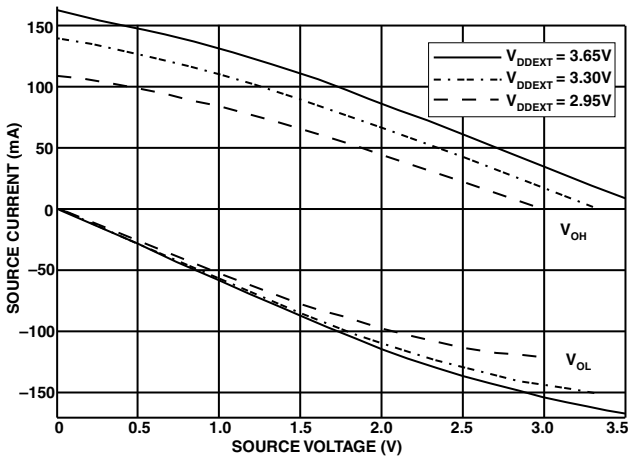


Figure 38. Drive Current B (V_{DDEXT} = 3.3 V)

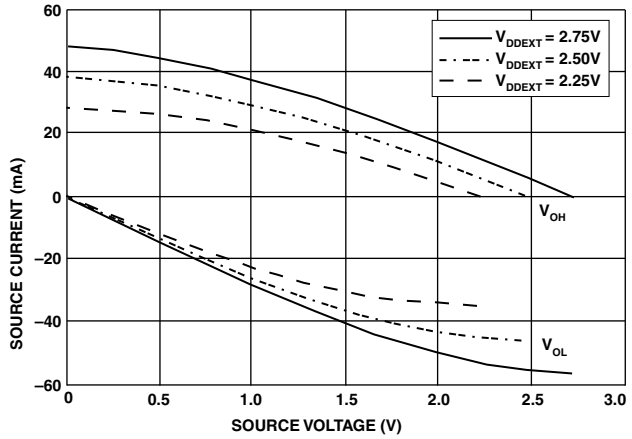


Figure 39. Drive Current C (V_{DDEXT} = 2.5 V)

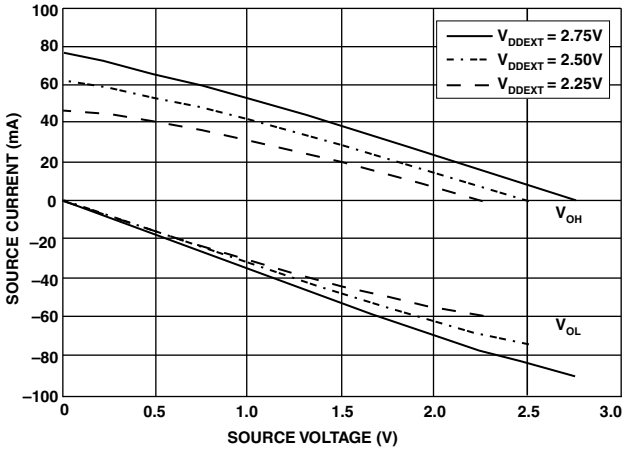


Figure 42. Drive Current D (V_{DDEXT} = 2.5 V)

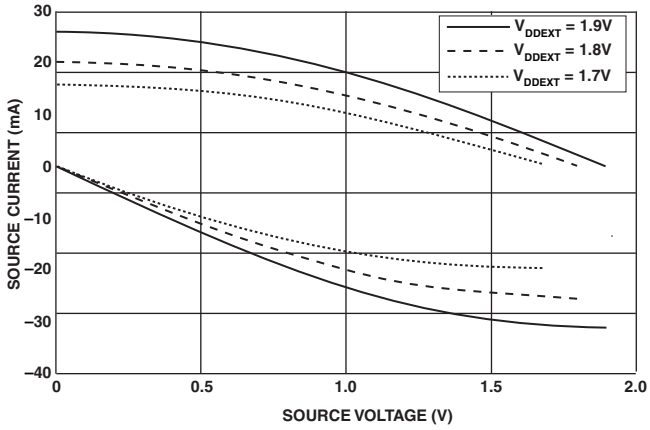


Figure 40. Drive Current C (V_{DDEXT} = 1.8 V)

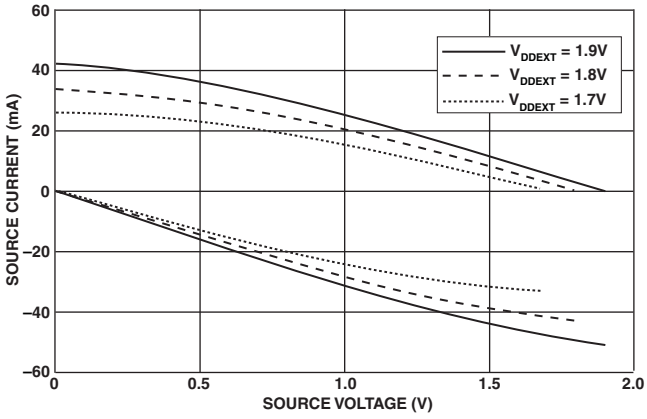


Figure 43. Drive Current D (V_{DDEXT} = 1.8 V)

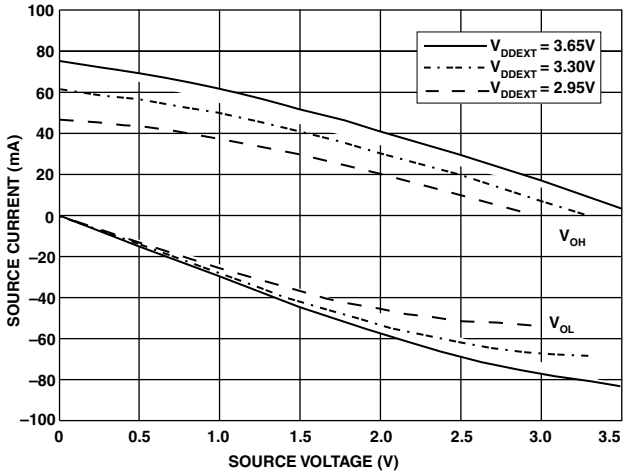


Figure 41. Drive Current C (V_{DDEXT} = 3.3 V)

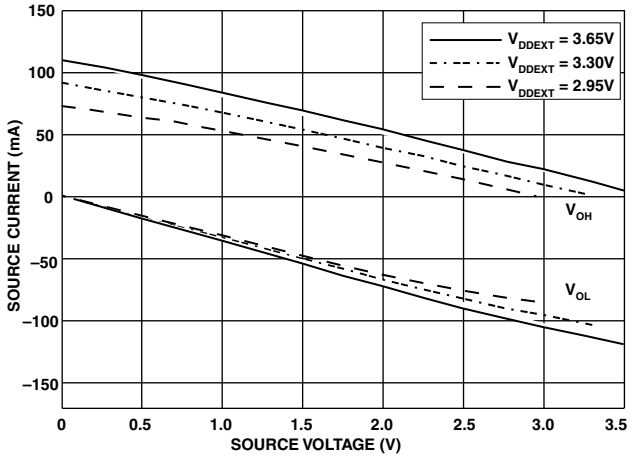


Figure 44. Drive Current D (V_{DDEXT} = 3.3 V)

Figure 60 shows the top view of the CSP_BGA ball configuration. Figure 61 shows the bottom view of the CSP_BGA ball configuration.

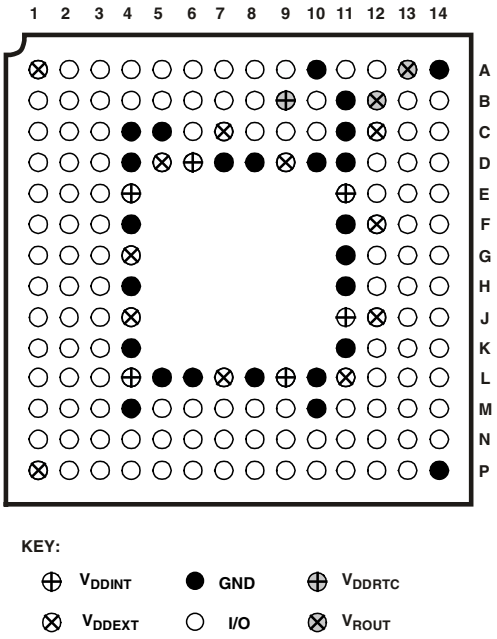


Figure 60. 160-Ball CSP_BGA Ground Configuration (Top View)

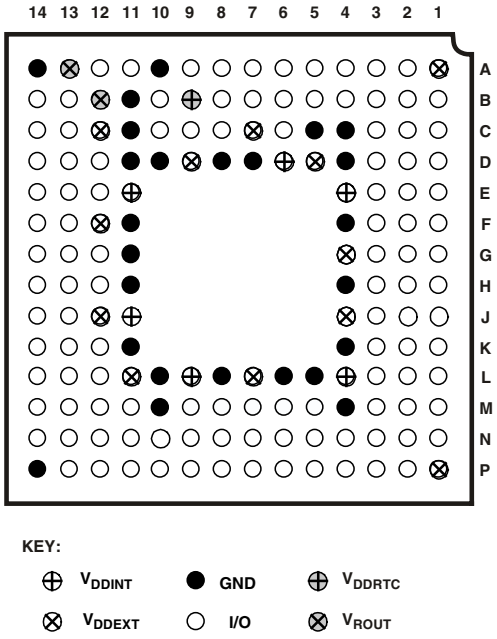


Figure 61. 160-Ball CSP_BGA Ground Configuration (Bottom View)

169-BALL PBGA BALL ASSIGNMENT

Table 43 lists the PBGA ball assignment by signal. Table 44 on Page 54 lists the PBGA ball assignment by ball number.

Table 43. 169-Ball PBGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{ABE0}$	H16	DATA4	U12	GND	K9	RTXI	A10	V_{DDEXT}	K6
$\overline{ABE1}$	H17	DATA5	U11	GND	K10	RTXO	A11	V_{DDEXT}	L6
ADDR1	J16	DATA6	T10	GND	K11	RX	T1	V_{DDEXT}	M6
ADDR2	J17	DATA7	U10	GND	L7	SA10	B15	V_{DDEXT}	M7
ADDR3	K16	DATA8	T9	GND	L8	$\overline{SCAS}$	A16	V_{DDEXT}	M8
ADDR4	K17	DATA9	U9	GND	L9	SCK	D1	V_{DDEXT}	T2
ADDR5	L16	DATA10	T8	GND	L10	SCKE	B14	VROUT0	B12
ADDR6	L17	DATA11	U8	GND	L11	$\overline{SMS}$	A17	VROUT1	B13
ADDR7	M16	DATA12	U7	GND	M9	$\overline{SRAS}$	A15	XTAL	A13
ADDR8	M17	DATA13	T7	GND	T16	$\overline{SWE}$	B17		
ADDR9	N17	DATA14	U6	MISO	E2	TCK	U4		
ADDR10	N16	DATA15	T6	MOSI	E1	TDI	U3		
ADDR11	P17	DR0PRI	M2	NMI	B11	TDO	T4		
ADDR12	P16	DR0SEC	M1	PF0	D2	TFS0	L1		
ADDR13	R17	DR1PRI	H1	PF1	C1	TFS1	G2		
ADDR14	R16	DR1SEC	H2	PF2	B1	TMR0	R1		
ADDR15	T17	DT0PRI	K2	PF3	C2	TMR1	P2		
ADDR16	U15	DT0SEC	K1	PF4	A1	TMR2	P1		
ADDR17	T15	DT1PRI	F1	PF5	A2	TMS	T3		
ADDR18	U16	DT1SEC	F2	PF6	B3	$\overline{TRST}$	U2		
ADDR19	T14	$\overline{EMU}$	U1	PF7	A3	TSCLK0	L2		
$\overline{AMS0}$	D17	GND	B16	PF8	B4	TSCLK1	G1		
$\overline{AMS1}$	E16	GND	F11	PF9	A4	TX	R2		
$\overline{AMS2}$	E17	GND	G7	PF10	B5	VDD	F12		
$\overline{AMS3}$	F16	GND	G8	PF11	A5	VDD	G12		
$\overline{AOE}$	F17	GND	G9	PF12	A6	VDD	H12		
ARDY	C16	GND	G10	PF13	B6	VDD	J12		
$\overline{ARE}$	G16	GND	G11	PF14	A7	VDD	K12		
$\overline{AWE}$	G17	GND	H7	PF15	B7	VDD	L12		
$\overline{BG}$	T13	GND	H8	PPI_CLK	B10	VDD	M10		
$\overline{BGH}$	U17	GND	H9	PPI0	B9	VDD	M11		
BMODE0	U5	GND	H10	PPI1	A9	VDD	M12		
BMODE1	T5	GND	H11	PPI2	B8	V_{DDEXT}	B2		
$\overline{BR}$	C17	GND	J7	PPI3	A8	V_{DDEXT}	F6		
CLKIN	A14	GND	J8	$\overline{RESET}$	A12	V_{DDEXT}	F7		
CLKOUT	D16	GND	J9	RFS0	N1	V_{DDEXT}	F8		
DATA0	U14	GND	J10	RFS1	J1	V_{DDEXT}	F9		
DATA1	T12	GND	J11	RSCLK0	N2	V_{DDEXT}	G6		
DATA2	U13	GND	K7	RSCLK1	J2	V_{DDEXT}	H6		
DATA3	T11	GND	K8	RTCVDD	F10	V_{DDEXT}	J6		

Table 44. 169-Ball PBGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	PF4	D16	CLKOUT	J2	RSCLK1	M12	VDD	U9	DATA9
A2	PF5	D17	$\overline{\text{AMS0}}$	J6	V_{DDEXT}	M16	ADDR7	U10	DATA7
A3	PF7	E1	MOSI	J7	GND	M17	ADDR8	U11	DATA5
A4	PF9	E2	MISO	J8	GND	N1	RFS0	U12	DATA4
A5	PF11	E16	$\overline{\text{AMS1}}$	J9	GND	N2	RSCLK0	U13	DATA2
A6	PF12	E17	$\overline{\text{AMS2}}$	J10	GND	N16	ADDR10	U14	DATA0
A7	PF14	F1	DT1PRI	J11	GND	N17	ADDR9	U15	ADDR16
A8	PPI3	F2	DT1SEC	J12	VDD	P1	TMR2	U16	ADDR18
A9	PPI1	F6	V_{DDEXT}	J16	ADDR1	P2	TMR1	U17	$\overline{\text{BGH}}$
A10	RTXI	F7	V_{DDEXT}	J17	ADDR2	P16	ADDR12		
A11	RTXO	F8	V_{DDEXT}	K1	DT0SEC	P17	ADDR11		
A12	$\overline{\text{RESET}}$	F9	V_{DDEXT}	K2	DT0PRI	R1	TMR0		
A13	XTAL	F10	RTCVDD	K6	V_{DDEXT}	R2	TX		
A14	CLKIN	F11	GND	K7	GND	R16	ADDR14		
A15	$\overline{\text{SRAS}}$	F12	VDD	K8	GND	R17	ADDR13		
A16	$\overline{\text{SCAS}}$	F16	$\overline{\text{AMS3}}$	K9	GND	T1	RX		
A17	$\overline{\text{SMS}}$	F17	$\overline{\text{AOE}}$	K10	GND	T2	V_{DDEXT}		
B1	PF2	G1	TSCLK1	K11	GND	T3	TMS		
B2	V_{DDEXT}	G2	TFS1	K12	VDD	T4	TDO		
B3	PF6	G6	V_{DDEXT}	K16	ADDR3	T5	BMODE1		
B4	PF8	G7	GND	K17	ADDR4	T6	DATA15		
B5	PF10	G8	GND	L1	TFS0	T7	DATA13		
B6	PF13	G9	GND	L2	TSCLK0	T8	DATA10		
B7	PF15	G10	GND	L6	V_{DDEXT}	T9	DATA8		
B8	PPI2	G11	GND	L7	GND	T10	DATA6		
B9	PPI0	G12	VDD	L8	GND	T11	DATA3		
B10	PPI_CLK	G16	$\overline{\text{ARE}}$	L9	GND	T12	DATA1		
B11	NMI	G17	$\overline{\text{AWE}}$	L10	GND	T13	$\overline{\text{BG}}$		
B12	VROUT0	H1	DR1PRI	L11	GND	T14	ADDR19		
B13	VROUT1	H2	DR1SEC	L12	VDD	T15	ADDR17		
B14	SCKE	H6	V_{DDEXT}	L16	ADDR5	T16	GND		
B15	SA10	H7	GND	L17	ADDR6	T17	ADDR15		
B16	GND	H8	GND	M1	DR0SEC	U1	$\overline{\text{EMU}}$		
B17	$\overline{\text{SWE}}$	H9	GND	M2	DR0PRI	U2	$\overline{\text{TRST}}$		
C1	PF1	H10	GND	M6	V_{DDEXT}	U3	TDI		
C2	PF3	H11	GND	M7	V_{DDEXT}	U4	TCK		
C16	ARDY	H12	VDD	M8	V_{DDEXT}	U5	BMODE0		
C17	$\overline{\text{BR}}$	H16	$\overline{\text{ABE0}}$	M9	GND	U6	DATA14		
D1	SCK	H17	$\overline{\text{ABE1}}$	M10	VDD	U7	DATA12		
D2	PF0	J1	RFS1	M11	VDD	U8	DATA11		

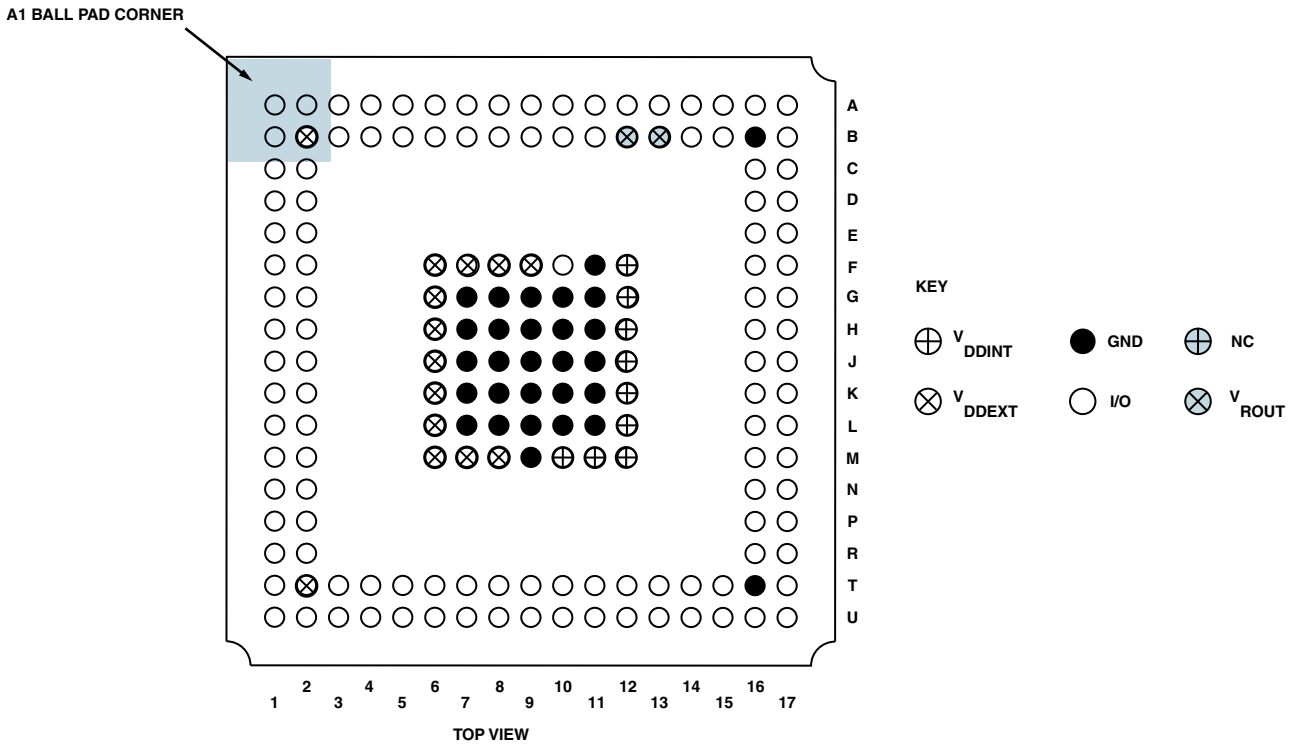


Figure 62. 169-Ball PBGA Ground Configuration (Top View)

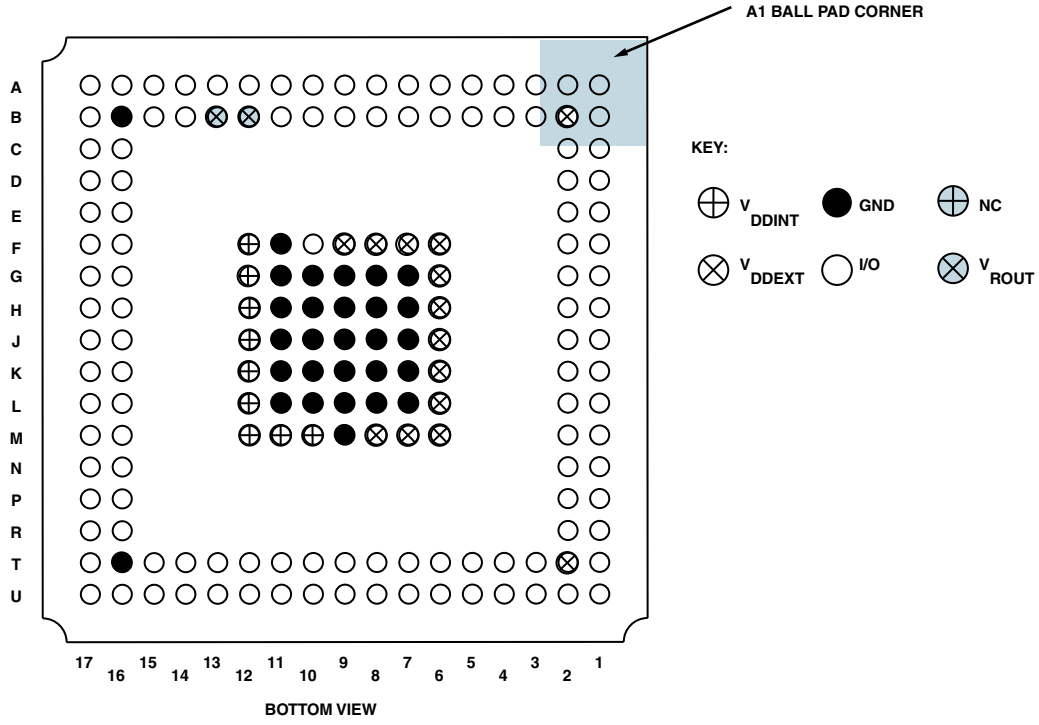


Figure 63. 169-Ball PBGA Ground Configuration (Bottom View)

Table 46. 176-Lead LQFP Pin Assignment (Numerical by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	GND	41	GND	81	TX	121	ADDR19	161	$\overline{AMS0}$
2	GND	42	GND	82	RX	122	ADDR18	162	ARDY
3	GND	43	GND	83	$\overline{EMU}$	123	ADDR17	163	$\overline{BR}$
4	VROUT1	44	GND	84	$\overline{TRST}$	124	ADDR16	164	SA10
5	VROUT0	45	V_{DDEXT}	85	TMS	125	ADDR15	165	$\overline{SWE}$
6	V_{DDEXT}	46	PF5	86	TDI	126	ADDR14	166	$\overline{SCAS}$
7	GND	47	PF4	87	TDO	127	ADDR13	167	$\overline{SRAS}$
8	GND	48	PF3	88	GND	128	GND	168	V_{DDINT}
9	GND	49	PF2	89	GND	129	GND	169	CLKOUT
10	CLKIN	50	PF1	90	GND	130	GND	170	GND
11	XTAL	51	PF0	91	GND	131	GND	171	V_{DDEXT}
12	V_{DDEXT}	52	V_{DDINT}	92	GND	132	GND	172	$\overline{SMS}$
13	$\overline{RESET}$	53	SCK	93	V_{DDEXT}	133	GND	173	SCKE
14	NMI	54	MISO	94	TCK	134	V_{DDEXT}	174	GND
15	GND	55	MOSI	95	BMODE1	135	ADDR12	175	GND
16	RTXO	56	GND	96	BMODE0	136	ADDR11	176	GND
17	RTXI	57	V_{DDEXT}	97	GND	137	ADDR10		
18	V_{DDRTC}	58	DT1SEC	98	DATA15	138	ADDR9		
19	GND	59	DT1PRI	99	DATA14	139	ADDR8		
20	V_{DDEXT}	60	TFS1	100	DATA13	140	ADDR7		
21	PPI_CLK	61	TSCLK1	101	DATA12	141	ADDR6		
22	PPI0	62	DR1SEC	102	DATA11	142	ADDR5		
23	PPI1	63	DR1PRI	103	DATA10	143	V_{DDINT}		
24	PPI2	64	RFS1	104	DATA9	144	GND		
25	V_{DDINT}	65	RSCLK1	105	DATA8	145	V_{DDEXT}		
26	PPI3	66	V_{DDINT}	106	GND	146	ADDR4		
27	PF15	67	DT0SEC	107	V_{DDEXT}	147	ADDR3		
28	PF14	68	DT0PRI	108	DATA7	148	ADDR2		
29	PF13	69	TFS0	109	DATA6	149	ADDR1		
30	GND	70	GND	110	DATA5	150	$\overline{ABE1}$		
31	V_{DDEXT}	71	V_{DDEXT}	111	V_{DDINT}	151	$\overline{ABE0}$		
32	PF12	72	TSCLK0	112	DATA4	152	$\overline{AWE}$		
33	PF11	73	DR0SEC	113	DATA3	153	$\overline{ARE}$		
34	PF10	74	DR0PRI	114	DATA2	154	$\overline{AOE}$		
35	PF9	75	RFS0	115	DATA1	155	GND		
36	PF8	76	RSCLK0	116	DATA0	156	V_{DDEXT}		
37	PF7	77	TMR2	117	GND	157	V_{DDINT}		
38	PF6	78	TMR1	118	V_{DDEXT}	158	$\overline{AMS3}$		
39	GND	79	TMR0	119	$\overline{BG}$	159	$\overline{AMS2}$		
40	GND	80	V_{DDINT}	120	$\overline{BGH}$	160	$\overline{AMS1}$		

OUTLINE DIMENSIONS

Dimensions in the outline dimension figures are shown in millimeters.

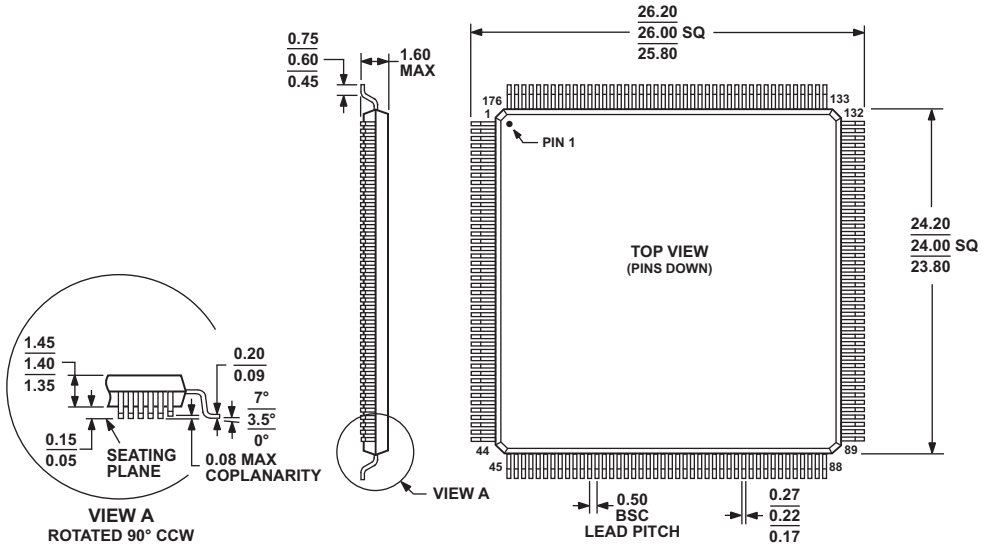


Figure 64. 176-Lead Low Profile Quad Flat Package [LQFP]
(ST-176-1)
Dimensions shown in millimeters