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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2125
Number of Logic Elements/Cells	17000
Total RAM Bits	282624
Number of I/O	201
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-17e-5ft256i

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Figure 2-2. PFU Diagram



Slice

Slice 0 through Slice 2 contain two 4-input combinatorial Look-Up Tables (LUT4), which feed two registers. Slice 3 contains two LUT4s and no registers. For PFUs, Slice 0 and Slice 2 can also be configured as distributed memory, a capability not available in PFF blocks. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured as positive/negative edge triggered or level sensitive clocks.

Table 2-1.	Resources	and Modes	Available	per Slice
			/ IT amaint	

	PFU E	BLock	PFF Block			
Slice	Resources	Modes	Resources	Modes		
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM		
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM		
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM		
Slice 3	2 LUT4s	Logic, ROM	2 LUT4s	Logic, ROM		

Slice 0 through Slice 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 13 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.



Routing

There are many resources provided in the LatticeXP2 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) or x6 (spans seven PFU) connections. The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered to allow both short and long connections routing between PFUs.

The LatticeXP2 family has an enhanced routing architecture to produce a compact design. The Diamond design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Phase Locked Loops (PLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The LatticeXP2 family supports between two and four full featured General Purpose PLLs (GPLL). The architecture of the GPLL is shown in Figure 2-4.

CLKI, the PLL reference frequency, is provided either from the pin or from routing; it feeds into the Input Clock Divider block. CLKFB, the feedback signal, is generated from CLKOP (the primary clock output) or from a user clock pin/logic. CLKFB feeds into the Feedback Divider and is used to multiply the reference frequency.

Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. The phase and frequency of the VCO are determined from the input path and feedback signals. A LOCK signal is generated by the VCO to indicate that the VCO is locked with the input clock signal.

The output of the VCO feeds into the CLKOP Divider, a post-scalar divider. The duty cycle of the CLKOP Divider output can be fine tuned using the Duty Trim block, which creates the CLKOP signal. By allowing the VCO to operate at higher frequencies than CLKOP, the frequency range of the GPLL is expanded. The output of the CLKOP Divider is passed through the CLKOK Divider, a secondary clock divider, to generate lower frequencies for the CLKOK output. For applications that require even lower frequencies, the CLKOP signal is passed through a divide-by-three divider to produce the CLKOK2 output. The CLKOK2 output is provided for applications that use source synchronous logic. The Phase/Duty Cycle/Duty Trim block is used to adjust the phase and duty cycle of the CLKOP Divider output to generate the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The clock outputs from the GPLL; CLKOP, CLKOK, CLKOK2 and CLKOS, are fed to the clock distribution network.

For further information on the GPLL please see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide.



Figure 2-4. General Purpose PLL (GPLL) Diagram



Table 2-4 provides a description of the signals in the GPLL blocks.

Signal	I/O	Description	
CLKI	I	Clock input from external pin or routing	
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)	
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers	
RSTK	I	"1" to reset K-divider	
DPHASE [3:0]	I	DPA Phase Adjust input	
DDDUTY [3:0]	I	DPA Duty Cycle Select input	
WRDEL	I	DPA Fine Delay Adjust input	
CLKOS	0	PLL output clock to clock tree (phase shifted/duty cycle changed)	
CLKOP	0	PLL output clock to clock tree (no phase shift)	
CLKOK	0	PLL output to clock tree through secondary clock divider	
CLKOK2	0	PLL output to clock tree (CLKOP divided by 3)	
LOCK	0	"1" indicates PLL LOCK to CLKI	

Clock Dividers

LatticeXP2 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from the CLKOP output from the GPLLs or from the Edge Clocks (ECLK). The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets the input and forces all outputs to low. The RELEASE signal releases outputs to the input clock. For further information on clock dividers, please see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide. Figure 2-5 shows the clock divider connections.



Figure 2-5. Clock Divider Connections



Clock Distribution Network

LatticeXP2 devices have eight quadrant-based primary clocks and between six and eight flexible region-based secondary clocks/control signals. Two high performance edge clocks are available on each edge of the device to support high speed interfaces. The clock inputs are selected from external I/Os, the sysCLOCK PLLs, or routing. Clock inputs are fed throughout the chip via the primary, secondary and edge clock networks.

Primary Clock Sources

LatticeXP2 devices derive primary clocks from four sources: PLL outputs, CLKDIV outputs, dedicated clock inputs and routing. LatticeXP2 devices have two to four sysCLOCK PLLs, located in the four corners of the device. There are eight dedicated clock inputs, two on each side of the device. Figure 2-6 shows the primary clock sources.







sysDSP Block Capabilities

The sysDSP block in the LatticeXP2 family supports four functional elements in three 9, 18 and 36 data path widths. The user selects a function element for a DSP block and then selects the width and type (signed/unsigned) of its operands. The operands in the LatticeXP2 family sysDSP Blocks can be either signed or unsigned but not mixed within a function element. Similarly, the operand widths cannot be mixed within a block. DSP elements can be concatenated.

The resources in each sysDSP block can be configured to support the following four elements:

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Accumulate)

The number of elements available in each block depends on the width selected from the three available options: x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP functions. Table 2-6 shows the capabilities of the block.

Width of Multiply	x9	x18	x36
MULT	8	4	1
MAC	2	2	_
MULTADDSUB	4	2	_
MULTADDSUBSUM	2	1	_

Some options are available in four elements. The input register in all the elements can be directly loaded or can be loaded as shift register from previous operand registers. By selecting 'dynamic operation' the following operations are possible:



MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/ subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-23 shows the MULTADDSUBSUM sysDSP element.

Figure 2-23. MULTADDSUBSUM



Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable (CE) and Reset (RST) signals from routing are available to every DSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output



Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysIO buffers as shown in Figure 2-25. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysIO buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

Figure 2-25. PIC Diagram



Signals are available on left/right/bottom edges only.
Selected blocks.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C") as shown in Figure 2-25. The PAD Labels "T" and "C" distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as inputs.



shows the diagram using this gearbox function. For more information on this topic, see TN1138, <u>LatticeXP2 High</u> <u>Speed I/O Interface</u>.







original backup configuration and try again. This all can be done without power cycling the system. For more information please see TN1220, <u>LatticeXP2 Dual Boot Feature</u>.

For more information on device configuration, please see TN1141, LatticeXP2 sysCONFIG Usage Guide.

Soft Error Detect (SED) Support

LatticeXP2 devices have dedicated logic to perform Cyclic Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, LatticeXP2 devices can be programmed for checking soft errors in SRAM. SED can be run on a programmed device when the user logic is not active. In the event a soft error occurs, the device can be programmed to either reload from a known good boot image (from internal Flash or external SPI memory) or generate an error signal.

For further information on SED support, please see TN1130, LatticeXP2 Soft Error Detection (SED) Usage Guide.

On-Chip Oscillator

Every LatticeXP2 device has an internal CMOS oscillator that is used to derive a Master Clock (CCLK) for configuration. The oscillator and CCLK run continuously and are available to user logic after configuration is complete. The available CCLK frequencies are listed in Table 2-14. When a different CCLK frequency is selected during the design process, the following sequence takes place:

- 1. Device powers up with the default CCLK frequency.
- 2. During configuration, users select a different CCLK frequency.
- 3. CCLK frequency changes to the selected frequency after clock configuration bits are received.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1141, <u>LatticeXP2 sysCON-FIG Usage Guide</u>.

Table 2-14. Selectable	CCLKs and Oscillato	r Freauencies Durina	Configuration and	User Mode

CCLK/Oscillator (MHz)				
2.5 ¹				
3.1 ²				
4.3				
5.4				
6.9				
8.1				
9.2				
10				
13				
15				
20				
26				
32				
40				
54				
80 ³				
163 ³				
1 Software default oscillator frequency				

1. Software default oscillator frequency.

2. Software default CCLK frequency.

3. Frequency not valid for CCLK.



Density Shifting

The LatticeXP2 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.



Supply Current (Standby)^{1, 2, 3, 4}

Symbol	Parameter	Device	Typical⁵	Units
		XP2-5	14	mA
		XP2-8	18	mA
I _{CC}	Core Power Supply Current	XP2-17	24	mA
		XP2-30	35	mA
		XP2-40	45	mA
		XP2-5	15	mA
		XP2-8	15	mA
I _{CCAUX}	Auxiliary Power Supply Current ⁶	XP2-17	15	mA
		XP2-30	16	mA
		XP2-40	16	mA
I _{CCPLL}	PLL Power Supply Current (per PLL)		0.1	mA
I _{CCIO}	Bank Power Supply Current (per bank)		2	mA
I _{CCJ}	V _{CCJ} Power Supply Current		0.25	mA

Over Recommended Operating Conditions

1. For further information on supply current, please see TN1139, Power Estimation and Management for LatticeXP2 Devices.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

3. Frequency 0 MHz.

4. Pattern represents a "blank" configuration data file.

5. $T_J = 25^{\circ}C$, power supplies at nominal voltage.

6. In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.



RSDS

The LatticeXP2 devices support differential RSDS standard. This standard is emulated using complementary LVC-MOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.



Figure 3-4. RSDS (Reduced Swing Differential Standard)

Table 3-4. RSDS DC Conditions¹

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/-1%)	294	Ω
R _P	Driver Parallel Resistor (+/-1%)	121	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage (After R _P)	1.35	V
V _{OL}	Output Low Voltage (After R _P)	1.15	V
V _{OD}	Output Differential Voltage (After R _P)	0.20	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	101.5	Ω
I _{DC}	DC Output Current	3.66	mA

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.



LatticeXP2 Internal Switching Characteristics¹ (Continued)

		-7		-	-6		-5	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{RST_PIO}	Asynchronous reset time for PFU Logic	—	0.386	—	0.419	—	0.452	ns
t _{DEL}	Dynamic Delay Step Size	0.035	0.035	0.035	0.035	0.035	0.035	ns
EBR Timing	· · · · · ·							
t _{CO_EBR}	Clock (Read) to Output from Address or Data	_	2.774	_	3.142	_	3.510	ns
t _{COO_EBR}	Clock (Write) to Output from EBR Output Register	_	0.360	_	0.408	—	0.456	ns
^t SUDATA_EBR	Setup Data to EBR Memory (Write Clk)	-0.167	—	-0.198	_	-0.229	—	ns
t _{HDATA_EBR}	Hold Data to EBR Memory (Write Clk)	0.194	—	0.231	_	0.267	_	ns
t _{SUADDR_EBR}	Setup Address to EBR Memory (Write Clk)	-0.117	—	-0.137	_	-0.157	—	ns
t _{HADDR_EBR}	Hold Address to EBR Memory (Write Clk)	0.157	_	0.182	_	0.207	_	ns
t _{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory (Write/Read Clk)	-0.135	_	-0.159	_	-0.182	_	ns
t _{HWREN_EBR}	Hold Write/Read Enable to EBR Memory (Write/Read Clk)	0.158	—	0.186	_	0.214	_	ns
t _{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register (Read Clk)	0.144	—	0.160	_	0.176	_	ns
t _{HCE_EBR}	Clock Enable Hold Time to EBR Output Register (Read Clk)	-0.097	—	-0.113	_	-0.129	_	ns
t _{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register (Asynchro- nous)	_	1.156	_	1.341	_	1.526	ns
t _{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.117	—	-0.137	_	-0.157	_	ns
t _{HBE_EBR}	Byte Enable Hold Time to EBR Output Register Dynamic Delay on Each PIO	0.157	_	0.182	_	0.207	_	ns
t _{RSTREC_EBR}	Asynchronous reset recovery time for EBR	0.233	—	0.291		0.347	—	ns
t _{RST_EBR}	Asynchronous reset time for EBR	—	1.156	—	1.341	_	1.526	ns
PLL Paramete	ers							
t _{RSTKREC_PLL}	After RSTK De-assert, Recovery Time Before Next Clock Edge Can Toggle K-divider Counter	1.000	_	1.000	_	1.000	_	ns
t _{RSTREC_PLL}	After RST De-assert, Recovery Time Before Next Clock Edge Can Toggle M-divider Counter (Applies to M-Divider Portion of RST Only ²)	1.000	_	1.000		1.000	_	ns
DSP Block Tir	DSP Block Timing							
t _{SUI_DSP}	Input Register Setup Time	0.135		0.151		0.166		ns
t _{HI_DSP}	Input Register Hold Time	0.021	—	-0.006	—	-0.031		ns
t _{SUP_DSP}	Pipeline Register Setup Time	2.505	—	2.784	—	3.064	—	ns

Over Recommended Operating Conditions



LatticeXP2 Internal Switching Characteristics¹ (Continued)

		-	7	-	6	-		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{HP_DSP}	Pipeline Register Hold Time	-0.787	_	-0.890	_	-0.994	—	ns
t _{SUO_DSP}	Output Register Setup Time	4.896	—	5.413	—	5.931	—	ns
t _{HO_DSP}	Output Register Hold Time	-1.439	—	-1.604	—	-1.770	—	ns
t _{COI_DSP} ³	Input Register Clock to Output Time	_	4.513	_	4.947	—	5.382	ns
t _{COP_DSP} ³	Pipeline Register Clock to Output Time	_	2.153	_	2.272	—	2.391	ns
t _{COO_DSP} ³	O_DSP ³ Output Register Clock to Output Time		0.569	_	0.600	—	0.631	ns
t _{SUADSUB}	AdSub Input Register Setup Time	-0.270	—	-0.298	_	-0.327	—	ns
t _{HADSUB}	AdSub Input Register Hold Time	0.306	—	0.338	—	0.371	—	ns

Over Recommended Operating Conditions

1. Internal parameters are characterized, but not tested on every device.

2. RST resets VCO and all counters in PLL.

3. These parameters include the Adder Subtractor block in the path.



LatticeXP2 Family Timing Adders^{1, 2, 3, 4} (Continued)

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	0.32	0.69	1.06	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	0.32	0.69	1.06	ns
SSTL33_I	SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33_II	SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33D_II	Differential SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL18_I	SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
LVTTL33_4mA	LVTTL 4mA drive	-0.37	-0.05	0.26	ns
LVTTL33_8mA	LVTTL 8mA drive	-0.45	-0.18	0.10	ns
LVTTL33_12mA	LVTTL 12mA drive	-0.52	-0.24	0.04	ns
LVTTL33_16mA	LVTTL 16mA drive	-0.43	-0.14	0.14	ns
LVTTL33_20mA	LVTTL 20mA drive	-0.46	-0.18	0.09	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	-0.37	-0.05	0.26	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	-0.45	-0.18	0.10	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	-0.52	-0.24	0.04	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	-0.43	-0.14	0.14	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	-0.46	-0.18	0.09	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	-0.42	-0.15	0.13	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	-0.48	-0.21	0.05	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	-0.45	-0.18	0.08	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	-0.49	-0.22	0.04	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	-0.46	-0.18	0.10	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	-0.52	-0.25	0.02	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.56	-0.30	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	-0.50	-0.24	0.03	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate	-0.45	-0.17	0.11	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate	-0.53	-0.26	0.00	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate	-0.46	-0.19	0.08	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate	-0.55	-0.29	-0.02	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate	0.98	1.41	1.84	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate	0.74	1.16	1.58	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate	0.56	0.97	1.38	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate	0.77	1.19	1.61	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate	0.57	0.98	1.40	ns

Over Recommended Operating Conditions



sysCLOCK PLL Timing

Parameter	Description	Conditions	Min.	Тур.	Max.	Units
f _{IN}	Input Clock Frequency (CLKI, CLKFB)		10		435	MHz
fouт	Output Clock Frequency (CLKOP, CLKOS)		10	_	435	MHz
fourz fvco fpFD AC Characte tDT tcPA tpH ⁴ toPJIT ¹	K-Divider Output Frequency	CLKOK	0.078		217.5	MHz
'OUT2		CLKOK2	3.3		145	MHz
f _{VCO}	PLL VCO Frequency		435	_	870	MHz
f _{PFD}	Phase Detector Input Frequency		10		435	MHz
AC Characte	eristics					
t _{DT}	Output Clock Duty Cycle	Default duty cycle selected ³	45	50	55	%
t _{CPA}	Coarse Phase Adjust		-5	0	5	%
t _{PH} ⁴	Output Phase Accuracy		-5	0	5	%
		f _{OUT} > 400 MHz	—		±50	ps
t _{OPJIT} 1	Output Clock Period Jitter	100 MHz < f _{OUT} < 400 MHz	—	_	±125	ps
tDT OL tCPA Cc tPH ⁴ OL tOPJIT ¹ OL tSK Inp tOPW OL		f _{OUT} < 100 MHz	—	_	0.025	UIPP
t _{SK}	Input Clock to Output Clock Skew	N/M = integer	—		±240	ps
t _{OPW}	Output Clock Pulse Width	At 90% or 10%	1	_	—	ns
+ 2	PLL Look in Timo	25 to 435 MHz	—	_	50	μs
LOCK		10 to 25 MHz	_		100	μs
t _{IPJIT}	Input Clock Period Jitter		_		±200	ps
t _{FBKDLY}	External Feedback Delay		_		10	ns
t _{HI}	Input Clock High Time	90% to 90%	0.5	_	—	ns
t _{LO}	Input Clock Low Time	10% to 10%	0.5		_	ns
t _{RSTKW}	Reset Signal Pulse Width (RSTK)		10	—	—	ns
t _{RSTW}	Reset Signal Pulse Width (RST)		500	—	—	ns

Over Recommended Operating Conditions

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. Relative to CLKOP.



FlashBAK Time (from EBR to Flash)

Over Recommended Operating Conditions

Device	EBR Density (Bits)	Time (Typ.)	Units
XP2-5	166K	1.5	S
XP2-8	221K	1.5	S
XP2-17	276K	1.5	S
XP2-30	387K	2.0	S
XP2-40	885K	3.0	S

JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	TCK Clock Frequency	—	25	MHz
t _{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t _{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t _{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t _{BTS}	TCK [BSCAN] setup time	8	—	ns
t _{BTH}	TCK [BSCAN] hold time	10	—	ns
t _{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t _{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t _{BTCODIS}	TAP controller falling edge of clock to valid disable	—	10	ns
t _{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t _{BTCRS}	BSCAN test capture register setup time	8	—	ns
t _{BTCRH}	BSCAN test capture register hold time	25	—	ns
t _{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
t _{BTUODIS}	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
t _{BTUPOEN}	BSCAN test update register, falling edge of clock to valid enable	_	25	ns



Pin Information Summary

			XP	2-5			XP	2-8			XP2-17	7	XP2-30		XP2-40		
Pin Ty	ре	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
Single Ended Use	er I/O	86	100	146	172	86	100	146	201	146	201	358	201	363	472	363	540
Differential Pair	Normal	35	39	57	66	35	39	57	77	57	77	135	77	137	180	137	204
User I/O	Highspeed	8	11	16	20	8	11	16	23	16	23	44	23	44	56	44	66
	TAP	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
Configuration	Muxed	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9
	Dedicated	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Non Configura-	Muxed	5	5	7	7	7	7	9	9	11	11	21	7	11	13	11	13
tion	Dedicated	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Vcc		6	4	9	6	6	4	9	6	9	6	16	6	16	20	16	20
Vccaux		4	4	4	4	4	4	4	4	4	4	8	4	8	8	8	8
VCCPLL		2	2	2	-	2	2	2	-	4	-	-	-	-	-	-	-
	Bank0	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
	Bank1	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank2	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
VCCIO	Bank3	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
10010	Bank4	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank5	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
	Bank6	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank7	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
GND, GND0-GNI	77	15	15	20	20	15	15	22	20	22	20	56	20	56	64	56	64
NC		-	-	4	31	-	-	2	2	-	2	7	2	2	69	2	1
	Bank0	18/9	20/10	20/10	26/13	18/9	20/10	20/10	28/14	20/10	28/14	52/26	28/14	52/26	70/35	52/26	70/35
	Bank1	4/2	6/3	18/9	18/9	4/2	6/3	18/9	22/11	18/9	22/11	36/18	22/11	36/18	54/27	36/18	70/35
	Bank2	16/8	18/9	18/9	22/11	16/8	18/9	18/9	26/13	18/9	26/13	46/23	26/13	46/23	56/28	46/23	64/32
Single Ended/	Bank3	4/2	4/2	16/8	20/10	4/2	4/2	16/8	24/12	16/8	24/12	44/22	24/12	46/23	56/28	46/23	66/33
per Bank	Bank4	8/4	8/4	18/9	18/9	8/4	8/4	18/9	26/13	18/9	26/13	36/18	26/13	38/19	54/27	38/19	70/35
	Bank5	14/7	18/9	20/10	24/12	14/7	18/9	20/10	24/12	20/10	24/12	52/26	24/12	53/26	70/35	53/26	70/35
	Bank6	6/3	8/4	18/9	22/11	6/3	8/4	18/9	27/13	18/9	27/13	46/23	27/13	46/23	56/28	46/23	66/33
	Bank7	16/8	18/9	18/9	22/11	16/8	18/9	18/9	24/12	18/9	24/12	46/23	24/12	46/23	56/28	46/23	64/32
	Bank0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank2	3	4	4	5	3	4	4	6	4	6	11	6	11	14	11	16
True LVDS Pairs	Bank3	1	1	4	5	1	1	4	6	4	6	11	6	11	14	11	17
Bank	Bank4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank6	1	2	4	5	1	2	4	6	4	6	11	6	11	14	11	17
	Bank7	3	4	4	5	3	4	4	5	4	5	11	5	11	14	11	16
	Bank0	1	1	1	1	1	1	1	1	1	1	3	1	2	4	2	4
	Bank1	0	0	1	1	0	0	1	1	1	1	2	1	2	3	2	4
	Bank2	1	1	1	1	1	1	1	1	1	1	2	1	3	3	3	4
DDR Banks	Bank3	0	0	1	1	0	0	1	1	1	1	2	1	3	3	3	4
I/O Bank ¹	Bank4	0	0	1	1	0	0	1	1	1	1	2	1	2	3	2	4
	Bank5	1	1	1	1	1	1	1	1	1	1	3	1	2	4	2	4
	Bank6	0	0	1	1	0	0	1	1	1	1	2	1	3	3	3	4
	Bank7	1	1	1	1	1	1	1	1	1	1	2	1	3	3	3	4



Pin Information Summary (Cont.)

		XP2-5				XP2-8			XP2-17			XP2-30		XP2-40			
Pin Type		132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
	Bank0	18	20	20	26	18	20	20	28	20	28	52	28	52	70	52	70
	Bank1	4	6	18	18	4	6	18	22	18	22	36	22	36	54	36	70
	Bank2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI capable I/Os	Bank3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bank	Bank4	8	8	18	18	8	8	18	26	18	26	36	26	38	54	38	70
	Bank5	14	18	20	24	14	18	20	24	20	24	52	24	53	70	53	70
	Bank6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

Logic Signal Connections

Package pinout information can be found under "Data Sheets" on the LatticeXP2 product page of the Lattice website a www.latticesemi.com/products/fpga/xp2 and in the Lattice Diamond design software.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Lattice <u>Thermal Management</u> document to find the device/ package specific thermal values.

For Further Information

- TN1139, Power Estimation and Management for LatticeXP2 Devices
- Power Calculator tool is included with the Lattice Diamond design tool or as a standalone download from www.latticesemi.com/products/designsoftware



Lead-Free Packaging

Commercial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5MN132C	1.2V	-5	Lead-Free csBGA	132	COM	5
LFXP2-5E-6MN132C	1.2V	-6	Lead-Free csBGA	132	COM	5
LFXP2-5E-7MN132C	1.2V	-7	Lead-Free csBGA	132	COM	5
LFXP2-5E-5TN144C	1.2V	-5	Lead-Free TQFP	144	COM	5
LFXP2-5E-6TN144C	1.2V	-6	Lead-Free TQFP	144	COM	5
LFXP2-5E-7TN144C	1.2V	-7	Lead-Free TQFP	144	COM	5
LFXP2-5E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	5
LFXP2-5E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	5
LFXP2-5E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	5
LFXP2-5E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	5
LFXP2-5E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	5
LFXP2-5E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5MN132C	1.2V	-5	Lead-Free csBGA	132	COM	8
LFXP2-8E-6MN132C	1.2V	-6	Lead-Free csBGA	132	COM	8
LFXP2-8E-7MN132C	1.2V	-7	Lead-Free csBGA	132	COM	8
LFXP2-8E-5TN144C	1.2V	-5	Lead-Free TQFP	144	COM	8
LFXP2-8E-6TN144C	1.2V	-6	Lead-Free TQFP	144	COM	8
LFXP2-8E-7TN144C	1.2V	-7	Lead-Free TQFP	144	COM	8
LFXP2-8E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	8
LFXP2-8E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	8
LFXP2-8E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	8
LFXP2-8E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	8
LFXP2-8E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	8
LFXP2-8E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	17
LFXP2-17E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	17
LFXP2-17E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	17
LFXP2-17E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	17
LFXP2-17E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	17
LFXP2-17E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	17
LFXP2-17E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	17
LFXP2-17E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	17
LFXP2-17E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	17