Lattice Semiconductor Corporation - LFXP2-17E-6FN484I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2125
Number of Logic Elements/Cells	17000
Total RAM Bits	282624
Number of I/O	358
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-17e-6fn484i

Figure 2-4. General Purpose PLL (GPLL) Diagram

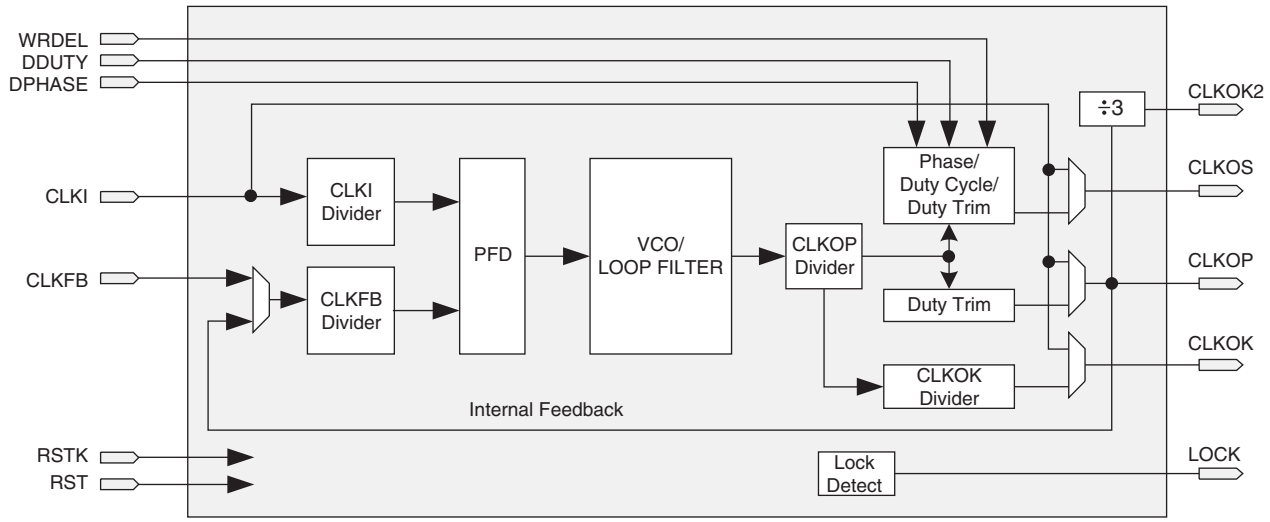


Table 2-4 provides a description of the signals in the GPLL blocks.

Table 2-4. GPLL Block Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
DPHASE [3:0]	I	DPA Phase Adjust input
DDDUTY [3:0]	I	DPA Duty Cycle Select input
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
CLKOK2	O	PLL output to clock tree (CLKOP divided by 3)
LOCK	O	"1" indicates PLL LOCK to CLKI

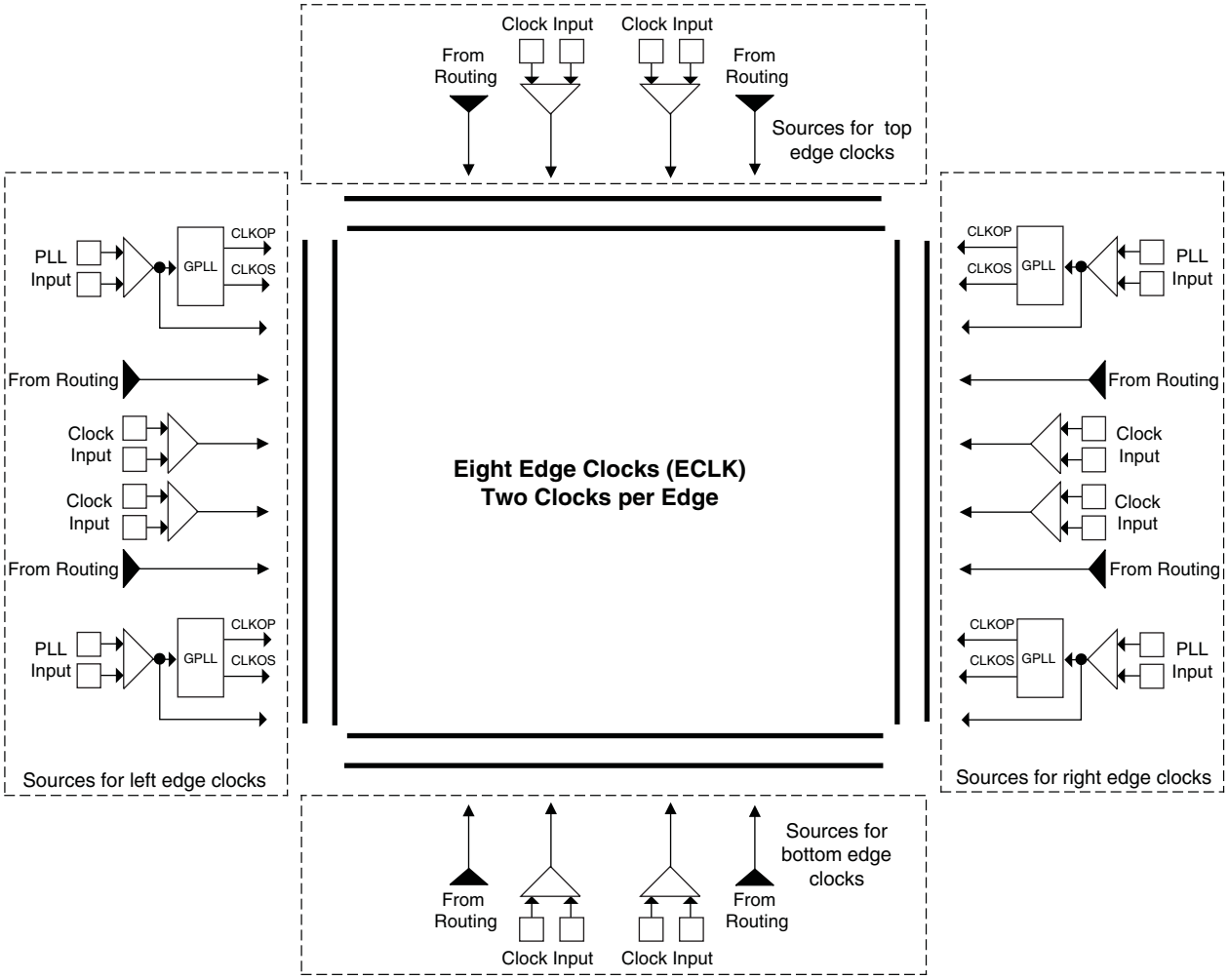
Clock Dividers

LatticeXP2 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from the CLKOP output from the GPLLs or from the Edge Clocks (ECLK). The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets the input and forces all outputs to low. The RELEASE signal releases outputs to the input clock. For further information on clock dividers, please see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide. Figure 2-5 shows the clock divider connections.

Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs and clock dividers as shown in Figure 2-8.

Figure 2-8. Edge Clock Sources



Note: This diagram shows sources for the XP2-17 device. Smaller LatticeXP2 devices have two GPLLs.

sysMEM Memory

LatticeXP2 devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of 18 Kbit RAM with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-5. FIFOs can be implemented in sysMEM EBR blocks by using support logic with PFUs. The EBR block supports an optional parity bit for each data byte to facilitate parity checking. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths.

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

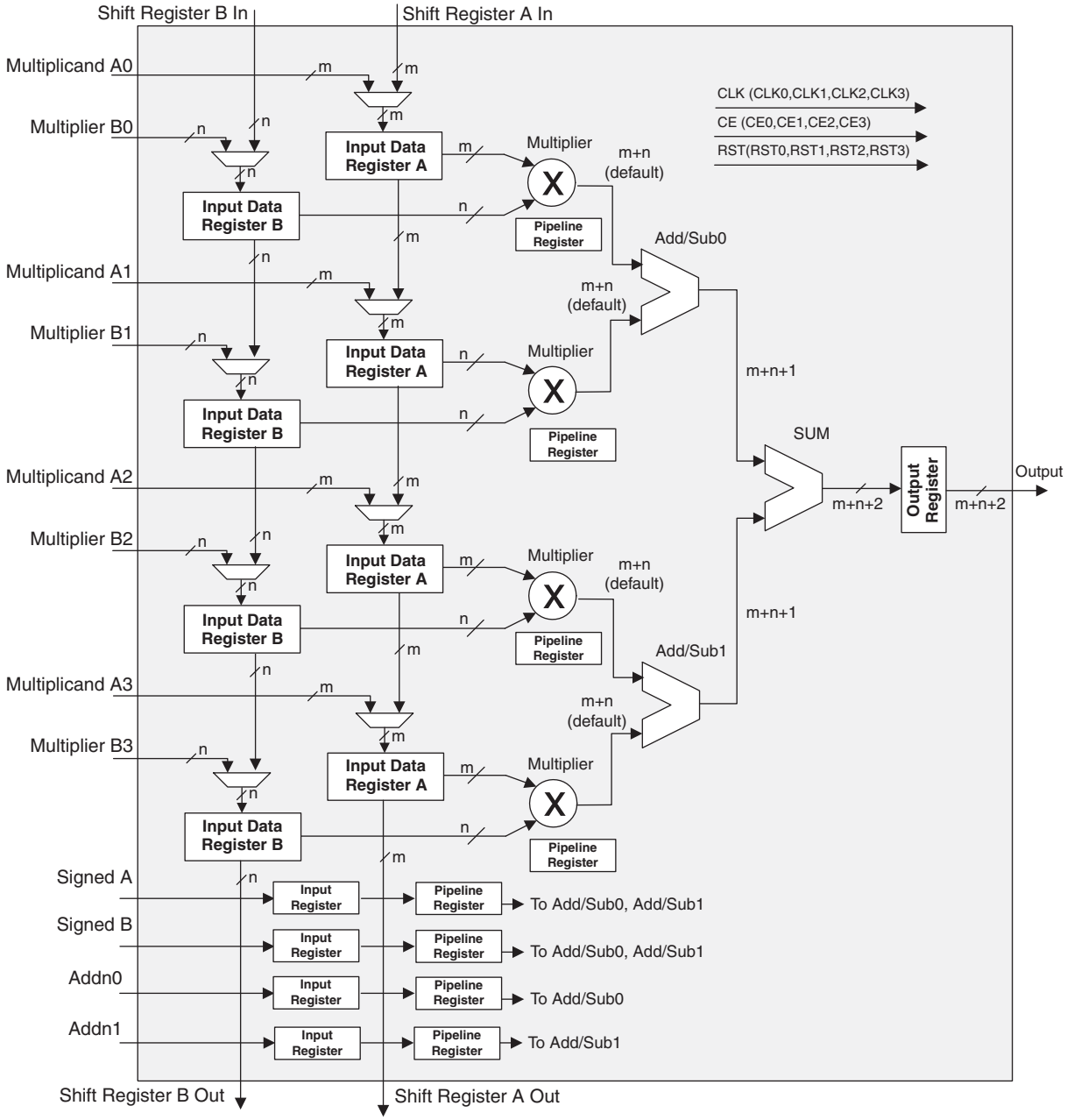
FlashBAK EBR Content Storage

All the EBR memory in the LatticeXP2 is shadowed by Flash memory. Optionally, initialization values for the memory blocks can be defined using the Lattice Diamond design tools. The initialization values are loaded into the Flash memory during device programming and into the SRAM at power up or whenever the device is reconfigured. This feature is ideal for the storage of a variety of information such as look-up tables and microprocessor code. It is also possible to write the current contents of the EBR memory back to Flash memory. This capability is useful for the storage of data such as error codes and calibration information. For additional information on the FlashBAK capability see TN1137, LatticeXP2 Memory Usage Guide.

MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-23 shows the MULTADDSUBSUM sysDSP element.

Figure 2-23. MULTADDSUBSUM

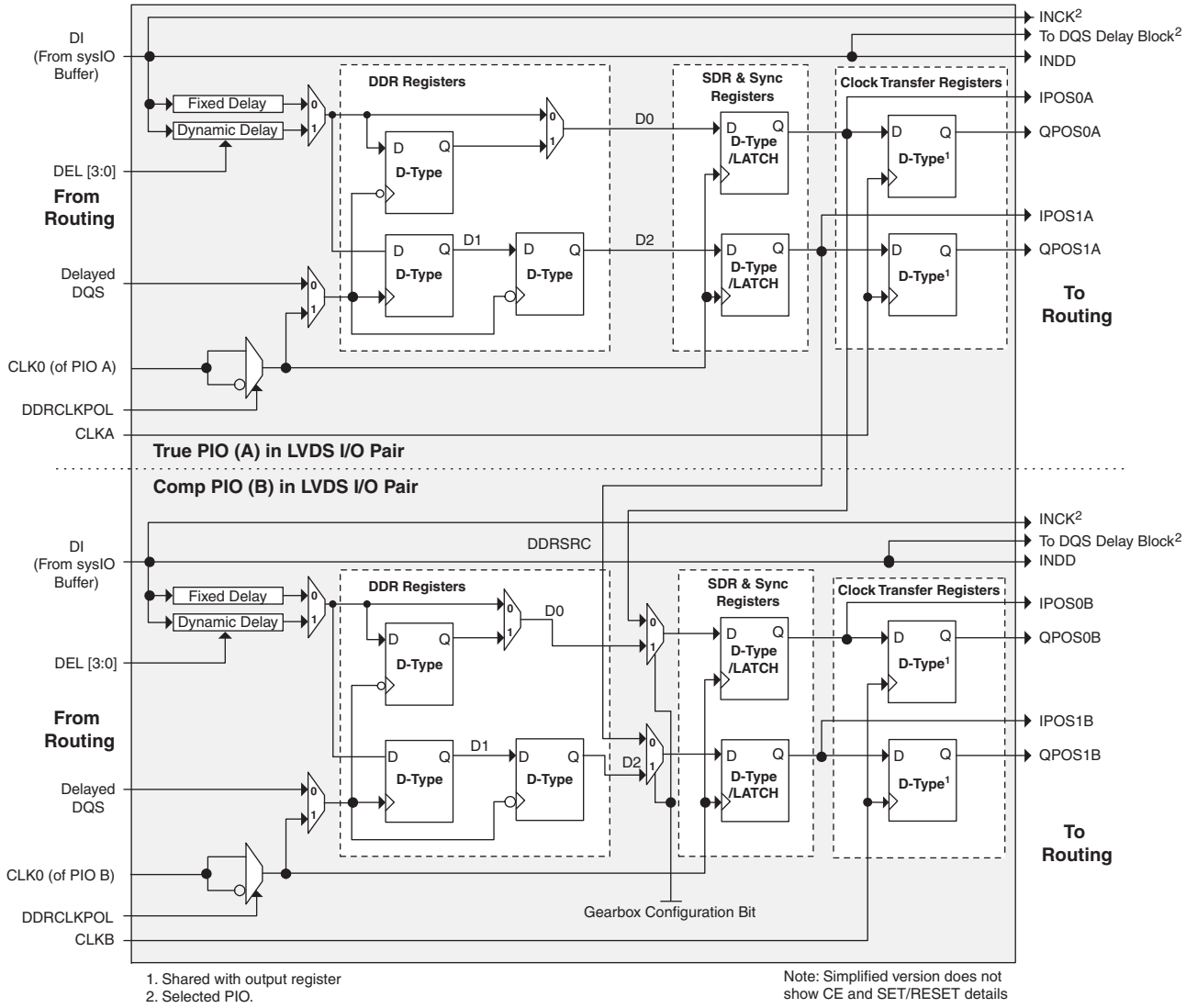


Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable (CE) and Reset (RST) signals from routing are available to every DSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.

Figure 2-26. Input Register Block



1. Shared with output register
2. Selected PIO.

Note: Simplified version does not show CE and SET/RESET details

Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The blocks on the PIOs on the left, right and bottom contain registers for SDR operation that are combined with an additional latch for DDR operation. Figure 2-27 shows the diagram of the Output Register Block for PIOs.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or latch. In DDR mode, ONEG0 and OPOS0 are fed into registers on the positive edge of the clock. At the next clock cycle the registered OPOS0 is latched. A multiplexer running off the same clock cycle selects the correct register to feed the output (D0).

By combining output blocks of the complementary PIOs and sharing some registers from input blocks, a gearbox function can be implemented, to take four data streams ONEG0A, ONEG1A, ONEG1B and ONEG1B. Figure 2-27

shows the diagram using this gearbox function. For more information on this topic, see TN1138, LatticeXP2 High Speed I/O Interface.

Figure 2-27. Output and Tristate Block

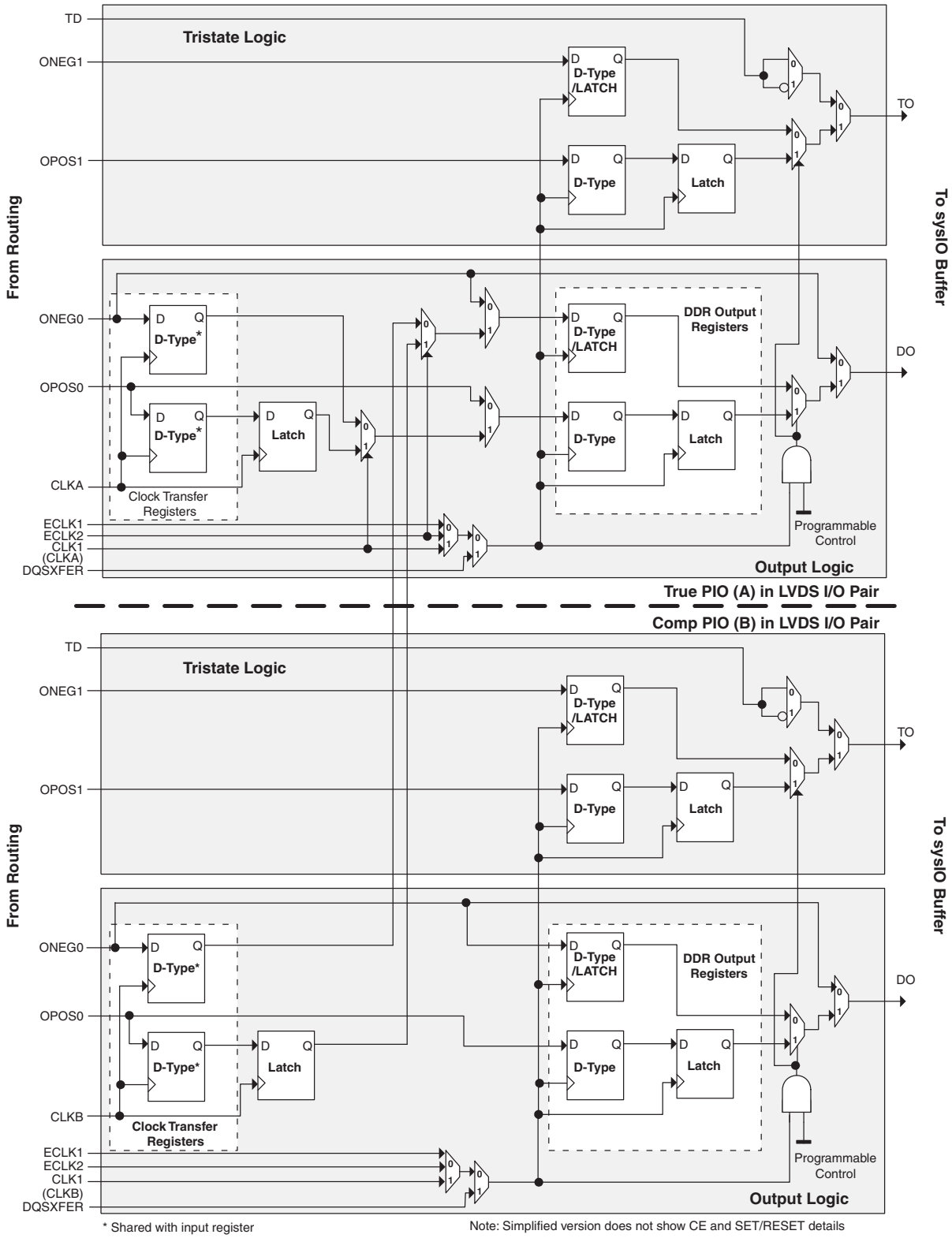
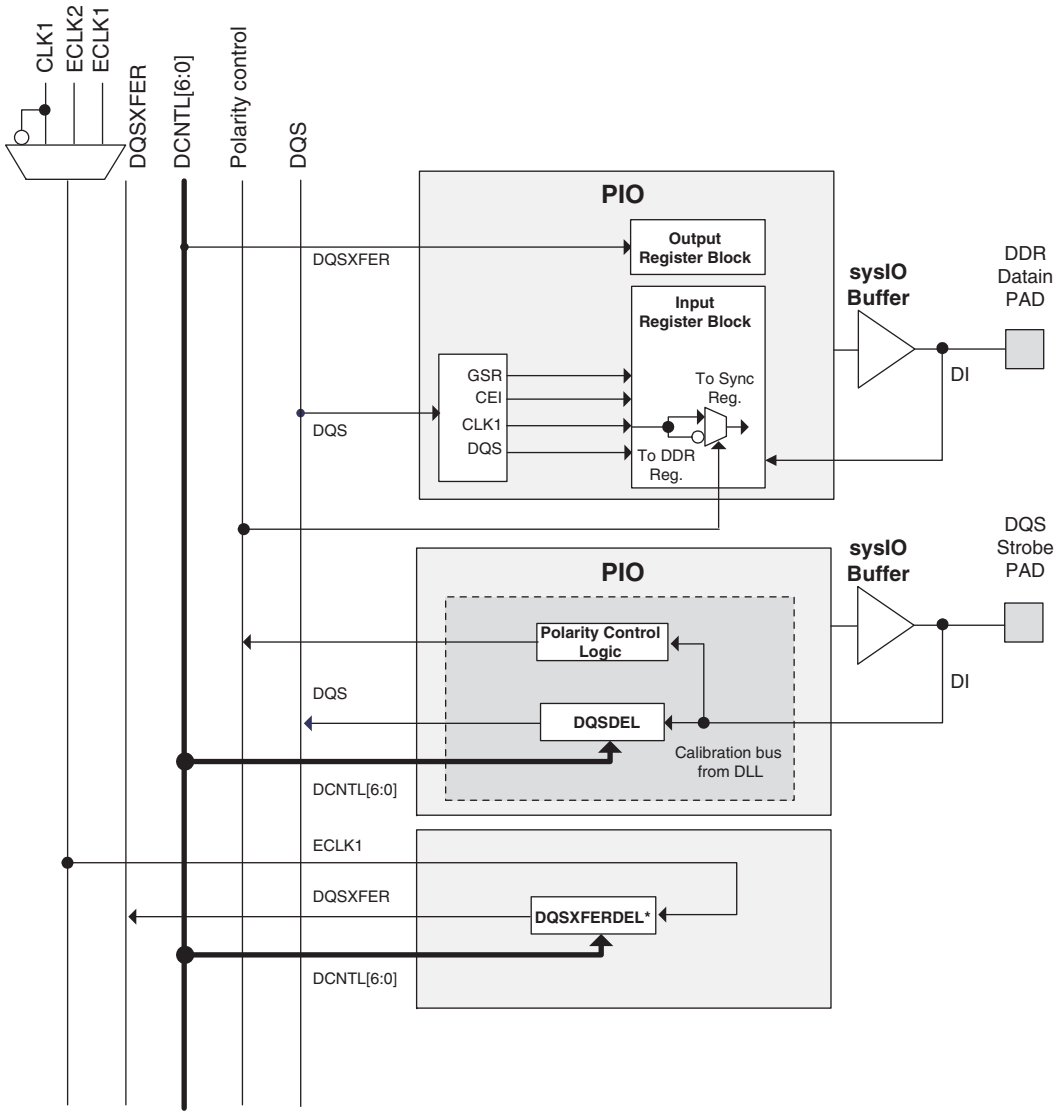


Figure 2-31. DQS Local Bus



*DQSXFERDEL shifts ECLK1 by 90% and is not associated with a particular PIO.

Polarity Control Logic

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeXP2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block and requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

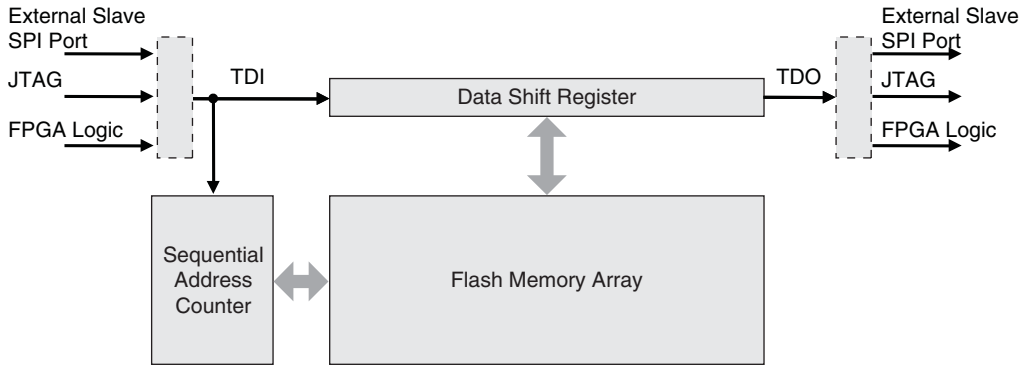
1. Unlocked
2. Key Locked – Presenting the key through the programming interface allows the device to be unlocked.
3. Permanently Locked – The device is permanently locked.

To further complement the security of the device a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash portion of the device.

Serial TAG Memory

LatticeXP2 devices offer 0.6 to 3.3kbits of Flash memory in the form of Serial TAG memory. The TAG memory is an area of the on-chip Flash that can be used for non-volatile storage including electronic ID codes, version codes, date stamps, asset IDs and calibration settings. A block diagram of the TAG memory is shown in Figure 2-34. The TAG memory is accessed in the same way as external SPI Flash and it can be read or programmed either through JTAG, an external Slave SPI Port, or directly from FPGA logic. To read the TAG memory, a start address is specified and the entire TAG memory contents are read sequentially in a first-in-first-out manner. The TAG memory is independent of the Flash used for device configuration and given its use for general-purpose storage functions is always accessible regardless of the device security settings. For more information, see TN1137, LatticeXP2 Memory Usage Guide and TN1141, LatticeXP2 sysCONFIG Usage Guide.

Figure 2-34. Serial TAG Memory Diagram



Live Update Technology

Many applications require field updates of the FPGA. LatticeXP2 devices provide three features that enable this configuration to be done in a secure and failsafe manner while minimizing impact on system operation.

1. **Decryption Support**
   LatticeXP2 devices provide on-chip, non-volatile key storage to support decryption of a 128-bit AES encrypted bitstream, securing designs and deterring design piracy.

2. **TransFR (Transparent Field Reconfiguration)**
   TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. For more information please see TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

3. **Dual Boot Image Support**
   Dual boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeXP2 can be re-booted from this new configuration file. If there is a problem such as corrupt data during download or incorrect version number with this new boot image, the LatticeXP2 device can revert back to the

sysIO Single-Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}		
	Min. (V)	Max. (V)	Min. (V)	Max. (V)	Max. (V)	Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
LVCMOS33	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL33	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS25	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS18	-0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS15	-0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS12	-0.3	0.35 V_{CC}	0.65 V_{CC}	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI33	-0.3	0.3 V_{CCIO}	0.5 V_{CCIO}	3.6	0.1 V_{CCIO}	0.9 V_{CCIO}	1.5	-0.5
SSTL33_I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	-8
SSTL33_II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	-16
SSTL25_I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	-7.6
							12	-12
SSTL25_II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	-15.2
							20	-20
SSTL18_I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	-6.7
SSTL18_II	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.28	V_{CCIO} - 0.28	8	-8
							11	-11
HSTL15_I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	4	-4
							8	-8
HSTL18_I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	-8
							12	-12
HSTL18_II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	-16

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA, where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

sysIO Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage		0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	+/-10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9V	1.03	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SA}	Output Short Circuit Current	V_{OD} = 0V Driver Outputs Shorted to Ground	—	—	24	mA
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V Driver Outputs Shorted to Each Other	—	—	12	mA

Differential HSTL and SSTL

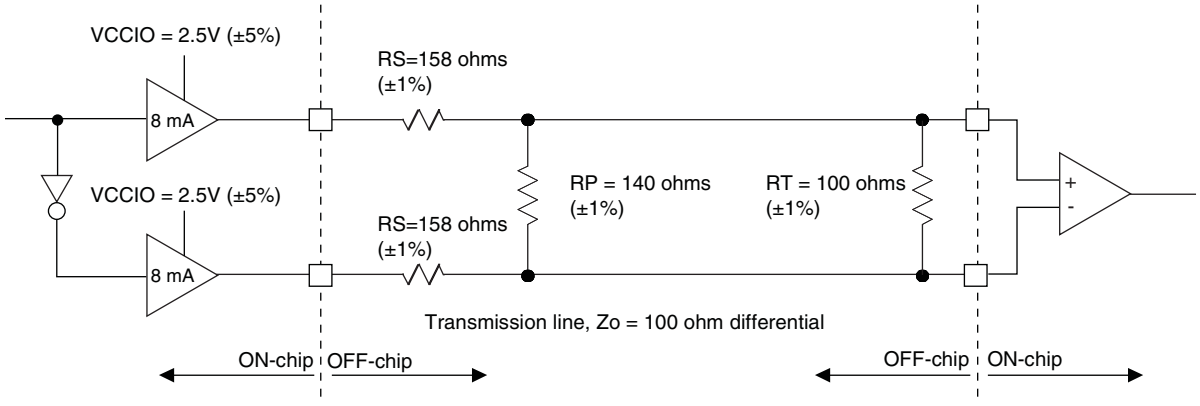
Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see details in additional technical notes listed at the end of this data sheet.

LVDS25E

The top and bottom sides of LatticeXP2 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example



LatticeXP2 External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (using Primary Clock without PLL)[1]									
t_{CO}	Clock to Output - PIO Output Register	XP2-5	—	3.80	—	4.20	—	4.60	ns
		XP2-8	—	3.80	—	4.20	—	4.60	ns
		XP2-17	—	3.80	—	4.20	—	4.60	ns
		XP2-30	—	4.00	—	4.40	—	4.90	ns
		XP2-40	—	4.00	—	4.40	—	4.90	ns
t_{SU}	Clock to Data Setup - PIO Input Register	XP2-5	0.00	—	0.00	—	0.00	—	ns
		XP2-8	0.00	—	0.00	—	0.00	—	ns
		XP2-17	0.00	—	0.00	—	0.00	—	ns
		XP2-30	0.00	—	0.00	—	0.00	—	ns
		XP2-40	0.00	—	0.00	—	0.00	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	XP2-5	1.40	—	1.70	—	1.90	—	ns
		XP2-8	1.40	—	1.70	—	1.90	—	ns
		XP2-17	1.40	—	1.70	—	1.90	—	ns
		XP2-30	1.40	—	1.70	—	1.90	—	ns
		XP2-40	1.40	—	1.70	—	1.90	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	XP2-5	1.40	—	1.70	—	1.90	—	ns
		XP2-8	1.40	—	1.70	—	1.90	—	ns
		XP2-17	1.40	—	1.70	—	1.90	—	ns
		XP2-30	1.40	—	1.70	—	1.90	—	ns
		XP2-40	1.40	—	1.70	—	1.90	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	XP2-5	0.00	—	0.00	—	0.00	—	ns
		XP2-8	0.00	—	0.00	—	0.00	—	ns
		XP2-17	0.00	—	0.00	—	0.00	—	ns
		XP2-30	0.00	—	0.00	—	0.00	—	ns
		XP2-40	0.00	—	0.00	—	0.00	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	XP2	—	420	—	357	—	311	MHz
General I/O Pin Parameters (using Edge Clock without PLL)[1]									
t_{COE}	Clock to Output - PIO Output Register	XP2-5	—	3.20	—	3.60	—	3.90	ns
		XP2-8	—	3.20	—	3.60	—	3.90	ns
		XP2-17	—	3.20	—	3.60	—	3.90	ns
		XP2-30	—	3.20	—	3.60	—	3.90	ns
		XP2-40	—	3.20	—	3.60	—	3.90	ns
t_{SUE}	Clock to Data Setup - PIO Input Register	XP2-5	0.00	—	0.00	—	0.00	—	ns
		XP2-8	0.00	—	0.00	—	0.00	—	ns
		XP2-17	0.00	—	0.00	—	0.00	—	ns
		XP2-30	0.00	—	0.00	—	0.00	—	ns
		XP2-40	0.00	—	0.00	—	0.00	—	ns

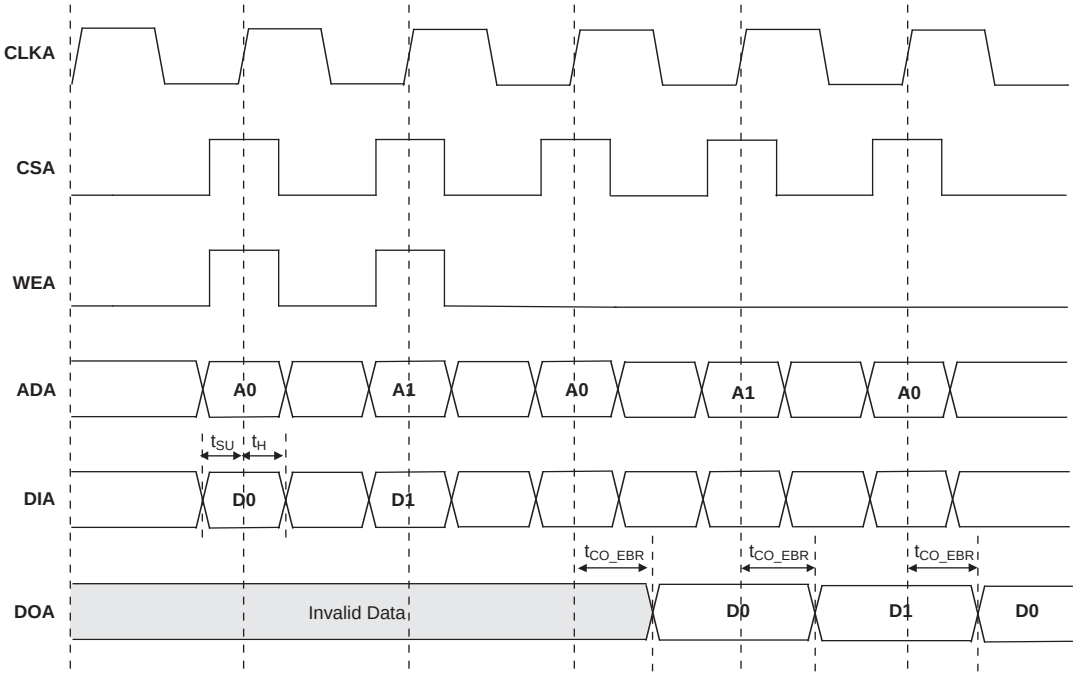
LatticeXP2 External Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HE}	Clock to Data Hold - PIO Input Register	XP2-5	1.00	—	1.30	—	1.60	—	ns
		XP2-8	1.00	—	1.30	—	1.60	—	ns
		XP2-17	1.00	—	1.30	—	1.60	—	ns
		XP2-30	1.20	—	1.60	—	1.90	—	ns
		XP2-40	1.20	—	1.60	—	1.90	—	ns
t_{SU_DELE}	Clock to Data Setup - PIO Input Register with Data Input Delay	XP2-5	1.00	—	1.30	—	1.60	—	ns
		XP2-8	1.00	—	1.30	—	1.60	—	ns
		XP2-17	1.00	—	1.30	—	1.60	—	ns
		XP2-30	1.20	—	1.60	—	1.90	—	ns
		XP2-40	1.20	—	1.60	—	1.90	—	ns
t_{H_DELE}	Clock to Data Hold - PIO Input Register with Input Data Delay	XP2-5	0.00	—	0.00	—	0.00	—	ns
		XP2-8	0.00	—	0.00	—	0.00	—	ns
		XP2-17	0.00	—	0.00	—	0.00	—	ns
		XP2-30	0.00	—	0.00	—	0.00	—	ns
		XP2-40	0.00	—	0.00	—	0.00	—	ns
f_{MAX_IOE}	Clock Frequency of I/O and PFU Register	XP2	—	420	—	357	—	311	MHz
General I/O Pin Parameters (using Primary Clock with PLL)[1]									
t_{COPLL}	Clock to Output - PIO Output Register	XP2-5	—	3.00	—	3.30	—	3.70	ns
		XP2-8	—	3.00	—	3.30	—	3.70	ns
		XP2-17	—	3.00	—	3.30	—	3.70	ns
		XP2-30	—	3.00	—	3.30	—	3.70	ns
		XP2-40	—	3.00	—	3.30	—	3.70	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	XP2-5	1.00	—	1.20	—	1.40	—	ns
		XP2-8	1.00	—	1.20	—	1.40	—	ns
		XP2-17	1.00	—	1.20	—	1.40	—	ns
		XP2-30	1.00	—	1.20	—	1.40	—	ns
		XP2-40	1.00	—	1.20	—	1.40	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	XP2-5	0.90	—	1.10	—	1.30	—	ns
		XP2-8	0.90	—	1.10	—	1.30	—	ns
		XP2-17	0.90	—	1.10	—	1.30	—	ns
		XP2-30	1.00	—	1.20	—	1.40	—	ns
		XP2-40	1.00	—	1.20	—	1.40	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	XP2-5	1.90	—	2.10	—	2.30	—	ns
		XP2-8	1.90	—	2.10	—	2.30	—	ns
		XP2-17	1.90	—	2.10	—	2.30	—	ns
		XP2-30	2.00	—	2.20	—	2.40	—	ns
		XP2-40	2.00	—	2.20	—	2.40	—	ns

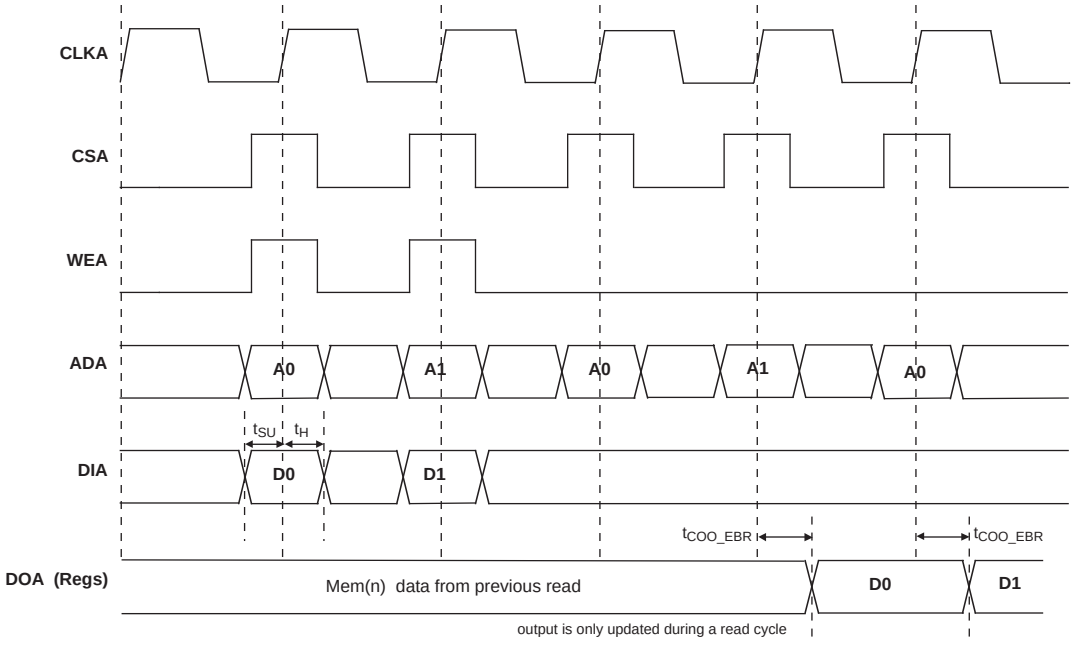
EBR Timing Diagrams

Figure 3-6. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-7. Read/Write Mode with Input and Output Registers



LatticeXP2 Family Timing Adders[1, 2, 3, 4]

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
Input Adjusters					
LVDS25	LVDS	-0.26	-0.11	0.04	ns
BLVDS25	BLVDS	-0.26	-0.11	0.04	ns
MLVDS	LVDS	-0.26	-0.11	0.04	ns
RSDS	RSDS	-0.26	-0.11	0.04	ns
LVPECL33	LVPECL	-0.26	-0.11	0.04	ns
HSTL18_I	HSTL_18 class I	-0.23	-0.08	0.07	ns
HSTL18_II	HSTL_18 class II	-0.23	-0.08	0.07	ns
HSTL18D_I	Differential HSTL 18 class I	-0.28	-0.13	0.02	ns
HSTL18D_II	Differential HSTL 18 class II	-0.28	-0.13	0.02	ns
HSTL15_I	HSTL_15 class I	-0.23	-0.09	0.06	ns
HSTL15D_I	Differential HSTL 15 class I	-0.28	-0.13	0.01	ns
SSTL33_I	SSTL_3 class I	-0.20	-0.04	0.12	ns
SSTL33_II	SSTL_3 class II	-0.20	-0.04	0.12	ns
SSTL33D_I	Differential SSTL_3 class I	-0.27	-0.11	0.04	ns
SSTL33D_II	Differential SSTL_3 class II	-0.27	-0.11	0.04	ns
SSTL25_I	SSTL_2 class I	-0.21	-0.06	0.10	ns
SSTL25_II	SSTL_2 class II	-0.21	-0.06	0.10	ns
SSTL25D_I	Differential SSTL_2 class I	-0.27	-0.12	0.03	ns
SSTL25D_II	Differential SSTL_2 class II	-0.27	-0.12	0.03	ns
SSTL18_I	SSTL_18 class I	-0.23	-0.08	0.07	ns
SSTL18_II	SSTL_18 class II	-0.23	-0.08	0.07	ns
SSTL18D_I	Differential SSTL_18 class I	-0.28	-0.13	0.02	ns
SSTL18D_II	Differential SSTL_18 class II	-0.28	-0.13	0.02	ns
LVTTL33	LVTTL	-0.09	0.05	0.18	ns
LVCMOS33	LVCMOS 3.3	-0.09	0.05	0.18	ns
LVCMOS25	LVCMOS 2.5	0.00	0.00	0.00	ns
LVCMOS18	LVCMOS 1.8	-0.23	-0.07	0.09	ns
LVCMOS15	LVCMOS 1.5	-0.20	-0.02	0.16	ns
LVCMOS12	LVCMOS 1.2	-0.35	-0.20	-0.04	ns
PCI33	3.3V PCI	-0.09	0.05	0.18	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E[5]	-0.25	0.02	0.30	ns
LVDS25	LVDS 2.5	-0.25	0.02	0.30	ns
BLVDS25	BLVDS 2.5	-0.28	0.00	0.28	ns
MLVDS	MLVDS 2.5[5]	-0.28	0.00	0.28	ns
RSDS	RSDS 2.5[5]	-0.25	0.02	0.30	ns
LVPECL33	LVPECL 3.3[5]	-0.37	-0.10	0.18	ns
HSTL18_I	HSTL_18 class I 8mA drive	-0.17	0.13	0.43	ns
HSTL18_II	HSTL_18 class II	-0.29	0.00	0.29	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	-0.17	0.13	0.43	ns
HSTL18D_II	Differential HSTL 18 class II	-0.29	0.00	0.29	ns

LatticeXP2 Family Timing Adders[1, 2, 3, 4] (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	0.32	0.69	1.06	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	0.32	0.69	1.06	ns
SSTL33_I	SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33_II	SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33D_II	Differential SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL18_I	SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
LVTTL33_4mA	LVTTL 4mA drive	-0.37	-0.05	0.26	ns
LVTTL33_8mA	LVTTL 8mA drive	-0.45	-0.18	0.10	ns
LVTTL33_12mA	LVTTL 12mA drive	-0.52	-0.24	0.04	ns
LVTTL33_16mA	LVTTL 16mA drive	-0.43	-0.14	0.14	ns
LVTTL33_20mA	LVTTL 20mA drive	-0.46	-0.18	0.09	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	-0.37	-0.05	0.26	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	-0.45	-0.18	0.10	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	-0.52	-0.24	0.04	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	-0.43	-0.14	0.14	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	-0.46	-0.18	0.09	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	-0.42	-0.15	0.13	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	-0.48	-0.21	0.05	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	-0.45	-0.18	0.08	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	-0.49	-0.22	0.04	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	-0.46	-0.18	0.10	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	-0.52	-0.25	0.02	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.56	-0.30	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	-0.50	-0.24	0.03	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate	-0.45	-0.17	0.11	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate	-0.53	-0.26	0.00	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate	-0.46	-0.19	0.08	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate	-0.55	-0.29	-0.02	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate	0.98	1.41	1.84	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate	0.74	1.16	1.58	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate	0.56	0.97	1.38	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate	0.77	1.19	1.61	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate	0.57	0.98	1.40	ns

Flash Download Time (from On-Chip Flash to SRAM)

Over Recommended Operating Conditions

Symbol	Parameter		Min.	Typ.	Max.	Units
$t_{REFRESH}$	PROGRAMN Low-to-High. Transition to Done High.	XP2-5	—	1.8	2.1	ms
		XP2-8	—	1.9	2.3	ms
		XP2-17	—	1.7	2.0	ms
		XP2-30	—	2.0	2.1	ms
		XP2-40	—	2.0	2.3	ms
	Power-up refresh when PROGRAMN is pulled up to V_{CC} (V_{CC}=V_{CC} Min)	XP2-5	—	1.8	2.1	ms
		XP2-8	—	1.9	2.3	ms
		XP2-17	—	1.7	2.0	ms
		XP2-30	—	2.0	2.1	ms
		XP2-40	—	2.0	2.3	ms

Flash Program Time

Over Recommended Operating Conditions

Device	Flash Density		Program Time Typ.	Units
XP2-5	1.2M	TAG	1.0	ms
		Main Array	1.1	s
XP2-8	2.0M	TAG	1.0	ms
		Main Array	1.4	s
XP2-17	3.6M	TAG	1.0	ms
		Main Array	1.8	s
XP2-30	6.0M	TAG	2.0	ms
		Main Array	3.0	s
XP2-40	8.0M	TAG	2.0	ms
		Main Array	4.0	s

Flash Erase Time

Over Recommended Operating Conditions

Device	Flash Density		Erase Time Typ.	Units
XP2-5	1.2M	TAG	1.0	s
		Main Array	3.0	s
XP2-8	2.0M	TAG	1.0	s
		Main Array	4.0	s
XP2-17	3.6M	TAG	1.0	s
		Main Array	5.0	s
XP2-30	6.0M	TAG	2.0	s
		Main Array	7.0	s
XP2-40	8.0M	TAG	2.0	s
		Main Array	9.0	s

FlashBAK Time (from EBR to Flash)

Over Recommended Operating Conditions

Device	EBR Density (Bits)	Time (Typ.)	Units
XP2-5	166K	1.5	s
XP2-8	221K	1.5	s
XP2-17	276K	1.5	s
XP2-30	387K	2.0	s
XP2-40	885K	3.0	s

JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK Clock Frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Signal Descriptions (Cont.)

Signal Name	I/O	Description
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used during sysCONFIG)		
CFG[1:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, an internal pull-up is enabled.
INITN[1]	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
SISPI[2]	I/O	Input data pin in slave SPI mode and Output data pin in Master SPI mode.
SOSPI[2]	I/O	Output data pin in slave SPI mode and Input data pin in Master SPI mode.
CSSPIN[2]	O	Chip select for external SPI Flash memory in Master SPI mode. This pin has a weak internal pull-up.
CSSPISN	I	Chip select in Slave SPI mode. This pin has a weak internal pull-up.
TOE	I	Test Output Enable tristates all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to V_{CC} is recommended.

1. If not actively driven, the internal pull-up may not be sufficient. An external pull-up resistor of 4.7k to 10kΩ is recommended.
2. When using the device in Master SPI mode, it must be mutually exclusive from JTAG operations (i.e. TCK tied to GND) or the JTAG TCK must be free-running when used in a system JTAG test environment. If Master SPI mode is used in conjunction with a JTAG download cable, the device power cycle is required after the cable is unplugged.

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-30E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	30
LFXP2-30E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	30
LFXP2-30E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	30
LFXP2-30E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	30
LFXP2-30E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	30
LFXP2-30E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	30
LFXP2-30E-5FN672C	1.2V	-5	Lead-Free fpBGA	672	COM	30
LFXP2-30E-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	30
LFXP2-30E-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	30

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	40
LFXP2-40E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	40
LFXP2-40E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	40
LFXP2-40E-5FN672C	1.2V	-5	Lead-Free fpBGA	672	COM	40
LFXP2-40E-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	40
LFXP2-40E-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	40

Industrial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5MN132I	1.2V	-5	Lead-Free csBGA	132	IND	5
LFXP2-5E-6MN132I	1.2V	-6	Lead-Free csBGA	132	IND	5
LFXP2-5E-5TN144I	1.2V	-5	Lead-Free TQFP	144	IND	5
LFXP2-5E-6TN144I	1.2V	-6	Lead-Free TQFP	144	IND	5
LFXP2-5E-5QN208I	1.2V	-5	Lead-Free PQFP	208	IND	5
LFXP2-5E-6QN208I	1.2V	-6	Lead-Free PQFP	208	IND	5
LFXP2-5E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	5
LFXP2-5E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5MN132I	1.2V	-5	Lead-Free csBGA	132	IND	8
LFXP2-8E-6MN132I	1.2V	-6	Lead-Free csBGA	132	IND	8
LFXP2-8E-5TN144I	1.2V	-5	Lead-Free TQFP	144	IND	8
LFXP2-8E-6TN144I	1.2V	-6	Lead-Free TQFP	144	IND	8
LFXP2-8E-5QN208I	1.2V	-5	Lead-Free PQFP	208	IND	8
LFXP2-8E-6QN208I	1.2V	-6	Lead-Free PQFP	208	IND	8
LFXP2-8E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	8
LFXP2-8E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	8

Date	Version	Section	Change Summary
April 2008 (cont.)	01.4 (cont.)	DC and Switching Characteristics (cont.)	Updated Flash Download Time (From On-Chip Flash to SRAM) Table
			Updated Flash Program Time Table
			Updated Flash Erase Time Table
			Updated FlashBAK (from EBR to Flash) Table
			Updated Hot Socketing Specifications Table footnotes
		Pinout Information	Updated Signal Descriptions Table
June 2008	01.5	Architecture	Removed Read-Before-Write sysMEM EBR mode.
			Clarification of the operation of the secondary clock regions.
		DC and Switching Characteristics	Removed Read-Before-Write sysMEM EBR mode.
		Pinout Information	Updated DDR Banks Bonding Out per I/O Bank section of Pin Information Summary Table.
August 2008	01.6	—	Data sheet status changed from preliminary to final.
		Architecture	Clarification of the operation of the secondary clock regions.
		DC and Switching Characteristics	Removed “8W” specification from Hot Socketing Specifications table.
			Removed "8W" footnote from DC Electrical Characteristics table.
			Updated Register-to-Register Performance table.
		Ordering Information	Removed “8W” option from Part Number Description.
			Removed XP2-17 “8W” OPNs.
April 2011	01.7	DC and Switching Characteristics	Recommended Operating Conditions table, added footnote 5.
			On-Chip Flash Memory Specifications table, added footnote 1.
			BLVDS DC Conditions, corrected column title to be Z0 = 90 ohms.
			sysCONFIG Port Timing Specifications table, added footnote 1 for t_{DINIT}.
January 2012	01.8	Multiple	Added support for Lattice Diamond design software.
		Architecture	Corrected information regarding SED support.
		DC and Switching Characteristics	Added reference to ESD Performance Qualification Summary information.
May 2013	01.9	All	Updated document with new corporate logo.
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.
			Added information regarding SED support.
		DC and Switching Characteristics	Removed Input Clock Rise/Fall Time 1ns max from the sysCLOCK PLL Timing table.
		Ordering Information	Updated topside mark in Ordering Information diagram.
March 2014	02.0	Architecture	Updated Typical sysIO I/O Behavior During Power-up section. Added information on POR signal deactivation.
August 2014	02.1	Architecture	Updated Typical sysIO I/O Behavior During Power-up section. Described user I/Os during power up and before FPGA core logic is active.
September 2014	2.2	DC and Switching Characteristics	Updated Switching Test Conditions section. Re-linked missing figure.