Lattice Semiconductor Corporation - LFXP2-17E-6FT256C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

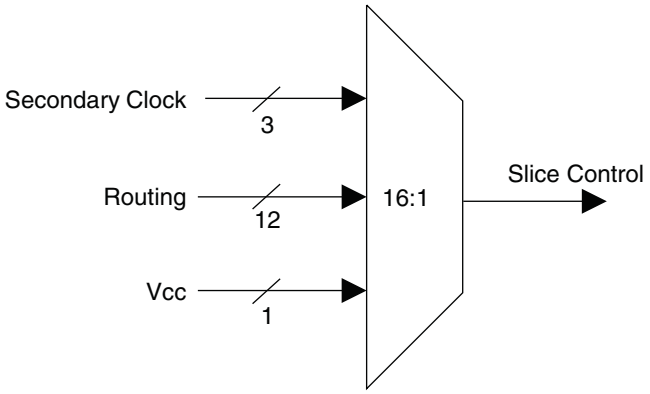
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2125
Number of Logic Elements/Cells	17000
Total RAM Bits	282624
Number of I/O	201
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-17e-6ft256c

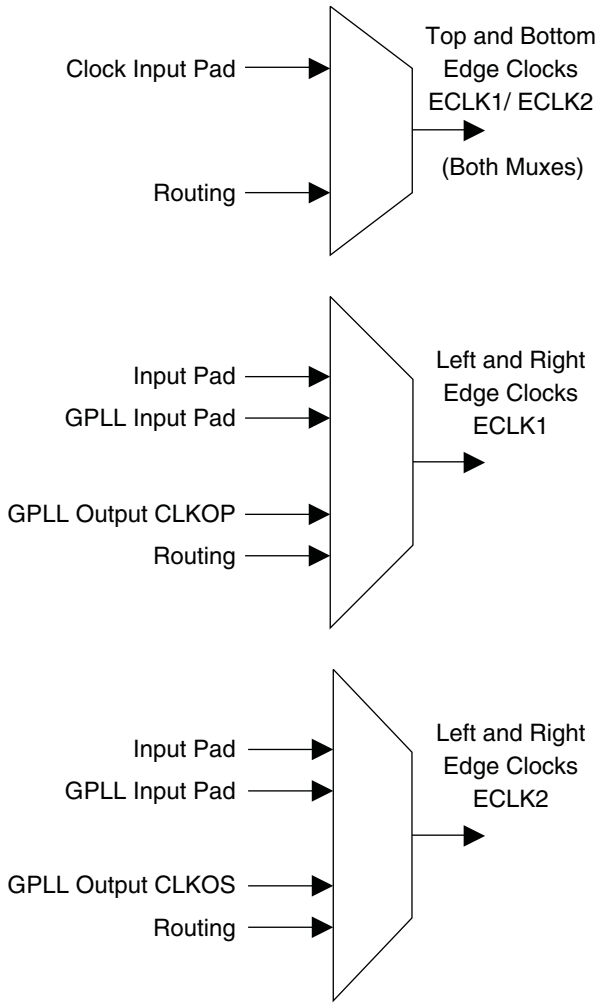
Figure 2-14. Slice0 through Slice2 Control Selection



Edge Clock Routing

LatticeXP2 devices have eight high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. Each device has two edge clocks per edge. Figure 2-15 shows the selection muxes for these clocks.

Figure 2-15. Edge Clock Mux Connections

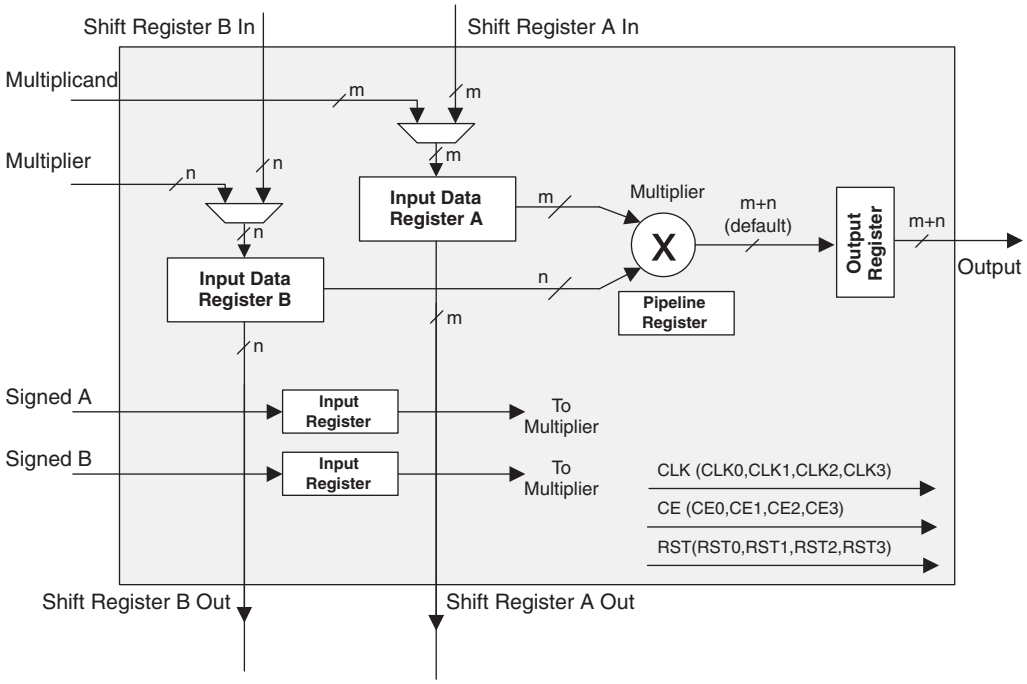


- In the ‘Signed/Unsigned’ options the operands can be switched between signed and unsigned on every cycle.
- In the ‘Add/Sub’ option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-20 shows the MULT sysDSP element.

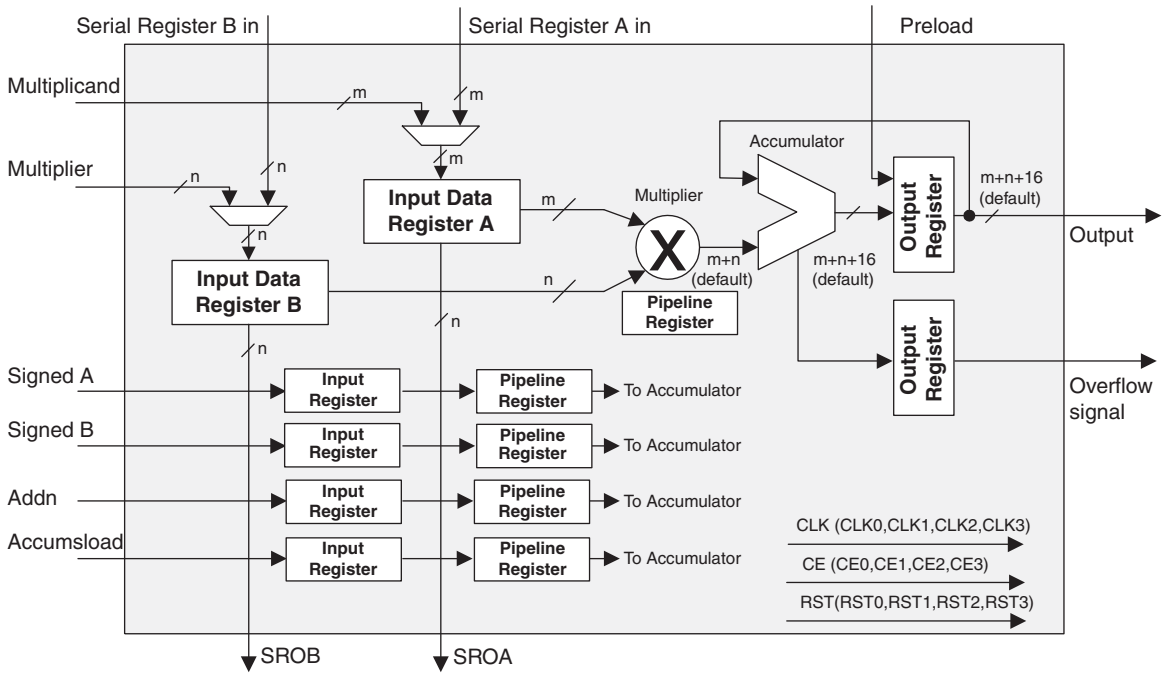
Figure 2-20. MULT sysDSP Element



MAC sysDSP Element

In this case, the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers but the output register is always enabled. The output register is used to store the accumulated value. The Accumulators in the DSP blocks in LatticeXP2 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-21 shows the MAC sysDSP element.

Figure 2-21. MAC sysDSP



shows the diagram using this gearbox function. For more information on this topic, see TN1138, LatticeXP2 High Speed I/O Interface.

Figure 2-27. Output and Tristate Block

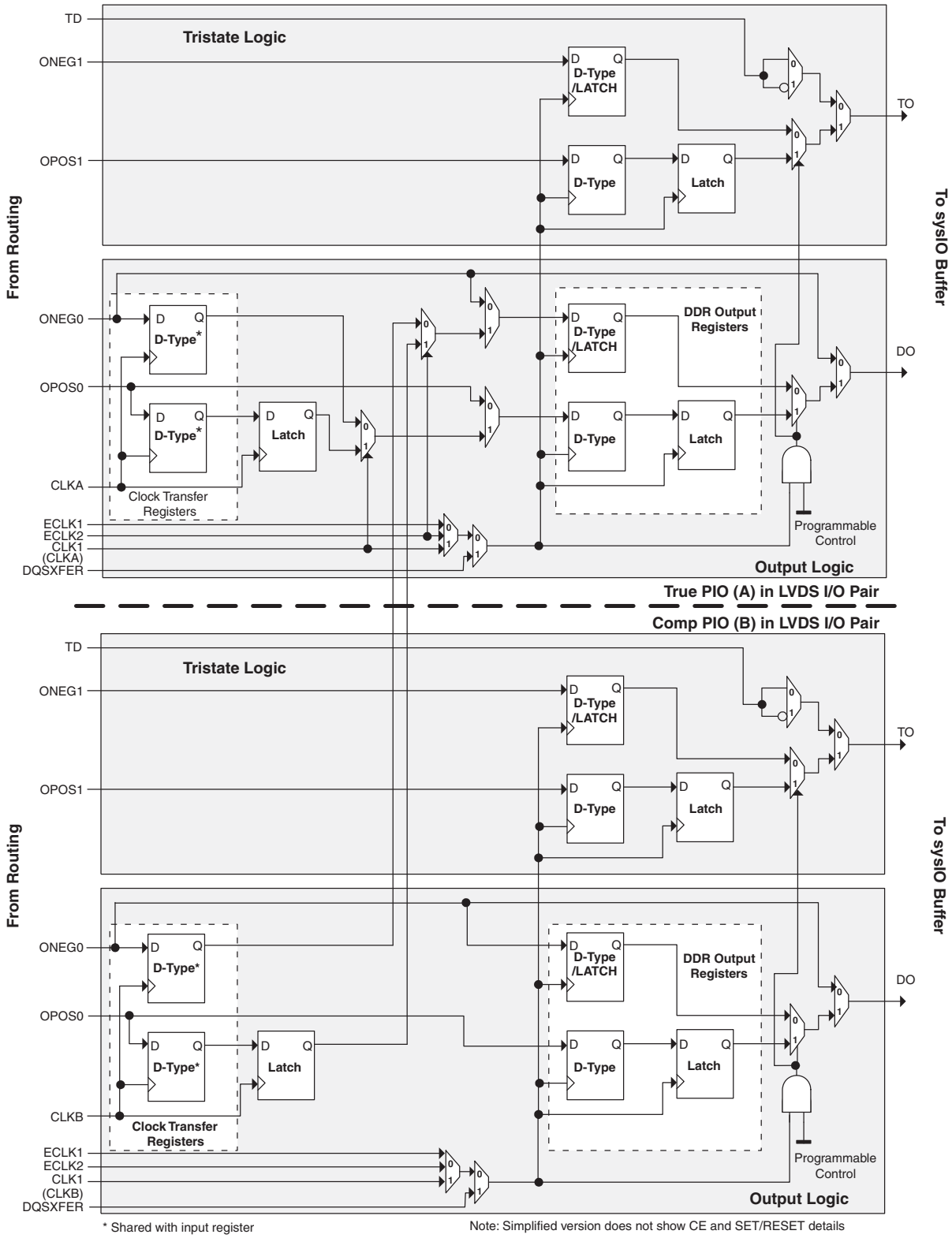


Figure 2-28. DQS Input Routing (Left and Right)

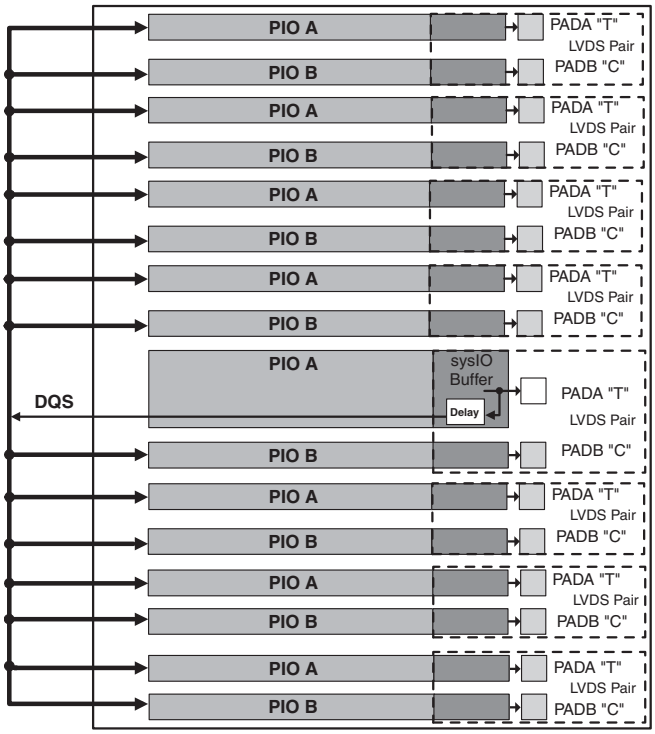
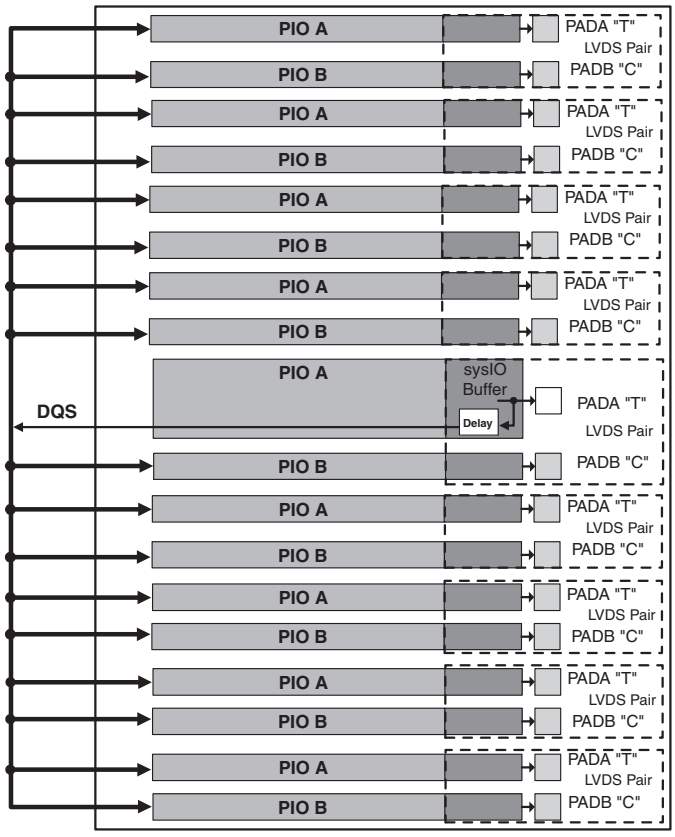


Figure 2-29. DQS Input Routing (Top and Bottom)



DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock, referred to as DQS, is not free-running, and this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only, as shown in Figure 2-30) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figure 2-30 and Figure 2-31 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of 6-bit bus calibration signals from two dedicated DLLs (DDR_DLL) on opposite sides of the device. Each DLL compensates DQS delays in its half of the device as shown in Figure 2-30. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

Figure 2-30. Edge Clock, DLL Calibration and DQS Local Bus Distribution

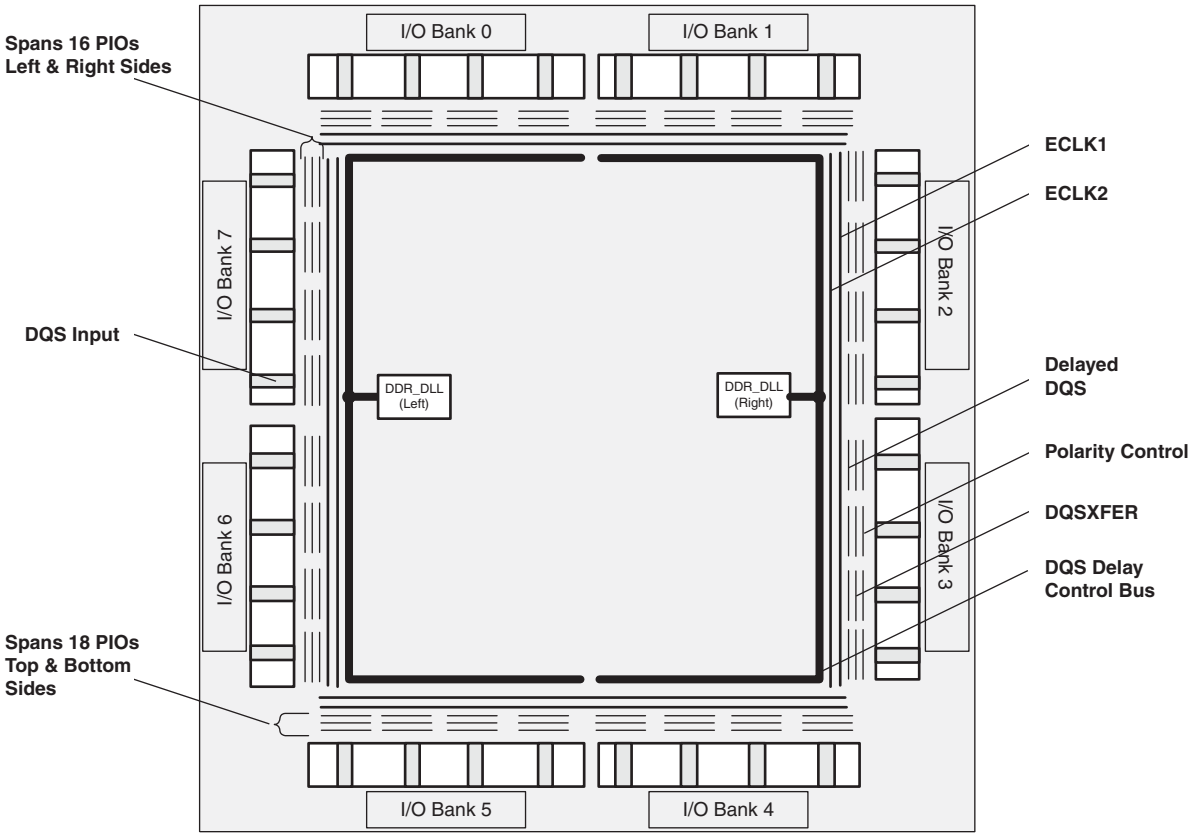


Table 2-13. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVCMOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVCMOS25	4mA, 8mA, 12mA, 16mA, 20mA	2.5
LVCMOS18	4mA, 8mA, 12mA, 16mA	1.8
LVCMOS15	4mA, 8mA	1.5
LVCMOS12	2mA, 6mA	1.2
LVCMOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II	N/A	1.8
HSTL15 Class I	N/A	1.5
SSTL33 Class I, II	N/A	3.3
SSTL25 Class I, II	N/A	2.5
SSTL18 Class I, II	N/A	1.8
Differential Interfaces		
Differential SSTL33, Class I, II	N/A	3.3
Differential SSTL25, Class I, II	N/A	2.5
Differential SSTL18, Class I, II	N/A	1.8
Differential HSTL18, Class I, II	N/A	1.8
Differential HSTL15, Class I	N/A	1.5
LVDS[1, 2]	N/A	2.5
MLVDS[1]	N/A	2.5
BLVDS[1]	N/A	2.5
LVPECL[1]	N/A	3.3
RSDS[1]	N/A	2.5
LVCMOS33D[1]	4mA, 8mA, 12mA, 16mA, 20mA	3.3

1. Emulated with external resistors.
2. On the left and right edges, LVDS outputs are supported with a dedicated differential output driver on 50% of the I/Os. This solution does not require external resistors at the driver.

Hot Socketing

LatticeXP2 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the LatticeXP2 ideal for many multiple power supply and hot-swap applications.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeXP2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in

Density Shifting

The LatticeXP2 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

sysIO Recommended Operating Conditions

Over Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS33[2]	3.135	3.3	3.465	—	—	—
LVCMOS25[2]	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12[2]	1.14	1.2	1.26	—	—	—
LVTTL33[2]	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
SSTL18_I[2], SSTL18_II[2]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I[2], SSTL25_II[2]	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I[2], SSTL33_II[2]	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I[2]	1.425	1.5	1.575	0.68	0.75	0.9
HSTL18_I[2], HSTL18_II[2]	1.71	1.8	1.89	0.816	0.9	1.08
LVDS25[2]	2.375	2.5	2.625	—	—	—
MLVDS25[1]	2.375	2.5	2.625	—	—	—
LVPECL33[1, 2]	3.135	3.3	3.465	—	—	—
BLVDS25[1, 2]	2.375	2.5	2.625	—	—	—
RSDS[1, 2]	2.375	2.5	2.625	—	—	—
SSTL18D_I[2], SSTL18D_II[2]	1.71	1.8	1.89	—	—	—
SSTL25D_ I[2], SSTL25D_II[2]	2.375	2.5	2.625	—	—	—
SSTL33D_ I[2], SSTL33D_ II[2]	3.135	3.3	3.465	—	—	—
HSTL15D_ I[2]	1.425	1.5	1.575	—	—	—
HSTL18D_ I[2], HSTL18D_ II[2]	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. Input on this standard does not depend on the value of V_{CCIO}.

sysIO Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage		0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	+/-10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9V	1.03	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SA}	Output Short Circuit Current	V_{OD} = 0V Driver Outputs Shorted to Ground	—	—	24	mA
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V Driver Outputs Shorted to Each Other	—	—	12	mA

Differential HSTL and SSTL

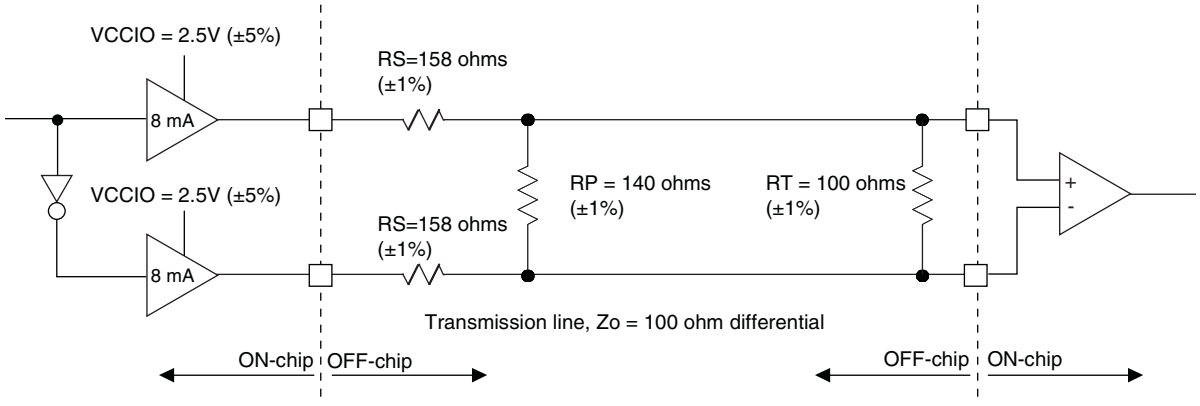
Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see details in additional technical notes listed at the end of this data sheet.

LVDS25E

The top and bottom sides of LatticeXP2 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example



LatticeXP2 External Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HE}	Clock to Data Hold - PIO Input Register	XP2-5	1.00	—	1.30	—	1.60	—	ns
		XP2-8	1.00	—	1.30	—	1.60	—	ns
		XP2-17	1.00	—	1.30	—	1.60	—	ns
		XP2-30	1.20	—	1.60	—	1.90	—	ns
		XP2-40	1.20	—	1.60	—	1.90	—	ns
t_{SU_DELE}	Clock to Data Setup - PIO Input Register with Data Input Delay	XP2-5	1.00	—	1.30	—	1.60	—	ns
		XP2-8	1.00	—	1.30	—	1.60	—	ns
		XP2-17	1.00	—	1.30	—	1.60	—	ns
		XP2-30	1.20	—	1.60	—	1.90	—	ns
		XP2-40	1.20	—	1.60	—	1.90	—	ns
t_{H_DELE}	Clock to Data Hold - PIO Input Register with Input Data Delay	XP2-5	0.00	—	0.00	—	0.00	—	ns
		XP2-8	0.00	—	0.00	—	0.00	—	ns
		XP2-17	0.00	—	0.00	—	0.00	—	ns
		XP2-30	0.00	—	0.00	—	0.00	—	ns
		XP2-40	0.00	—	0.00	—	0.00	—	ns
f_{MAX_IOE}	Clock Frequency of I/O and PFU Register	XP2	—	420	—	357	—	311	MHz
General I/O Pin Parameters (using Primary Clock with PLL)[1]									
t_{COPLL}	Clock to Output - PIO Output Register	XP2-5	—	3.00	—	3.30	—	3.70	ns
		XP2-8	—	3.00	—	3.30	—	3.70	ns
		XP2-17	—	3.00	—	3.30	—	3.70	ns
		XP2-30	—	3.00	—	3.30	—	3.70	ns
		XP2-40	—	3.00	—	3.30	—	3.70	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	XP2-5	1.00	—	1.20	—	1.40	—	ns
		XP2-8	1.00	—	1.20	—	1.40	—	ns
		XP2-17	1.00	—	1.20	—	1.40	—	ns
		XP2-30	1.00	—	1.20	—	1.40	—	ns
		XP2-40	1.00	—	1.20	—	1.40	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	XP2-5	0.90	—	1.10	—	1.30	—	ns
		XP2-8	0.90	—	1.10	—	1.30	—	ns
		XP2-17	0.90	—	1.10	—	1.30	—	ns
		XP2-30	1.00	—	1.20	—	1.40	—	ns
		XP2-40	1.00	—	1.20	—	1.40	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	XP2-5	1.90	—	2.10	—	2.30	—	ns
		XP2-8	1.90	—	2.10	—	2.30	—	ns
		XP2-17	1.90	—	2.10	—	2.30	—	ns
		XP2-30	2.00	—	2.20	—	2.40	—	ns
		XP2-40	2.00	—	2.20	—	2.40	—	ns

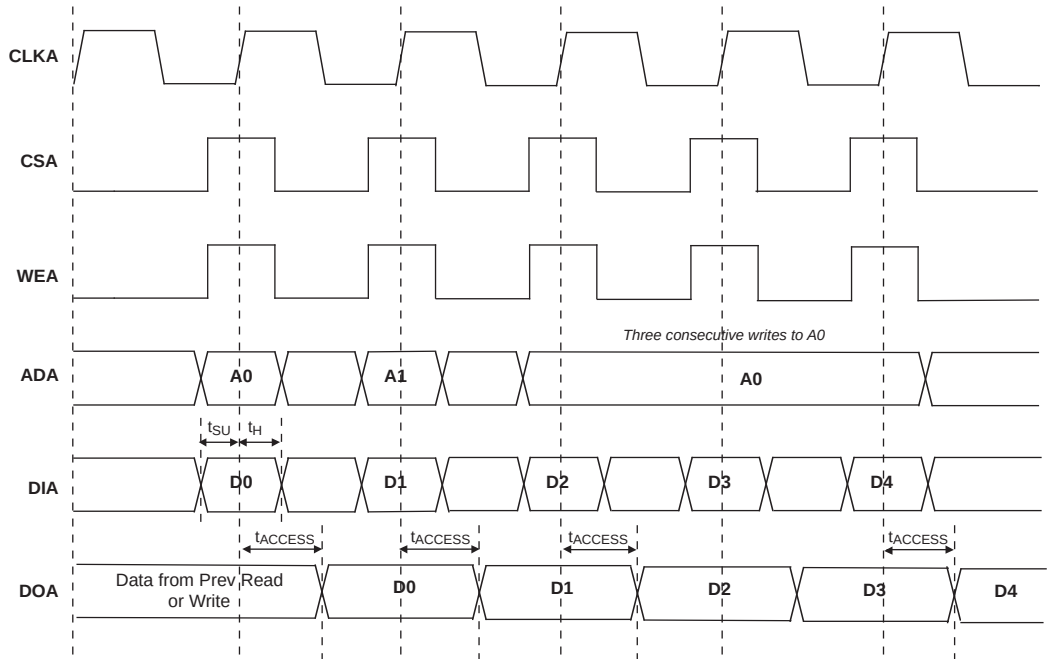
LatticeXP2 Internal Switching Characteristics[1] (Continued)

Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HP_DSP}	Pipeline Register Hold Time	-0.787	—	-0.890	—	-0.994	—	ns
t_{SUO_DSP}	Output Register Setup Time	4.896	—	5.413	—	5.931	—	ns
t_{HO_DSP}	Output Register Hold Time	-1.439	—	-1.604	—	-1.770	—	ns
t_{COI_DSP}[3]	Input Register Clock to Output Time	—	4.513	—	4.947	—	5.382	ns
t_{COP_DSP}[3]	Pipeline Register Clock to Output Time	—	2.153	—	2.272	—	2.391	ns
t_{COO_DSP}[3]	Output Register Clock to Output Time	—	0.569	—	0.600	—	0.631	ns
$t_{SUADSUB}$	AdSub Input Register Setup Time	-0.270	—	-0.298	—	-0.327	—	ns
t_{HADSUB}	AdSub Input Register Hold Time	0.306	—	0.338	—	0.371	—	ns

1. Internal parameters are characterized, but not tested on every device.
2. RST resets VCO and all counters in PLL.
3. These parameters include the Adder Subtractor block in the path.

Figure 3-8. Write Through (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

LatticeXP2 Family Timing Adders[1, 2, 3, 4]

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
Input Adjusters					
LVDS25	LVDS	-0.26	-0.11	0.04	ns
BLVDS25	BLVDS	-0.26	-0.11	0.04	ns
MLVDS	LVDS	-0.26	-0.11	0.04	ns
RSDS	RSDS	-0.26	-0.11	0.04	ns
LVPECL33	LVPECL	-0.26	-0.11	0.04	ns
HSTL18_I	HSTL_18 class I	-0.23	-0.08	0.07	ns
HSTL18_II	HSTL_18 class II	-0.23	-0.08	0.07	ns
HSTL18D_I	Differential HSTL 18 class I	-0.28	-0.13	0.02	ns
HSTL18D_II	Differential HSTL 18 class II	-0.28	-0.13	0.02	ns
HSTL15_I	HSTL_15 class I	-0.23	-0.09	0.06	ns
HSTL15D_I	Differential HSTL 15 class I	-0.28	-0.13	0.01	ns
SSTL33_I	SSTL_3 class I	-0.20	-0.04	0.12	ns
SSTL33_II	SSTL_3 class II	-0.20	-0.04	0.12	ns
SSTL33D_I	Differential SSTL_3 class I	-0.27	-0.11	0.04	ns
SSTL33D_II	Differential SSTL_3 class II	-0.27	-0.11	0.04	ns
SSTL25_I	SSTL_2 class I	-0.21	-0.06	0.10	ns
SSTL25_II	SSTL_2 class II	-0.21	-0.06	0.10	ns
SSTL25D_I	Differential SSTL_2 class I	-0.27	-0.12	0.03	ns
SSTL25D_II	Differential SSTL_2 class II	-0.27	-0.12	0.03	ns
SSTL18_I	SSTL_18 class I	-0.23	-0.08	0.07	ns
SSTL18_II	SSTL_18 class II	-0.23	-0.08	0.07	ns
SSTL18D_I	Differential SSTL_18 class I	-0.28	-0.13	0.02	ns
SSTL18D_II	Differential SSTL_18 class II	-0.28	-0.13	0.02	ns
LVTTL33	LVTTL	-0.09	0.05	0.18	ns
LVCMOS33	LVCMOS 3.3	-0.09	0.05	0.18	ns
LVCMOS25	LVCMOS 2.5	0.00	0.00	0.00	ns
LVCMOS18	LVCMOS 1.8	-0.23	-0.07	0.09	ns
LVCMOS15	LVCMOS 1.5	-0.20	-0.02	0.16	ns
LVCMOS12	LVCMOS 1.2	-0.35	-0.20	-0.04	ns
PCI33	3.3V PCI	-0.09	0.05	0.18	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E[5]	-0.25	0.02	0.30	ns
LVDS25	LVDS 2.5	-0.25	0.02	0.30	ns
BLVDS25	BLVDS 2.5	-0.28	0.00	0.28	ns
MLVDS	MLVDS 2.5[5]	-0.28	0.00	0.28	ns
RSDS	RSDS 2.5[5]	-0.25	0.02	0.30	ns
LVPECL33	LVPECL 3.3[5]	-0.37	-0.10	0.18	ns
HSTL18_I	HSTL_18 class I 8mA drive	-0.17	0.13	0.43	ns
HSTL18_II	HSTL_18 class II	-0.29	0.00	0.29	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	-0.17	0.13	0.43	ns
HSTL18D_II	Differential HSTL 18 class II	-0.29	0.00	0.29	ns

LatticeXP2 Family Timing Adders[1, 2, 3, 4] (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, slow slew rate	1.05	1.43	1.81	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, slow slew rate	0.78	1.15	1.52	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, slow slew rate	0.59	0.96	1.33	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, slow slew rate	0.81	1.18	1.55	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, slow slew rate	0.61	0.98	1.35	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, slow slew rate	1.01	1.38	1.75	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, slow slew rate	0.72	1.08	1.45	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, slow slew rate	0.53	0.90	1.26	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, slow slew rate	0.74	1.11	1.48	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, slow slew rate	0.96	1.33	1.71	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, slow slew rate	-0.53	-0.26	0.00	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, slow slew rate	0.90	1.27	1.65	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, slow slew rate	-0.55	-0.29	-0.02	ns
PCI33	3.3V PCI	-0.29	-0.01	0.26	ns

1. Timing Adders are characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. The base parameters used with these timing adders to calculate timing are listed in the LatticeXP2 Internal Switching Characteristics table under PIO Input/Output Timing.
5. These timing adders are measured with the recommended resistor values.

Pin Information Summary

Pin Type		XP2-5				XP2-8				XP2-17			XP2-30			XP2-40	
		132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
Single Ended User I/O		86	100	146	172	86	100	146	201	146	201	358	201	363	472	363	540
Differential Pair User I/O	Normal	35	39	57	66	35	39	57	77	57	77	135	77	137	180	137	204
	Highspeed	8	11	16	20	8	11	16	23	16	23	44	23	44	56	44	66
Configuration	TAP	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
	Muxed	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9
	Dedicated	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Non Configuration	Muxed	5	5	7	7	7	7	9	9	11	11	21	7	11	13	11	13
	Dedicated	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Vcc		6	4	9	6	6	4	9	6	9	6	16	6	16	20	16	20
Vccaux		4	4	4	4	4	4	4	4	4	4	8	4	8	8	8	8
VCCPLL		2	2	2	-	2	2	2	-	4	-	-	-	-	-	-	-
VCCIO	Bank0	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
	Bank1	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank2	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
	Bank3	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank4	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank5	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
	Bank6	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank7	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
GND, GND0-GND7		15	15	20	20	15	15	22	20	22	20	56	20	56	64	56	64
NC		-	-	4	31	-	-	2	2	-	2	7	2	2	69	2	1
Single Ended/ Differential I/O per Bank	Bank0	18/9	20/10	20/10	26/13	18/9	20/10	20/10	28/14	20/10	28/14	52/26	28/14	52/26	70/35	52/26	70/35
	Bank1	4/2	6/3	18/9	18/9	4/2	6/3	18/9	22/11	18/9	22/11	36/18	22/11	36/18	54/27	36/18	70/35
	Bank2	16/8	18/9	18/9	22/11	16/8	18/9	18/9	26/13	18/9	26/13	46/23	26/13	46/23	56/28	46/23	64/32
	Bank3	4/2	4/2	16/8	20/10	4/2	4/2	16/8	24/12	16/8	24/12	44/22	24/12	46/23	56/28	46/23	66/33
	Bank4	8/4	8/4	18/9	18/9	8/4	8/4	18/9	26/13	18/9	26/13	36/18	26/13	38/19	54/27	38/19	70/35
	Bank5	14/7	18/9	20/10	24/12	14/7	18/9	20/10	24/12	20/10	24/12	52/26	24/12	53/26	70/35	53/26	70/35
	Bank6	6/3	8/4	18/9	22/11	6/3	8/4	18/9	27/13	18/9	27/13	46/23	27/13	46/23	56/28	46/23	66/33
	Bank7	16/8	18/9	18/9	22/11	16/8	18/9	18/9	24/12	18/9	24/12	46/23	24/12	46/23	56/28	46/23	64/32
True LVDS Pairs Bonding Out per Bank	Bank0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank2	3	4	4	5	3	4	4	6	4	6	11	6	11	14	11	16
	Bank3	1	1	4	5	1	1	4	6	4	6	11	6	11	14	11	17
	Bank4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank6	1	2	4	5	1	2	4	6	4	6	11	6	11	14	11	17
	Bank7	3	4	4	5	3	4	4	5	4	5	11	5	11	14	11	16
DDR Banks Bonding Out per I/O Bank[1]	Bank0	1	1	1	1	1	1	1	1	1	1	3	1	2	4	2	4
	Bank1	0	0	1	1	0	0	1	1	1	1	2	1	2	3	2	4
	Bank2	1	1	1	1	1	1	1	1	1	1	2	1	3	3	3	4
	Bank3	0	0	1	1	0	0	1	1	1	1	2	1	3	3	3	4
	Bank4	0	0	1	1	0	0	1	1	1	1	2	1	2	3	2	4
	Bank5	1	1	1	1	1	1	1	1	1	1	3	1	2	4	2	4
	Bank6	0	0	1	1	0	0	1	1	1	1	2	1	3	3	3	4
	Bank7	1	1	1	1	1	1	1	1	1	1	2	1	3	3	3	4

Pin Information Summary (Cont.)

Pin Type		XP2-5				XP2-8				XP2-17			XP2-30			XP2-40	
		132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
PCI capable I/Os Bonding Out per Bank	Bank0	18	20	20	26	18	20	20	28	20	28	52	28	52	70	52	70
	Bank1	4	6	18	18	4	6	18	22	18	22	36	22	36	54	36	70
	Bank2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank4	8	8	18	18	8	8	18	26	18	26	36	26	38	54	38	70
	Bank5	14	18	20	24	14	18	20	24	20	24	52	24	53	70	53	70
	Bank6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

Logic Signal Connections

Package pinout information can be found under “Data Sheets” on the LatticeXP2 product page of the Lattice website a www.latticesemi.com/products/fpga/xp2 and in the Lattice Diamond design software.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Lattice Thermal Management document to find the device/package specific thermal values.

For Further Information

- TN1139, Power Estimation and Management for LatticeXP2 Devices
- Power Calculator tool is included with the Lattice Diamond design tool or as a standalone download from www.latticesemi.com/products/designsoftware

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-30E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	30
LFXP2-30E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	30
LFXP2-30E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	30
LFXP2-30E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	30
LFXP2-30E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	30
LFXP2-30E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	30
LFXP2-30E-5FN672C	1.2V	-5	Lead-Free fpBGA	672	COM	30
LFXP2-30E-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	30
LFXP2-30E-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	30

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	40
LFXP2-40E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	40
LFXP2-40E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	40
LFXP2-40E-5FN672C	1.2V	-5	Lead-Free fpBGA	672	COM	40
LFXP2-40E-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	40
LFXP2-40E-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	40

Industrial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5MN132I	1.2V	-5	Lead-Free csBGA	132	IND	5
LFXP2-5E-6MN132I	1.2V	-6	Lead-Free csBGA	132	IND	5
LFXP2-5E-5TN144I	1.2V	-5	Lead-Free TQFP	144	IND	5
LFXP2-5E-6TN144I	1.2V	-6	Lead-Free TQFP	144	IND	5
LFXP2-5E-5QN208I	1.2V	-5	Lead-Free PQFP	208	IND	5
LFXP2-5E-6QN208I	1.2V	-6	Lead-Free PQFP	208	IND	5
LFXP2-5E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	5
LFXP2-5E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5MN132I	1.2V	-5	Lead-Free csBGA	132	IND	8
LFXP2-8E-6MN132I	1.2V	-6	Lead-Free csBGA	132	IND	8
LFXP2-8E-5TN144I	1.2V	-5	Lead-Free TQFP	144	IND	8
LFXP2-8E-6TN144I	1.2V	-6	Lead-Free TQFP	144	IND	8
LFXP2-8E-5QN208I	1.2V	-5	Lead-Free PQFP	208	IND	8
LFXP2-8E-6QN208I	1.2V	-6	Lead-Free PQFP	208	IND	8
LFXP2-8E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	8
LFXP2-8E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5F484I	1.2V	-5	fpBGA	484	IND	40
LFXP2-40E-6F484I	1.2V	-6	fpBGA	484	IND	40
LFXP2-40E-5F672I	1.2V	-5	fpBGA	672	IND	40
LFXP2-40E-6F672I	1.2V	-6	fpBGA	672	IND	40

Date	Version	Section	Change Summary
April 2008 (cont.)	01.4 (cont.)	DC and Switching Characteristics (cont.)	Updated Flash Download Time (From On-Chip Flash to SRAM) Table
			Updated Flash Program Time Table
			Updated Flash Erase Time Table
			Updated FlashBAK (from EBR to Flash) Table
			Updated Hot Socketing Specifications Table footnotes
		Pinout Information	Updated Signal Descriptions Table
June 2008	01.5	Architecture	Removed Read-Before-Write sysMEM EBR mode.
			Clarification of the operation of the secondary clock regions.
		DC and Switching Characteristics	Removed Read-Before-Write sysMEM EBR mode.
		Pinout Information	Updated DDR Banks Bonding Out per I/O Bank section of Pin Information Summary Table.
August 2008	01.6	—	Data sheet status changed from preliminary to final.
		Architecture	Clarification of the operation of the secondary clock regions.
		DC and Switching Characteristics	Removed “8W” specification from Hot Socketing Specifications table.
			Removed "8W" footnote from DC Electrical Characteristics table.
			Updated Register-to-Register Performance table.
		Ordering Information	Removed “8W” option from Part Number Description.
			Removed XP2-17 “8W” OPNs.
April 2011	01.7	DC and Switching Characteristics	Recommended Operating Conditions table, added footnote 5.
			On-Chip Flash Memory Specifications table, added footnote 1.
			BLVDS DC Conditions, corrected column title to be Z0 = 90 ohms.
			sysCONFIG Port Timing Specifications table, added footnote 1 for t_{DINIT}.
January 2012	01.8	Multiple	Added support for Lattice Diamond design software.
		Architecture	Corrected information regarding SED support.
		DC and Switching Characteristics	Added reference to ESD Performance Qualification Summary information.
May 2013	01.9	All	Updated document with new corporate logo.
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.
			Added information regarding SED support.
		DC and Switching Characteristics	Removed Input Clock Rise/Fall Time 1ns max from the sysCLOCK PLL Timing table.
		Ordering Information	Updated topside mark in Ordering Information diagram.
March 2014	02.0	Architecture	Updated Typical sysIO I/O Behavior During Power-up section. Added information on POR signal deactivation.
August 2014	02.1	Architecture	Updated Typical sysIO I/O Behavior During Power-up section. Described user I/Os during power up and before FPGA core logic is active.
September 2014	2.2	DC and Switching Characteristics	Updated Switching Test Conditions section. Re-linked missing figure.