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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	2125
Number of Logic Elements/Cells	17000
Total RAM Bits	282624
Number of I/O	201
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-17e-6ft256i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



# Introduction

LatticeXP2 devices combine a Look-up Table (LUT) based FPGA fabric with non-volatile Flash cells in an architecture referred to as flexiFLASH.

The flexiFLASH approach provides benefits including instant-on, infinite reconfigurability, on chip storage with FlashBAK embedded block memory and Serial TAG memory and design security. The parts also support Live Update technology with TransFR, 128-bit AES Encryption and Dual-boot technologies.

The LatticeXP2 FPGA fabric was optimized for the new technology from the outset with high performance and low cost in mind. LatticeXP2 devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support and enhanced sysDSP blocks.

Lattice Diamond<sup>®</sup> design software allows large and complex designs to be efficiently implemented using the LatticeXP2 family of FPGA devices. Synthesis library support for LatticeXP2 is available for popular logic synthesis tools. The Diamond software uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeXP2 device. The Diamond tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed Intellectual Property (IP) LatticeCORE<sup>™</sup> modules for the LatticeXP2 family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.



# Routing

There are many resources provided in the LatticeXP2 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) or x6 (spans seven PFU) connections. The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered to allow both short and long connections routing between PFUs.

The LatticeXP2 family has an enhanced routing architecture to produce a compact design. The Diamond design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

# sysCLOCK Phase Locked Loops (PLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The LatticeXP2 family supports between two and four full featured General Purpose PLLs (GPLL). The architecture of the GPLL is shown in Figure 2-4.

CLKI, the PLL reference frequency, is provided either from the pin or from routing; it feeds into the Input Clock Divider block. CLKFB, the feedback signal, is generated from CLKOP (the primary clock output) or from a user clock pin/logic. CLKFB feeds into the Feedback Divider and is used to multiply the reference frequency.

Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. The phase and frequency of the VCO are determined from the input path and feedback signals. A LOCK signal is generated by the VCO to indicate that the VCO is locked with the input clock signal.

The output of the VCO feeds into the CLKOP Divider, a post-scalar divider. The duty cycle of the CLKOP Divider output can be fine tuned using the Duty Trim block, which creates the CLKOP signal. By allowing the VCO to operate at higher frequencies than CLKOP, the frequency range of the GPLL is expanded. The output of the CLKOP Divider is passed through the CLKOK Divider, a secondary clock divider, to generate lower frequencies for the CLKOK output. For applications that require even lower frequencies, the CLKOP signal is passed through a divide-by-three divider to produce the CLKOK2 output. The CLKOK2 output is provided for applications that use source synchronous logic. The Phase/Duty Cycle/Duty Trim block is used to adjust the phase and duty cycle of the CLKOP Divider output to generate the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The clock outputs from the GPLL; CLKOP, CLKOK, CLKOK2 and CLKOS, are fed to the clock distribution network.

For further information on the GPLL please see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide.



Figure 2-5. Clock Divider Connections



# **Clock Distribution Network**

LatticeXP2 devices have eight quadrant-based primary clocks and between six and eight flexible region-based secondary clocks/control signals. Two high performance edge clocks are available on each edge of the device to support high speed interfaces. The clock inputs are selected from external I/Os, the sysCLOCK PLLs, or routing. Clock inputs are fed throughout the chip via the primary, secondary and edge clock networks.

### **Primary Clock Sources**

LatticeXP2 devices derive primary clocks from four sources: PLL outputs, CLKDIV outputs, dedicated clock inputs and routing. LatticeXP2 devices have two to four sysCLOCK PLLs, located in the four corners of the device. There are eight dedicated clock inputs, two on each side of the device. Figure 2-6 shows the primary clock sources.



For further information on the sysMEM EBR block, please see TN1137, LatticeXP2 Memory Usage Guide.

### **EBR Asynchronous Reset**

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the low-to-high transition of the reset signal, as shown in Figure 2-18. The GSR input to the EBR is always asynchronous.



Reset	
Clock	
Clock —————— Enable	

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of 1/f<sub>MAX</sub> (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

## sysDSP™ Block

The LatticeXP2 family provides a sysDSP block making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications include Bit Correlators, Fast Fourier Transform (FFT) functions, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/ Decoder and Convolutional Encoder/Decoder. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

### sysDSP Block Approach Compare to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeXP2 family, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-19 compares the fully serial and the mixed parallel and serial implementations.



### **MULTADDSUB sysDSP Element**

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. The user can enable the input, output and pipeline registers. Figure 2-22 shows the MULTADDSUB sysDSP element.

#### Figure 2-22. MULTADDSUB





register. Similarly, CE and RST are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

### Signed and Unsigned with Different Widths

The DSP block supports other widths, in addition to x9, x18 and x36 widths, of signed and unsigned multipliers. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2-7 provides an example of this.

#### Table 2-7. Sign Extension Example

Number	Unsigned	Unsigned 9-bit	Unsigned 18-bit	Signed	Two's Complement Signed 9 Bits	Two's Complement Signed 18 Bits
+5	0101	000000101	00000000000000101	0101	00000101	00000000000000101
-6	N/A	N/A	N/A	1010	111111010	1111111111111111010

### **OVERFLOW Flag from MAC**

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. "Roll-over" occurs and an overflow signal is indicated when any of the following is true: two unsigned numbers are added and the result is a smaller number than the accumulator, two positive numbers are added with a negative sum or two negative numbers are added with a positive sum. Note that when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions for the overflow signal for signed and unsigned operands are listed in Figure 2-24.

#### Figure 2-24. Accumulator Overflow/Underflow





#### Figure 2-31. DQS Local Bus



\*DQSXFERDEL shifts ECLK1 by 90% and is not associated with a particular PIO.

## **Polarity Control Logic**

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeXP2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block and requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.



LatticeXP2 devices contain two types of sysIO buffer pairs.

#### 1. Top and Bottom (Banks 0, 1, 4 and 5) sysIO Buffer Pairs (Single-Ended Outputs Only)

The sysIO buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Only the I/Os on the top and bottom banks have programmable PCI clamps.

2. Left and Right (Banks 2, 3, 6 and 7) sysIO Buffer Pairs (50% Differential and 100% Single-Ended Outputs) The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp pad is associated with the negative side of the differential I/O.

LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

### Typical sysIO I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when  $V_{CC, V} C_{CCONFIG} (V_{CCIO7})$  and  $V_{CCAUX}$  have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other  $V_{CCIO}$  banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. During power up and before the FPGA core logic becomes active, all user I/Os will be high-impedance with weak pull-up. Please refer to TN1136, <u>LatticeXP2 sysIO</u> Usage Guide for additional information.

The V<sub>CC</sub> and V<sub>CCAUX</sub> supply the power to the FPGA core fabric, whereas the V<sub>CCIO</sub> supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V<sub>CCIO</sub> supplies should be powered-up before or together with the V<sub>CC</sub> and V<sub>CCAUX</sub> supplies.

### Supported sysIO Standards

The LatticeXP2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8V, 2.5V and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, MLVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-12 and 2-13 show the I/O standards (together with their supply and reference voltages) supported by LatticeXP2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1136, LatticeXP2 sysIO Usage Guide.



### Table 2-12. Supported Input Standards

Input Standard	V <sub>REF</sub> (Nom.)	V <sub>CCIO</sub> <sup>1</sup> (Nom.)						
Single Ended Interfaces	Single Ended Interfaces							
LVTTL	—	—						
LVCMOS33	_	_						
LVCMOS25	—	—						
LVCMOS18	—	1.8						
LVCMOS15	_	1.5						
LVCMOS12	_	—						
PCI33	—	—						
HSTL18 Class I, II	0.9	_						
HSTL15 Class I	0.75	—						
SSTL33 Class I, II	1.5	—						
SSTL25 Class I, II	1.25	_						
SSTL18 Class I, II	0.9	—						
Differential Interfaces		-						
Differential SSTL18 Class I, II	—	—						
Differential SSTL25 Class I, II	—	—						
Differential SSTL33 Class I, II	—	—						
Differential HSTL15 Class I	—	—						
Differential HSTL18 Class I, II	—	—						
LVDS, MLVDS, LVPECL, BLVDS, RSDS	—	_						

1. When not specified,  $V_{CCIO}$  can be set anywhere in the valid operating range (page 3-1).



- 1. Unlocked
- 2. Key Locked Presenting the key through the programming interface allows the device to be unlocked.
- 3. Permanently Locked The device is permanently locked.

To further complement the security of the device a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash portion of the device.

### Serial TAG Memory

LatticeXP2 devices offer 0.6 to 3.3kbits of Flash memory in the form of Serial TAG memory. The TAG memory is an area of the on-chip Flash that can be used for non-volatile storage including electronic ID codes, version codes, date stamps, asset IDs and calibration settings. A block diagram of the TAG memory is shown in Figure 2-34. The TAG memory is accessed in the same way as external SPI Flash and it can be read or programmed either through JTAG, an external Slave SPI Port, or directly from FPGA logic. To read the TAG memory, a start address is specified and the entire TAG memory contents are read sequentially in a first-in-first-out manner. The TAG memory is always accessible regardless of the device security settings. For more information, see TN1137, LatticeXP2 Memory Usage Guide and TN1141, LatticeXP2 sysCONFIG Usage Guide.

#### Figure 2-34. Serial TAG Memory Diagram



### Live Update Technology

Many applications require field updates of the FPGA. LatticeXP2 devices provide three features that enable this configuration to be done in a secure and failsafe manner while minimizing impact on system operation.

#### 1. **Decryption Support**

LatticeXP2 devices provide on-chip, non-volatile key storage to support decryption of a 128-bit AES encrypted bitstream, securing designs and deterring design piracy.

#### 2. TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. For more information please see TN1087, <u>Minimizing System Interruption During Configuration</u>. Using TransFR Technology.

#### 3. Dual Boot Image Support

Dual boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeXP2 can be re-booted from this new configuration file. If there is a problem such as corrupt data during download or incorrect version number with this new boot image, the LatticeXP2 device can revert back to the



# LatticeXP2 Family Data Sheet DC and Switching Characteristics

#### September 2014

Data Sheet DS1009

# Absolute Maximum Ratings<sup>1, 2, 3</sup>

Supply Voltage V <sub>CC</sub>
Supply Voltage V <sub>CCAUX</sub>
Supply Voltage V <sub>CCJ</sub>
Supply Voltage V <sub>CCPLL</sub> <sup>4</sup> 0.5 to 3.75V
Output Supply Voltage V <sub>CCIO</sub> 0.5 to 3.75V
Input or I/O Tristate Voltage Applied <sup>5</sup> 0.5 to 3.75V
Storage Temperature (Ambient)65 to 150°C
Junction Temperature Under Bias (Tj)+125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

2. Compliance with the Lattice <u>Thermal Management</u> document is required.

3. All voltages referenced to GND.

4. V<sub>CCPLL</sub> only available on csBGA, PQFP and TQFP packages.

5. Overshoot and undershoot of -2V to (V<sub>IHMAX</sub> + 2) volts is permitted for a duration of <20 ns.

# **Recommended Operating Conditions**

Symbol	Parameter	Min.	Max.	Units
V <sub>CC</sub>	Core Supply Voltage	1.14	1.26	V
V <sub>CCAUX</sub> <sup>4, 5</sup>	Auxiliary Supply Voltage	3.135	3.465	V
V <sub>CCPLL</sub> <sup>1</sup>	PLL Supply Voltage	3.135	3.465	V
V <sub>CCIO</sub> <sup>2, 3, 4</sup>	I/O Driver Supply Voltage	1.14	3.465	V
V <sub>CCJ</sub> <sup>2</sup>	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
t <sub>JCOM</sub>	Junction Temperature, Commercial Operation	0	85	°C
t <sub>JIND</sub>	Junction Temperature, Industrial Operation	-40	100	°C

1.  $V_{CCPLL}$  only available on csBGA, PQFP and TQFP packages.

If V<sub>CCIO</sub> or V<sub>CCJ</sub> is set to 1.2 V, they must be connected to the same power supply as V<sub>CC</sub>. If V<sub>CCIO</sub> or V<sub>CCJ</sub> is set to 3.3V, they must be connected to the same power supply as V<sub>CCAUX</sub>.

3. See recommended voltages by I/O standard in subsequent table.

4. To ensure proper I/O behavior,  $V_{CCIO}$  must be turned off at the same time or earlier than  $V_{CCAUX}$ .

5. In fpBGA and ftBGA packages, the PLLs are connected to, and powered from, the auxiliary power supply.

# **On-Chip Flash Memory Specifications**

Symbol	Parameter	Max.	Units
Nanagaya	Flash Programming Cycles per t <sub>RETENTION</sub> <sup>1</sup>	10,000	Cycles
NPROGCYC	Flash Functional Programming Cycles	100,000	Oycles

1. The minimum data retention, t<sub>RETENTION</sub>, is 20 years.

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# Hot Socketing Specifications<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
I <sub>DK</sub>	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX.)	_	_	+/-1	mA

1. Insensitive to sequence of  $V_{CC}$ ,  $V_{CCAUX}$  and  $V_{CCIO}$ . However, assumes monotonic rise/fall rates for  $V_{CC}$ ,  $V_{CCAUX}$  and  $V_{CCIO}$ .

2.  $0 \le V_{CC} \le V_{CC}$  (MAX),  $0 \le V_{CCIO} \le V_{CCIO}$  (MAX) or  $0 \le V_{CCAUX} \le V_{CCAUX}$  (MAX).

3.  $I_{DK}$  is additive to  $I_{PU}$ ,  $I_{PW}$  or  $I_{BH}$ .

4. LVCMOS and LVTTL only.

# **ESD** Performance

Please refer to the <u>LatticeXP2 Product Family Qualification Summary</u> for complete qualification data, including ESD performance.

# **DC Electrical Characteristics**

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
I I 1	Input or I/O Low Leakage	$0 \le V_{IN} \le V_{CCIO}$	—		10	μA
ηΓ, ηΗ		$V_{CCIO} \le V_{IN} \le V_{IH}$ (MAX)	—	_	150	μΑ
I <sub>PU</sub>	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7 \ V_{CCIO}$	-30	_	-150	μΑ
I <sub>PD</sub>	I/O Active Pull-down Current	$V_{IL} (MAX) \le V_{IN} \le V_{CCIO}$	30	_	210	μΑ
I <sub>BHLS</sub>	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	_	—	μΑ
I <sub>BHHS</sub>	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCIO}$	-30	_	—	μΑ
I <sub>BHLO</sub>	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	_	210	μΑ
I <sub>BHHO</sub>	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	_	-150	μΑ
V <sub>BHT</sub>	Bus Hold Trip Points		$V_{IL}$ (MAX)	_	V <sub>IH</sub> (MIN)	V
C1	I/O Capacitance <sup>2</sup>	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} \text{ (MAX)}$	—	8	—	pf
C2	Dedicated Input Capacitance	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} \text{ (MAX)}$	—	6	—	pf

#### **Over Recommended Operating Conditions**

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. T<sub>A</sub> 25°C, f = 1.0 MHz.



# Supply Current (Standby)<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Device	Typical⁵	Units
		XP2-5	14	mA
		XP2-8	18	mA
I <sub>CC</sub>	Core Power Supply Current	XP2-17	24	mA
		XP2-30	35	mA
		XP2-40	45	mA
	Auxiliary Power Supply Current <sup>6</sup>	XP2-5	15	mA
		XP2-8	15	mA
I <sub>CCAUX</sub>		XP2-17	15	mA
		XP2-30	16	mA
		XP2-40	16	mA
I <sub>CCPLL</sub>	PLL Power Supply Current (per PLL)		0.1	mA
I <sub>CCIO</sub>	Bank Power Supply Current (per bank)		2	mA
ICCJ	V <sub>CCJ</sub> Power Supply Current		0.25	mA

### **Over Recommended Operating Conditions**

1. For further information on supply current, please see TN1139, Power Estimation and Management for LatticeXP2 Devices.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V<sub>CCIO</sub> or GND.

3. Frequency 0 MHz.

4. Pattern represents a "blank" configuration data file.

5.  $T_J = 25^{\circ}C$ , power supplies at nominal voltage.

6. In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I<sub>CCAUX</sub> and I<sub>CCPLL</sub>. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.



### **Register-to-Register Performance (Continued)**

Function	-7 Timing	Units
DSP IP Functions		
16-Tap Fully-Parallel FIR Filter	198	MHz
1024-pt FFT	221	MHz
8X8 Matrix Multiplication	196	MHz

1. These timing numbers were generated using the ispLEVER design tool. Exact performance may vary with device, design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

# **Derating Timing Tables**

Logic timing provided in the following sections of this data sheet and the Diamond design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.



# **EBR Timing Diagrams**





Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-7. Read/Write Mode with Input and Output Registers





# LatticeXP2 Family Timing Adders<sup>1, 2, 3, 4</sup> (Continued)

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	0.32	0.69	1.06	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	0.32	0.69	1.06	ns
SSTL33_I	SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33_II	SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33D_II	Differential SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL18_I	SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
LVTTL33_4mA	LVTTL 4mA drive	-0.37	-0.05	0.26	ns
LVTTL33_8mA	LVTTL 8mA drive	-0.45	-0.18	0.10	ns
LVTTL33_12mA	LVTTL 12mA drive	-0.52	-0.24	0.04	ns
LVTTL33_16mA	LVTTL 16mA drive	-0.43	-0.14	0.14	ns
LVTTL33_20mA	LVTTL 20mA drive	-0.46	-0.18	0.09	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	-0.37	-0.05	0.26	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	-0.45	-0.18	0.10	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	-0.52	-0.24	0.04	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	-0.43	-0.14	0.14	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	-0.46	-0.18	0.09	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	-0.42	-0.15	0.13	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	-0.48	-0.21	0.05	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	-0.45	-0.18	0.08	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	-0.49	-0.22	0.04	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	-0.46	-0.18	0.10	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	-0.52	-0.25	0.02	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.56	-0.30	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	-0.50	-0.24	0.03	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate	-0.45	-0.17	0.11	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate	-0.53	-0.26	0.00	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate	-0.46	-0.19	0.08	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate	-0.55	-0.29	-0.02	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate	0.98	1.41	1.84	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate	0.74	1.16	1.58	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate	0.56	0.97	1.38	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate	0.77	1.19	1.61	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate	0.57	0.98	1.40	ns

### **Over Recommended Operating Conditions**



# FlashBAK Time (from EBR to Flash)

### **Over Recommended Operating Conditions**

Device	EBR Density (Bits)	Time (Typ.)	Units
XP2-5	166K	1.5	S
XP2-8	221K	1.5	S
XP2-17	276K	1.5	S
XP2-30	387K	2.0	S
XP2-40	885K	3.0	S

# JTAG Port Timing Specifications

### **Over Recommended Operating Conditions**

Symbol	Parameter	Min.	Max.	Units
f <sub>MAX</sub>	TCK Clock Frequency	—	25	MHz
t <sub>BTCP</sub>	TCK [BSCAN] clock pulse width	40	—	ns
t <sub>BTCPH</sub>	TCK [BSCAN] clock pulse width high	20	—	ns
t <sub>BTCPL</sub>	TCK [BSCAN] clock pulse width low	20	—	ns
t <sub>BTS</sub>	TCK [BSCAN] setup time	8	—	ns
t <sub>BTH</sub>	TCK [BSCAN] hold time	10	—	ns
t <sub>BTRF</sub>	TCK [BSCAN] rise/fall time	50	—	mV/ns
t <sub>BTCO</sub>	TAP controller falling edge of clock to valid output	—	10	ns
t <sub>BTCODIS</sub>	TAP controller falling edge of clock to valid disable	—	10	ns
t <sub>BTCOEN</sub>	TAP controller falling edge of clock to valid enable	—	10	ns
t <sub>BTCRS</sub>	BSCAN test capture register setup time	8	—	ns
t <sub>BTCRH</sub>	BSCAN test capture register hold time	25	—	ns
t <sub>BUTCO</sub>	BSCAN test update register, falling edge of clock to valid output	—	25	ns
t <sub>BTUODIS</sub>	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
t <sub>BTUPOEN</sub>	BSCAN test update register, falling edge of clock to valid enable	_	25	ns



# Pin Information Summary

			XP	2-5		XP2-8		XP2-17		XP2-30		XP2-40					
Pin Ty	ре	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
Single Ended Use	er I/O	86	100	146	172	86	100	146	201	146	201	358	201	363	472	363	540
Differential Pair	Normal	35	39	57	66	35	39	57	77	57	77	135	77	137	180	137	204
User I/O	Highspeed	8	11	16	20	8	11	16	23	16	23	44	23	44	56	44	66
	TAP	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
Configuration	Muxed	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9
	Dedicated	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Non Configura-	Muxed	5	5	7	7	7	7	9	9	11	11	21	7	11	13	11	13
tion	Dedicated	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Vcc		6	4	9	6	6	4	9	6	9	6	16	6	16	20	16	20
Vccaux		4	4	4	4	4	4	4	4	4	4	8	4	8	8	8	8
VCCPLL		2	2	2	-	2	2	2	-	4	-	-	-	-	-	-	-
	Bank0	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
	Bank1	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank2	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
VCCIO	Bank3	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
10010	Bank4	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank5	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
	Bank6	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank7	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
GND, GND0-GNI	77	15	15	20	20	15	15	22	20	22	20	56	20	56	64	56	64
NC		-	-	4	31	-	-	2	2	-	2	7	2	2	69	2	1
	Bank0	18/9	20/10	20/10	26/13	18/9	20/10	20/10	28/14	20/10	28/14	52/26	28/14	52/26	70/35	52/26	70/35
	Bank1	4/2	6/3	18/9	18/9	4/2	6/3	18/9	22/11	18/9	22/11	36/18	22/11	36/18	54/27	36/18	70/35
	Bank2	16/8	18/9	18/9	22/11	16/8	18/9	18/9	26/13	18/9	26/13	46/23	26/13	46/23	56/28	46/23	64/32
Single Ended/	Bank3	4/2	4/2	16/8	20/10	4/2	4/2	16/8	24/12	16/8	24/12	44/22	24/12	46/23	56/28	46/23	66/33
per Bank	Bank4	8/4	8/4	18/9	18/9	8/4	8/4	18/9	26/13	18/9	26/13	36/18	26/13	38/19	54/27	38/19	70/35
	Bank5	14/7	18/9	20/10	24/12	14/7	18/9	20/10	24/12	20/10	24/12	52/26	24/12	53/26	70/35	53/26	70/35
	Bank6	6/3	8/4	18/9	22/11	6/3	8/4	18/9	27/13	18/9	27/13	46/23	27/13	46/23	56/28	46/23	66/33
	Bank7	16/8	18/9	18/9	22/11	16/8	18/9	18/9	24/12	18/9	24/12	46/23	24/12	46/23	56/28	46/23	64/32
	Bank0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank2	3	4	4	5	3	4	4	6	4	6	11	6	11	14	11	16
True LVDS Pairs	Bank3	1	1	4	5	1	1	4	6	4	6	11	6	11	14	11	17
Bank	Bank4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank6	1	2	4	5	1	2	4	6	4	6	11	6	11	14	11	17
	Bank7	3	4	4	5	3	4	4	5	4	5	11	5	11	14	11	16
	Bank0	1	1	1	1	1	1	1	1	1	1	3	1	2	4	2	4
	Bank1	0	0	1	1	0	0	1	1	1	1	2	1	2	3	2	4
	Bank2	1	1	1	1	1	1	1	1	1	1	2	1	3	3	3	4
DDR Banks	Bank3	0	0	1	1	0	0	1	1	1	1	2	1	3	3	3	4
I/O Bank <sup>1</sup>	Bank4	0	0	1	1	0	0	1	1	1	1	2	1	2	3	2	4
	Bank5	1	1	1	1	1	1	1	1	1	1	3	1	2	4	2	4
	Bank6	0	0	1	1	0	0	1	1	1	1	2	1	3	3	3	4
Ba	Bank7	1	1	1	1	1	1	1	1	1	1	2	1	3	3	3	4



# LatticeXP2 Family Data Sheet Ordering Information

#### February 2012

Data Sheet DS1009

### **Part Number Description**



# **Ordering Information**

The LatticeXP2 devices are marked with a single temperature grade, either Commercial or Industrial, as shown below.



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Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5F484C	1.2V	-5	fpBGA	484	COM	40
LFXP2-40E-6F484C	1.2V	-6	fpBGA	484	COM	40
LFXP2-40E-7F484C	1.2V	-7	fpBGA	484	COM	40
LFXP2-40E-5F672C	1.2V	-5	fpBGA	672	COM	40
LFXP2-40E-6F672C	1.2V	-6	fpBGA	672	COM	40
LFXP2-40E-7F672C	1.2V	-7	fpBGA	672	COM	40

#### Industrial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5M132I	1.2V	-5	csBGA	132	IND	5
LFXP2-5E-6M132I	1.2V	-6	csBGA	132	IND	5
LFXP2-5E-6FT256I	1.2V	-6	ftBGA	256	IND	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5M132I	1.2V	-5	csBGA	132	IND	8
LFXP2-8E-6M132I	1.2V	-6	csBGA	132	IND	8
LFXP2-5E-5FT256I	1.2V	-5	ftBGA	256	IND	5
LFXP2-8E-5FT256I	1.2V	-5	ftBGA	256	IND	8
LFXP2-8E-6FT256I	1.2V	-6	ftBGA	256	IND	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5FT256I	1.2V	-5	ftBGA	256	IND	17
LFXP2-17E-6FT256I	1.2V	-6	ftBGA	256	IND	17
LFXP2-17E-5F484I	1.2V	-5	fpBGA	484	IND	17
LFXP2-17E-6F484I	1.2V	-6	fpBGA	484	IND	17

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-30E-5FT256I	1.2V	-5	ftBGA	256	IND	30
LFXP2-30E-6FT256I	1.2V	-6	ftBGA	256	IND	30
LFXP2-30E-5F484I	1.2V	-5	fpBGA	484	IND	30
LFXP2-30E-6F484I	1.2V	-6	fpBGA	484	IND	30
LFXP2-30E-5F672I	1.2V	-5	fpBGA	672	IND	30
LFXP2-30E-6F672I	1.2V	-6	fpBGA	672	IND	30