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Details

Product Status	Active
Number of LABs/CLBs	2125
Number of Logic Elements/Cells	17000
Total RAM Bits	282624
Number of I/O	146
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-17e-7qn208c

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PFU Blocks

The core of the LatticeXP2 device is made up of logic blocks in two forms, PFUs and PFFs. PFUs can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. PFF blocks can be programmed to perform logic, arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered Slice 0 through Slice 3, as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.



Figure 2-12. Secondary Clock Selection



Slice Clock Selection

Figure 2-13 shows the clock selections and Figure 2-14 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals, via routing, can be used as clock inputs to the slices. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control, then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-13. Slice0 through Slice2 Clock Selection





sysMEM Memory

LatticeXP2 devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of 18 Kbit RAM with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-5. FIFOs can be implemented in sysMEM EBR blocks by using support logic with PFUs. The EBR block supports an optional parity bit for each data byte to facilitate parity checking. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths.

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

FlashBAK EBR Content Storage

All the EBR memory in the LatticeXP2 is shadowed by Flash memory. Optionally, initialization values for the memory blocks can be defined using the Lattice Diamond design tools. The initialization values are loaded into the Flash memory during device programming and into the SRAM at power up or whenever the device is reconfigured. This feature is ideal for the storage of a variety of information such as look-up tables and microprocessor code. It is also possible to write the current contents of the EBR memory back to Flash memory. This capability is useful for the storage of data such as error codes and calibration information. For additional information on the FlashBAK capability see TN1137, LatticeXP2 Memory Usage Guide.



For further information on the sysMEM EBR block, please see TN1137, LatticeXP2 Memory Usage Guide.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the low-to-high transition of the reset signal, as shown in Figure 2-18. The GSR input to the EBR is always asynchronous.



Reset	
Clock	
Clock —————— Enable	

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of 1/f_{MAX} (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

sysDSP™ Block

The LatticeXP2 family provides a sysDSP block making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications include Bit Correlators, Fast Fourier Transform (FFT) functions, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/ Decoder and Convolutional Encoder/Decoder. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Block Approach Compare to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeXP2 family, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-19 compares the fully serial and the mixed parallel and serial implementations.



MULTADDSUB sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. The user can enable the input, output and pipeline registers. Figure 2-22 shows the MULTADDSUB sysDSP element.

Figure 2-22. MULTADDSUB





Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysIO buffers as shown in Figure 2-25. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysIO buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

Figure 2-25. PIC Diagram



Signals are available on left/right/bottom edges only.
 Selected blocks.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C") as shown in Figure 2-25. The PAD Labels "T" and "C" distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as inputs.



DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock, referred to as DQS, is not free-running, and this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only, as shown in Figure 2-30) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figure 2-30 and Figure 2-31 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of 6-bit bus calibration signals from two dedicated DLLs (DDR_DLL) on opposite sides of the device. Each DLL compensates DQS delays in its half of the device as shown in Figure 2-30. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.



Figure 2-30. Edge Clock, DLL Calibration and DQS Local Bus Distribution



Figure 2-31. DQS Local Bus



*DQSXFERDEL shifts ECLK1 by 90% and is not associated with a particular PIO.

Polarity Control Logic

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeXP2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block and requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.



DQSXFER

LatticeXP2 devices provide a DQSXFER signal to the output buffer to assist it in data transfer to DDR memories that require DQS strobe be shifted 90°. This shifted DQS strobe is generated by the DQSDEL block. The DQSXFER signal runs the span of the data bus.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

sysIO Buffer Banks

LatticeXP2 devices have eight sysIO buffer banks for user I/Os arranged two per side. Each bank is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank has voltage references, V_{REF1} and V_{REF2} , that allow it to be completely independent from the others. Figure 2-32 shows the eight banks and their associated supplies.

In LatticeXP2 devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO} . LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO} .

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2} , that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

тор

Figure 2-32. LatticeXP2 Banks



воттом



LatticeXP2 devices contain two types of sysIO buffer pairs.

1. Top and Bottom (Banks 0, 1, 4 and 5) sysIO Buffer Pairs (Single-Ended Outputs Only)

The sysIO buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Only the I/Os on the top and bottom banks have programmable PCI clamps.

2. Left and Right (Banks 2, 3, 6 and 7) sysIO Buffer Pairs (50% Differential and 100% Single-Ended Outputs) The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp pad is associated with the negative side of the differential I/O.

LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

Typical sysIO I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when $V_{CC, V} C_{CCONFIG} (V_{CCIO7})$ and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. During power up and before the FPGA core logic becomes active, all user I/Os will be high-impedance with weak pull-up. Please refer to TN1136, <u>LatticeXP2 sysIO</u> Usage Guide for additional information.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported sysIO Standards

The LatticeXP2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8V, 2.5V and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, MLVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-12 and 2-13 show the I/O standards (together with their supply and reference voltages) supported by LatticeXP2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1136, LatticeXP2 sysIO Usage Guide.



Supply Current (Standby)^{1, 2, 3, 4}

Symbol	Parameter	Device	Typical⁵	Units
		XP2-5	14	mA
		XP2-8	18	mA
I _{CC}	Core Power Supply Current	XP2-17	24	mA
		XP2-30	35	mA
		XP2-40	45	mA
		XP2-5	15	mA
	Auxiliary Power Supply Current ⁶	XP2-8	15	mA
I _{CCAUX}		XP2-17	15	mA
		XP2-30	16	mA
		XP2-40	16	mA
I _{CCPLL}	PLL Power Supply Current (per PLL)		0.1	mA
I _{CCIO}	Bank Power Supply Current (per bank)		2	mA
I _{CCJ}	V _{CCJ} Power Supply Current		0.25	mA

Over Recommended Operating Conditions

1. For further information on supply current, please see TN1139, Power Estimation and Management for LatticeXP2 Devices.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

3. Frequency 0 MHz.

4. Pattern represents a "blank" configuration data file.

5. $T_J = 25^{\circ}C$, power supplies at nominal voltage.

6. In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.



Programming and Erase Flash Supply Current^{1, 2, 3, 4, 5}

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical (25°C, Max. Supply) ⁶	Units
		XP2-5	17	mA
		XP2-8	21	mA
I _{CC}	Core Power Supply Current	XP2-17	28	mA
		XP2-30	36	mA
		XP2-40	50	mA
I _{CCAUX}		XP2-5	64	mA
	Auxiliary Power Supply Current ⁷	XP2-8	66	mA
		XP2-17	83	mA
		XP2-30	87	mA
		XP2-40	88	mA
I _{CCPLL}	PLL Power Supply Current (per PLL)		0.1	mA
I _{CCIO}	Bank Power Supply Current (per Bank)		5	mA
I _{CCJ}	V _{CCJ} Power Supply Current ⁸		14	mA

1. For further information on supply current, please see TN1139, Power Estimation and Management for LatticeXP2 Devices.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

3. Frequency 0 MHz (excludes dynamic power from FPGA operation).

4. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.

5. Bypass or decoupling capacitor across the supply.

6. $T_J = 25^{\circ}C$, power supplies at nominal voltage.

In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual
auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the
auxiliary power supply.

8. When programming via JTAG.



sysIO Single-Ended DC Electrical Characteristics

Input/Output		V _{IL}	V _{IH} V _{OL}		V _{OL}	V _{OH}			
Standard	Min. (V)	Max. (V)	Min. (V)	Max. (V)	Max. (V)	Min. (V)	l _{OL} 1 (mA)	l _{OH} ¹ (mA)	
LVCMOS33	-0.3	0.8	2.0	3.6	0.4	V _{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4	
					0.2	V _{CCIO} - 0.2	0.1	-0.1	
LVTTL33	-0.3	0.8	2.0	3.6	0.4	V _{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4	
					0.2	V _{CCIO} - 0.2	0.1	-0.1	
LVCMOS25	-0.3	0.7	1.7	3.6	0.4	V _{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4	
					0.2	V _{CCIO} - 0.2	0.1	-0.1	
LVCMOS18	-0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.6	0.4	V _{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4	
					0.2	V _{CCIO} - 0.2	0.1	-0.1	
	0.2	0.25 \/	0.65 \	2.6	0.4	V _{CCIO} - 0.4	8, 4	-8, -4	
	-0.3	0.35 VCCIO	0.05 V CCIO	3.0	0.2	V _{CCIO} - 0.2	0.1	-0.1	
	-0.3	0.35 V	0.65 V	3.6	0.4	V _{CCIO} - 0.4	6, 2	-6, -2	
	-0.5	0.35 V _{CC}	0.05 V _{CC}	3.0	0.2	V _{CCIO} - 0.2	0.1	-0.1	
PCI33	-0.3	0.3 V _{CCIO}	0.5 V _{CCIO}	3.6	0.1 V _{CCIO}	0.9 V _{CCIO}	1.5	-0.5	
SSTL33_I	-0.3	V _{REF} - 0.2	V _{REF} + 0.2	3.6	0.7	V _{CCIO} - 1.1	8	-8	
SSTL33_II	-0.3	V _{REF} - 0.2	V _{REF} + 0.2	3.6	0.5	V _{CCIO} - 0.9	16	-16	
SSTI 25 I	-0.3	-0.3 Vace - 0.18	Vpcc + 0.18	36	0.54	Vooio - 0.62	7.6	-7.6	
001220_1	-0.0	VREF - 0.10	VREF + 0.10	0.0	0.04	ACCIO - 0.05	12	-12	
SSTI 25 II	-0.3	V 0.19	V 10.19	2.6 0.25	6 0.35	36 035	Vac: a 0.43	15.2	-15.2
001225_11	-0.0	VREF - 0.10	VREF + 0.10	0.0	0.00	ACCIO - 0.42	20	-20	
SSTL18_I	-0.3	V _{REF} - 0.125	V _{REF} + 0.125	3.6	0.4	V _{CCIO} - 0.4	6.7	-6.7	
	-0.3	V0 125	V ± 0 125	36	0.28	Vac 0.28	8	-8	
001210_1	-0.0	VREF - 0.120	VREF + 0.120	0.0	0.20	VCCIO - 0.20	11	-11	
HSTI 15 I	-0.3	Vpcc - 0 1		3.6	0.4		4	-4	
	0.0	-0.3 V _{REF} - 0.1	VREF + 0.1	5.0	0.4	VCCIO - 0.4	8	-8	
HSTI 18 I	-0.3	Vp== - 0 1		26	0.4		8	-8	
	0.0	KEF - 0.1		0.0	U.T		12	-12	
HSTL18_II	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.6	0.4	V _{CCIO} - 0.4	16	-16	

Over Recommended Operating Conditions

 The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA, where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.



BLVDS

The LatticeXP2 devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.





Table 3-2. BLVDS DC Conditions¹

		Тур		
Parameter	Description	Ζο = 45 Ω	Ζο = 90 Ω	Units
V _{CCIO}	Output Driver Supply (+/- 5%)	2.50	2.50	V
Z _{OUT}	Driver Impedance	10.00	10.00	Ω
R _S	Driver Series Resistor (+/- 1%)	90.00	90.00	Ω
R _{TL}	Driver Parallel Resistor (+/- 1%)	45.00	90.00	Ω
R _{TR}	Receiver Termination (+/- 1%)	45.00	90.00	Ω
V _{OH}	Output High Voltage (After R _{TL})	1.38	1.48	V
V _{OL}	Output Low Voltage (After R _{TL})	1.12	1.02	V
V _{OD}	Output Differential Voltage (After R _{TL})	0.25	0.46	V
V _{CM}	Output Common Mode Voltage	1.25	1.25	V
I _{DC}	DC Output Current	11.24	10.20	mA

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.



Typical Building Block Function Performance¹

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	4.4	ns
32-bit Decoder	5.2	ns
64-bit Decoder	5.6	ns
4:1 MUX	3.7	ns
8:1 MUX	3.9	ns
16:1 MUX	4.3	ns
32:1 MUX	4.5	ns

Register-to-Register Performance

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	521	MHz
32-bit Decoder	537	MHz
64-bit Decoder	484	MHz
4:1 MUX	744	MHz
8:1 MUX	678	MHz
16:1 MUX	616	MHz
32:1 MUX	529	MHz
8-bit Adder	570	MHz
16-bit Adder	507	MHz
64-bit Adder	293	MHz
16-bit Counter	541	MHz
32-bit Counter	440	MHz
64-bit Counter	321	MHz
64-bit Accumulator	261	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	315	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	315	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	231	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (One PFU)	760	MHz
32x2 Pseudo-Dual Port RAM	455	MHz
64x1 Pseudo-Dual Port RAM	351	MHz
DSP Functions		
18x18 Multiplier (All Registers)	342	MHz
9x9 Multiplier (All Registers)	342	MHz
36x36 Multiply (All Registers)	330	MHz
18x18 Multiply/Accumulate (Input and Output Registers)	218	MHz
18x18 Multiply-Add/Sub-Sum (All Registers)	292	MHz



Register-to-Register Performance (Continued)

Function	-7 Timing	Units
DSP IP Functions		
16-Tap Fully-Parallel FIR Filter	198	MHz
1024-pt FFT	221	MHz
8X8 Matrix Multiplication	196	MHz

1. These timing numbers were generated using the ispLEVER design tool. Exact performance may vary with device, design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.



LatticeXP2 External Switching Characteristics (Continued)

			-	-7 -6		-5			
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
		XP2-5	1.00		1.30	_	1.60		ns
		XP2-8	1.00	_	1.30	_	1.60	_	ns
t _{HE}	Clock to Data Hold - PIO Input Register	XP2-17	1.00		1.30	_	1.60		ns
		XP2-30	1.20		1.60	_	1.90		ns
		XP2-40	1.20		1.60		1.90		ns
		XP2-5	1.00		1.30	_	1.60		ns
		XP2-8	1.00		1.30	_	1.60		ns
t _{SU_DELE}	Clock to Data Setup - PIO Input Begister with Data Input Delay	XP2-17	1.00		1.30	_	1.60		ns
		XP2-30	1.20		1.60		1.90		ns
		XP2-40	1.20		1.60		1.90		ns
		XP2-5	0.00		0.00		0.00		ns
		XP2-8	0.00	—	0.00	—	0.00	—	ns
t _{H_DELE}	Clock to Data Hold - PIO Input Begister with Input Data Delay	XP2-17	0.00	—	0.00	—	0.00	—	ns
		XP2-30	0.00		0.00		0.00		ns
		XP2-40	0.00		0.00		0.00		ns
f _{MAX_IOE}	Clock Frequency of I/O and PFU Register	XP2	_	420	_	357	_	311	MHz
General I/O Pir	Parameters (using Primary Clo	ck with PLL)1	1	1	1	1	1	
	Clock to Output - PIO Output Register	XP2-5	—	3.00	—	3.30	—	3.70	ns
		XP2-8		3.00		3.30		3.70	ns
t _{COPLL}		XP2-17		3.00		3.30		3.70	ns
		XP2-30	_	3.00		3.30		3.70	ns
		XP2-40		3.00		3.30		3.70	ns
		XP2-5	1.00		1.20		1.40		ns
		XP2-8	1.00		1.20		1.40		ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	XP2-17	1.00		1.20		1.40		ns
		XP2-30	1.00		1.20		1.40		ns
		XP2-40	1.00		1.20	_	1.40		ns
		XP2-5	0.90		1.10		1.30		ns
		XP2-8	0.90		1.10		1.30		ns
t _{HPLL}	Clock to Data Hold - PIO Input	XP2-17	0.90		1.10		1.30		ns
		XP2-30	1.00	—	1.20	—	1.40	—	ns
		XP2-40	1.00	—	1.20	—	1.40	—	ns
		XP2-5	1.90	—	2.10	—	2.30	—	ns
		XP2-8	1.90		2.10	—	2.30	_	ns
t _{SU_DELPLL}	Clock to Data Setup - PIO Input Begister with Data Input Delay	XP2-17	1.90	—	2.10	—	2.30	—	ns
	lingibion with Data input Delay	XP2-30	2.00	—	2.20	—	2.40	—	ns
		XP2-40	2.00	—	2.20	—	2.40	—	ns

Over Recommended Operating Conditions



LatticeXP2 Family Timing Adders^{1, 2, 3, 4} (Continued)

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	0.32	0.69	1.06	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	0.32	0.69	1.06	ns
SSTL33_I	SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33_II	SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33D_II	Differential SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL18_I	SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
LVTTL33_4mA	LVTTL 4mA drive	-0.37	-0.05	0.26	ns
LVTTL33_8mA	LVTTL 8mA drive	-0.45	-0.18	0.10	ns
LVTTL33_12mA	LVTTL 12mA drive	-0.52	-0.24	0.04	ns
LVTTL33_16mA	TTL33_16mA LVTTL 16mA drive		-0.14	0.14	ns
LVTTL33_20mA	.33_20mA LVTTL 20mA drive		-0.18	0.09	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	-0.37	-0.05	0.26	ns
LVCMOS33_8mA	BmA LVCMOS 3.3 8mA drive, fast slew rate		-0.18	0.10	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	-0.52	-0.24	0.04	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	-0.43	-0.14	0.14	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	-0.46	-0.18	0.09	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	-0.42	-0.15	0.13	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	-0.48	-0.21	0.05	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	-0.45	-0.18	0.08	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	-0.49	-0.22	0.04	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	-0.46	-0.18	0.10	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	-0.52	-0.25	0.02	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.56	-0.30	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	-0.50	-0.24	0.03	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate	-0.45	-0.17	0.11	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate	-0.53	-0.26	0.00	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate	-0.46	-0.19	0.08	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate	-0.55	-0.29	-0.02	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate	0.98	1.41	1.84	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate	0.74	1.16	1.58	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate	0.56	0.97	1.38	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate	0.77	1.19	1.61	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate	0.57	0.98	1.40	ns

Over Recommended Operating Conditions



LatticeXP2 Family Timing Adders^{1, 2, 3, 4} (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, slow slew rate	1.05	1.43	1.81	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, slow slew rate	0.78	1.15	1.52	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, slow slew rate	0.59	0.96	1.33	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, slow slew rate	0.81	1.18	1.55	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, slow slew rate	0.61	0.98	1.35	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, slow slew rate	1.01	1.38	1.75	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, slow slew rate	0.72	1.08	1.45	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, slow slew rate	0.53	0.90	1.26	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, slow slew rate	0.74	1.11	1.48	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, slow slew rate	0.96	1.33	1.71	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, slow slew rate	-0.53	-0.26	0.00	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, slow slew rate	0.90	1.27	1.65	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, slow slew rate	-0.55	-0.29	-0.02	ns
PCI33	3.3V PCI	-0.29	-0.01	0.26	ns

1. Timing Adders are characterized but not tested on every device.

2. LVCMOS timing measured with the load specified in Switching Test Condition table.

3. All other standards tested according to the appropriate specifications.

4. The base parameters used with these timing adders to calculate timing are listed in the LatticeXP2 Internal Switching Characteristics table under PIO Input/Output Timing.

5. These timing adders are measured with the recommended resistor values.



On-Chip Oscillator and Configuration Master Clock Characteristics

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value -30%	Selected value +30%	MHz
Duty Cycle	40	60	%

Over Recommended Operating Conditions

Figure 3-9. Master SPI Configuration Waveforms

