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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	3625
Number of Logic Elements/Cells	29000
Total RAM Bits	396288
Number of I/O	201
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-30e-5ftn256i

Features

■ flexiFLASH™ Architecture

- Instant-on
- Infinitely reconfigurable
- Single chip
- FlashBAK™ technology
- Serial TAG memory
- Design security

■ Live Update Technology

- TransFR™ technology
- Secure updates with 128 bit AES encryption
- Dual-boot with external SPI

■ sysDSP™ Block

- Three to eight blocks for high performance Multiply and Accumulate
- 12 to 32 18x18 multipliers
- Each block supports one 36x36 multiplier or four 18x18 or eight 9x9 multipliers

■ Embedded and Distributed Memory

- Up to 885 Kbits sysMEM™ EBR
- Up to 83 Kbits Distributed RAM

■ sysCLOCK™ PLLs

- Up to four analog PLLs per device
- Clock multiply, divide and phase shifting

■ Flexible I/O Buffer

- sysIO™ buffer supports:
 - LVCMOS 33/25/18/15/12; LVTTTL
 - SSTL 33/25/18 class I, II
 - HSTL15 class I; HSTL18 class I, II
 - PCI
 - LVDS, Bus-LVDS, MLVDS, LVPECL, RSDS

■ Pre-engineered Source Synchronous Interfaces

- DDR / DDR2 interfaces up to 200 MHz
- 7:1 LVDS interfaces support display applications
- XGMII

■ Density And Package Options

- 5k to 40k LUT4s, 86 to 540 I/Os
- csBGA, TQFP, PQFP, ftBGA and fpBGA packages
- Density migration supported

■ Flexible Device Configuration

- SPI (master and slave) Boot Flash Interface
- Dual Boot Image supported
- Soft Error Detect (SED) macro embedded

■ System Level Support

- IEEE 1149.1 and IEEE 1532 Compliant
- On-chip oscillator for initialization & general use
- Devices operate with 1.2V power supply

Table 1-1. LatticeXP2 Family Selection Guide

Device	XP2-5	XP2-8	XP2-17	XP2-30	XP2-40
LUTs (K)	5	8	17	29	40
Distributed RAM (KBits)	10	18	35	56	83
EBR SRAM (KBits)	166	221	276	387	885
EBR SRAM Blocks	9	12	15	21	48
sysDSP Blocks	3	4	5	7	8
18 x 18 Multipliers	12	16	20	28	32
V _{CC} Voltage	1.2	1.2	1.2	1.2	1.2
GPLL	2	2	4	4	4
Max Available I/O	172	201	358	472	540
Packages and I/O Combinations					
132-Ball csBGA (8 x 8 mm)	86	86			
144-Pin TQFP (20 x 20 mm)	100	100			
208-Pin PQFP (28 x 28 mm)	146	146	146		
256-Ball ftBGA (17 x 17 mm)	172	201	201	201	
484-Ball fpBGA (23 x 23 mm)			358	363	363
672-Ball fpBGA (27 x 27 mm)				472	540

Figure 2-5. Clock Divider Connections



Clock Distribution Network

LatticeXP2 devices have eight quadrant-based primary clocks and between six and eight flexible region-based secondary clocks/control signals. Two high performance edge clocks are available on each edge of the device to support high speed interfaces. The clock inputs are selected from external I/Os, the sysCLOCK PLLs, or routing. Clock inputs are fed throughout the chip via the primary, secondary and edge clock networks.

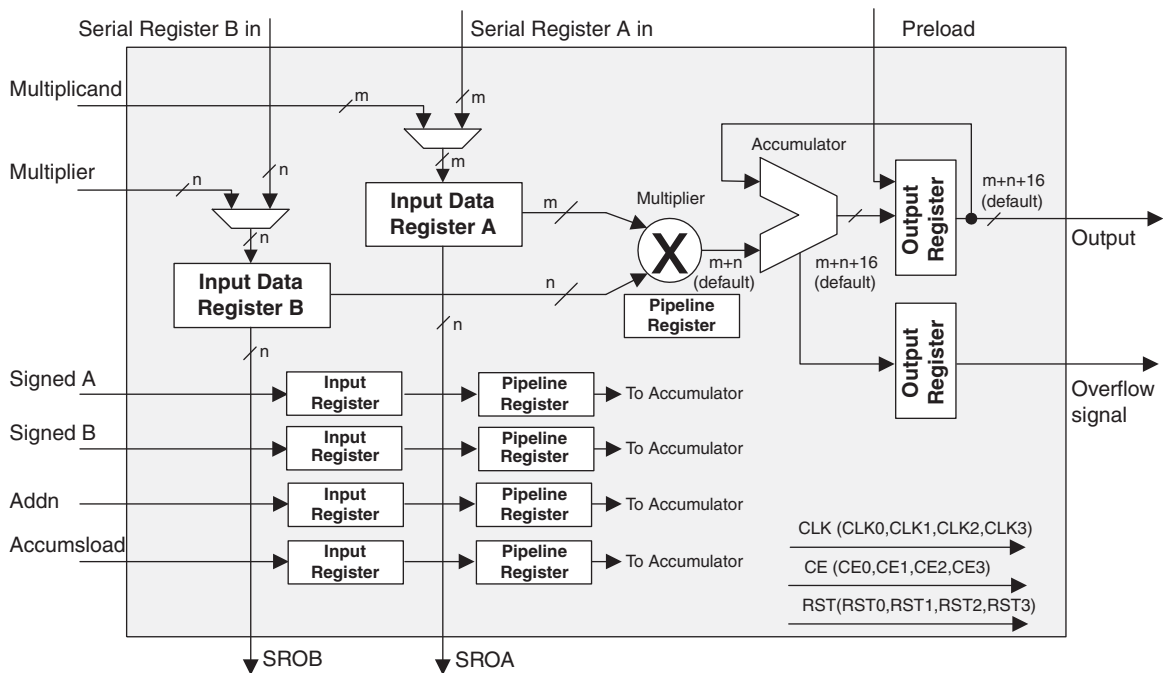
Primary Clock Sources

LatticeXP2 devices derive primary clocks from four sources: PLL outputs, CLKDIV outputs, dedicated clock inputs and routing. LatticeXP2 devices have two to four sysCLOCK PLLs, located in the four corners of the device. There are eight dedicated clock inputs, two on each side of the device. Figure 2-6 shows the primary clock sources.

MAC sysDSP Element

In this case, the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers but the output register is always enabled. The output register is used to store the accumulated value. The Accumulators in the DSP blocks in LatticeXP2 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-21 shows the MAC sysDSP element.

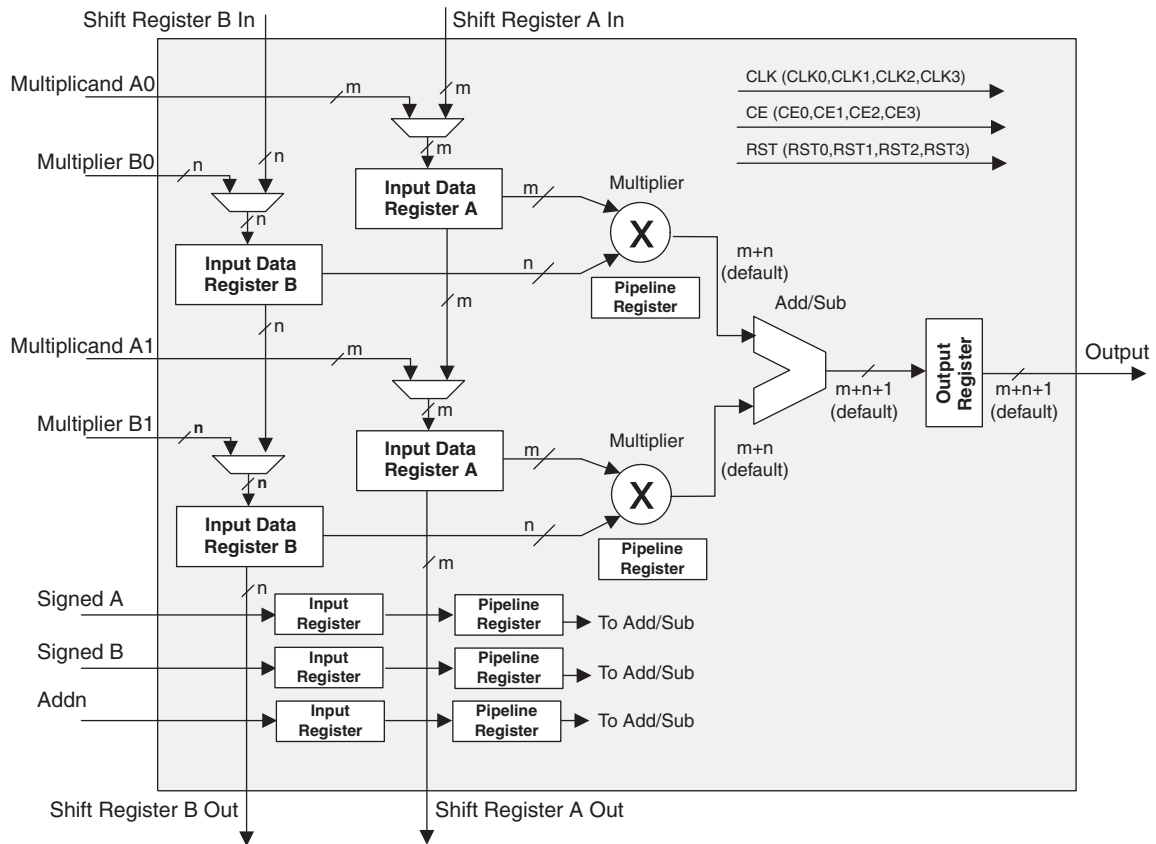
Figure 2-21. MAC sysDSP



MULTADDSUB sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. The user can enable the input, output and pipeline registers. Figure 2-22 shows the MULTADDSUB sysDSP element.

Figure 2-22. MULTADDSUB



IPexpress™

The user can access the sysDSP block via the Lattice IPexpress tool, which provides the option to configure each DSP module (or group of modules), or by direct HDL instantiation. In addition, Lattice has partnered with The Math-Works® to support instantiation in the Simulink® tool, a graphical simulation environment. Simulink works with Diamond to dramatically shorten the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LatticeXP2 DSP include the Bit Correlator, FFT functions, FIR Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IP cores.

Resources Available in the LatticeXP2 Family

Table 2-8 shows the maximum number of multipliers for each member of the LatticeXP2 family. Table 2-9 shows the maximum available EBR RAM Blocks and Serial TAG Memory bits in each LatticeXP2 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2-8. Maximum Number of DSP Blocks in the LatticeXP2 Family

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
XP2-5	3	24	12	3
XP2-8	4	32	16	4
XP2-17	5	40	20	5
XP2-30	7	56	28	7
XP2-40	8	64	32	8

Table 2-9. Embedded SRAM/TAG Memory in the LatticeXP2 Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)	TAG Memory (Bits)
XP2-5	9	166	632
XP2-8	12	221	768
XP2-17	15	276	2184
XP2-30	21	387	2640
XP2-40	48	885	3384

LatticeXP2 DSP Performance

Table 2-10 lists the maximum performance in Millions of MAC (MMAC) operations per second for each member of the LatticeXP2 family.

Table 2-10. DSP Performance

Device	DSP Block	DSP Performance MMAC
XP2-5	3	3,900
XP2-8	4	5,200
XP2-17	5	6,500
XP2-30	7	9,100
XP2-40	8	10,400

For further information on the sysDSP block, please see TN1140, [LatticeXP2 sysDSP Usage Guide](#).

DQSXFER

LatticeXP2 devices provide a DQSXFER signal to the output buffer to assist it in data transfer to DDR memories that require DQS strobe be shifted 90°. This shifted DQS strobe is generated by the DQSDEL block. The DQSXFER signal runs the span of the data bus.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

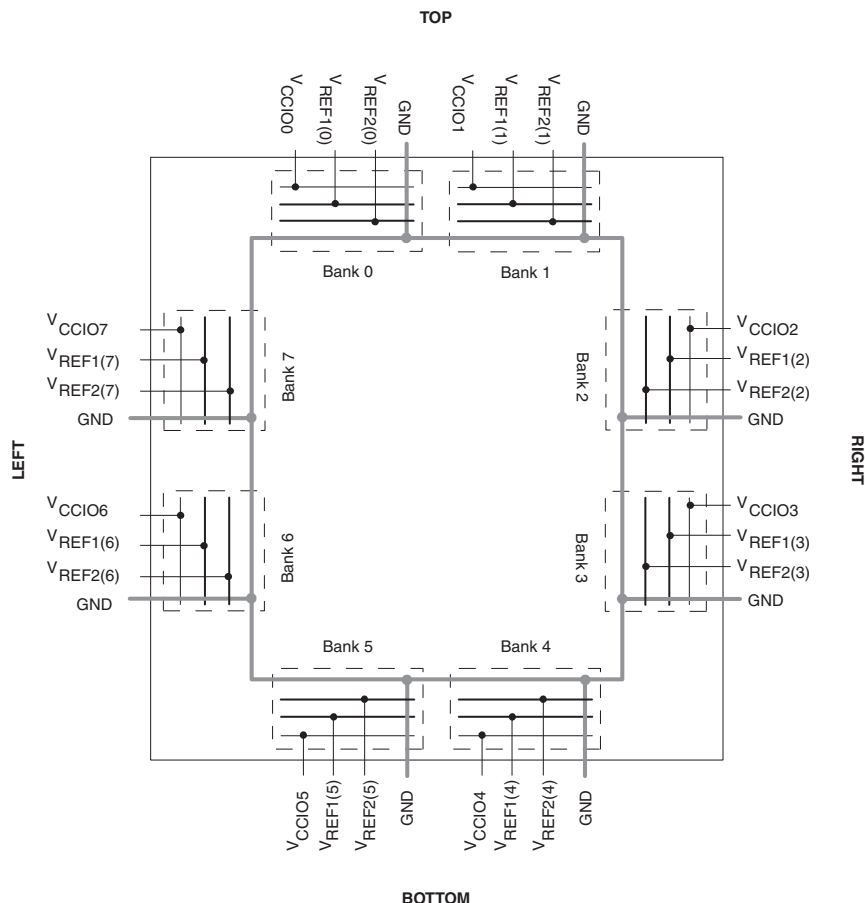
sysIO Buffer Banks

LatticeXP2 devices have eight sysIO buffer banks for user I/Os arranged two per side. Each bank is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank has voltage references, V_{REF1} and V_{REF2} , that allow it to be completely independent from the others. Figure 2-32 shows the eight banks and their associated supplies.

In LatticeXP2 devices, single-ended output buffers and ratioed input buffers (LVTTTL, LVCMOS and PCI) are powered using V_{CCIO} . LVTTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO} .

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2} , that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Figure 2-32. LatticeXP2 Banks



original backup configuration and try again. This all can be done without power cycling the system. For more information please see TN1220, [LatticeXP2 Dual Boot Feature](#).

For more information on device configuration, please see TN1141, [LatticeXP2 sysCONFIG Usage Guide](#).

Soft Error Detect (SED) Support

LatticeXP2 devices have dedicated logic to perform Cyclic Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, LatticeXP2 devices can be programmed for checking soft errors in SRAM. SED can be run on a programmed device when the user logic is not active. In the event a soft error occurs, the device can be programmed to either reload from a known good boot image (from internal Flash or external SPI memory) or generate an error signal.

For further information on SED support, please see TN1130, [LatticeXP2 Soft Error Detection \(SED\) Usage Guide](#).

On-Chip Oscillator

Every LatticeXP2 device has an internal CMOS oscillator that is used to derive a Master Clock (CCLK) for configuration. The oscillator and CCLK run continuously and are available to user logic after configuration is complete. The available CCLK frequencies are listed in Table 2-14. When a different CCLK frequency is selected during the design process, the following sequence takes place:

1. Device powers up with the default CCLK frequency.
2. During configuration, users select a different CCLK frequency.
3. CCLK frequency changes to the selected frequency after clock configuration bits are received.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1141, [LatticeXP2 sysCONFIG Usage Guide](#).

Table 2-14. Selectable CCLKs and Oscillator Frequencies During Configuration and User Mode

CCLK/Oscillator (MHz)
2.5 ¹
3.1 ²
4.3
5.4
6.9
8.1
9.2
10
13
15
20
26
32
40
54
80 ³
163 ³

1. Software default oscillator frequency.
2. Software default CCLK frequency.
3. Frequency not valid for CCLK.

Absolute Maximum Ratings^{1, 2, 3}

Supply Voltage V_{CC} -0.5 to 1.32V

Supply Voltage V_{CCAUX} -0.5 to 3.75V

Supply Voltage V_{CCJ} -0.5 to 3.75V

Supply Voltage V_{CCPLL} ⁴ -0.5 to 3.75V

Output Supply Voltage V_{CCIO} -0.5 to 3.75V

Input or I/O Tristate Voltage Applied⁵ -0.5 to 3.75V

Storage Temperature (Ambient) -65 to 150°C

Junction Temperature Under Bias (T_j) +125°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. V_{CCPLL} only available on csBGA, PQFP and TQFP packages.
5. Overshoot and undershoot of -2V to ($V_{IHMAX} + 2$) volts is permitted for a duration of <20 ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage	1.14	1.26	V
V_{CCAUX} ^{4, 5}	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCPLL} ¹	PLL Supply Voltage	3.135	3.465	V
V_{CCIO} ^{2, 3, 4}	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ} ²	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C

1. V_{CCPLL} only available on csBGA, PQFP and TQFP packages.
2. If V_{CCIO} or V_{CCJ} is set to 1.2 V, they must be connected to the same power supply as V_{CC} . If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX} .
3. See recommended voltages by I/O standard in subsequent table.
4. To ensure proper I/O behavior, V_{CCIO} must be turned off at the same time or earlier than V_{CCAUX} .
5. In fpBGA and ftBGA packages, the PLLs are connected to, and powered from, the auxiliary power supply.

On-Chip Flash Memory Specifications

Symbol	Parameter	Max.	Units
N_{PROG}	Flash Programming Cycles per $t_{RETENTION}$ ¹	10,000	Cycles
	Flash Functional Programming Cycles	100,000	

1. The minimum data retention, $t_{RETENTION}$, is 20 years.

Supply Current (Standby)^{1, 2, 3, 4}
Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical ⁵	Units
I_{CC}	Core Power Supply Current	XP2-5	14	mA
		XP2-8	18	mA
		XP2-17	24	mA
		XP2-30	35	mA
		XP2-40	45	mA
I_{CCAUX}	Auxiliary Power Supply Current ⁶	XP2-5	15	mA
		XP2-8	15	mA
		XP2-17	15	mA
		XP2-30	16	mA
		XP2-40	16	mA
I_{CCPLL}	PLL Power Supply Current (per PLL)		0.1	mA
I_{CCIO}	Bank Power Supply Current (per bank)		2	mA
I_{CCJ}	V_{CCJ} Power Supply Current		0.25	mA

1. For further information on supply current, please see TN1139, [Power Estimation and Management for LatticeXP2 Devices](#).
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0 MHz.
4. Pattern represents a "blank" configuration data file.
5. $T_J = 25^\circ\text{C}$, power supplies at nominal voltage.
6. In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL} . For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.

Table 3-1. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/-1%)	158	Ω
R _P	Driver Parallel Resistor (+/-1%)	140	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage (after R _P)	1.43	V
V _{OL}	Output Low Voltage (after R _P)	1.07	V
V _{OD}	Output Differential Voltage (After R _P)	0.35	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	6.03	mA

LVC MOS33D

All I/O banks support emulated differential I/O using the LVC MOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3V V_{CCIO}. The default drive current for LVC MOS33D output is 12mA with the option to change the device strength to 4mA, 8mA, 16mA or 20mA. Follow the LVC MOS33 specifications for the DC characteristics of the LVC MOS33D.

RSDS

The LatticeXP2 devices support differential RSDS standard. This standard is emulated using complementary LVC-MOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

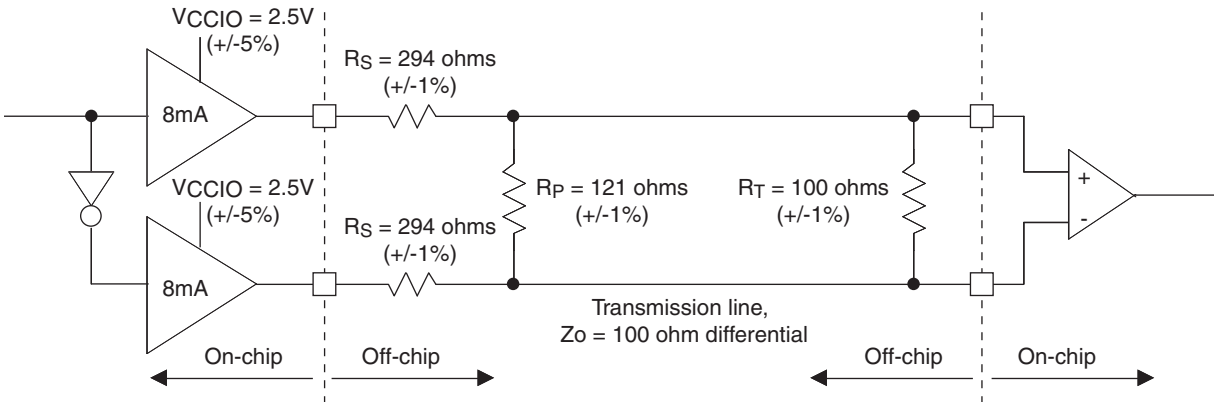


Table 3-4. RSDS DC Conditions¹

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply ($\pm 5\%$)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor ($\pm 1\%$)	294	Ω
R_P	Driver Parallel Resistor ($\pm 1\%$)	121	Ω
R_T	Receiver Termination ($\pm 1\%$)	100	Ω
V_{OH}	Output High Voltage (After R_P)	1.35	V
V_{OL}	Output Low Voltage (After R_P)	1.15	V
V_{OD}	Output Differential Voltage (After R_P)	0.20	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	101.5	Ω
I_{DC}	DC Output Current	3.66	mA

1. For input buffer, see LVDS table.

MLVDS

The LatticeXP2 devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.

Figure 3-5. MLVDS (Reduced Swing Differential Standard)

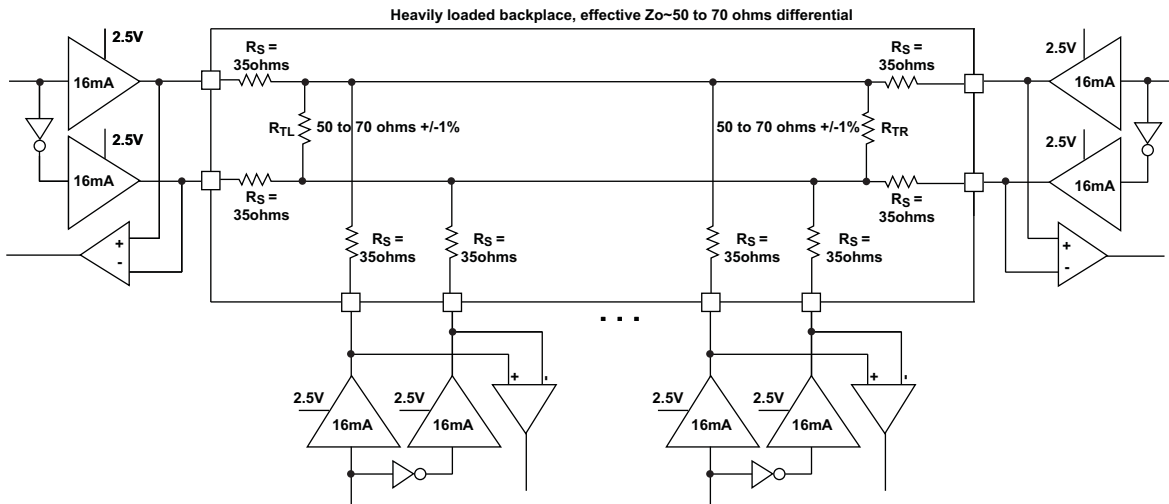


Table 3-5. MLVDS DC Conditions¹

Parameter	Description	Typical		Units
		$Z_o=50\Omega$	$Z_o=70\Omega$	
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (+/-1%)	35.00	35.00	Ω
R_{TL}	Driver Parallel Resistor (+/-1%)	50.00	70.00	Ω
R_{TR}	Receiver Termination (+/-1%)	50.00	70.00	Ω
V_{OH}	Output High Voltage (After R_{TL})	1.52	1.60	V
V_{OL}	Output Low Voltage (After R_{TL})	0.98	0.90	V
V_{OD}	Output Differential Voltage (After R_{TL})	0.54	0.70	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see details of additional technical information at the end of this data sheet.

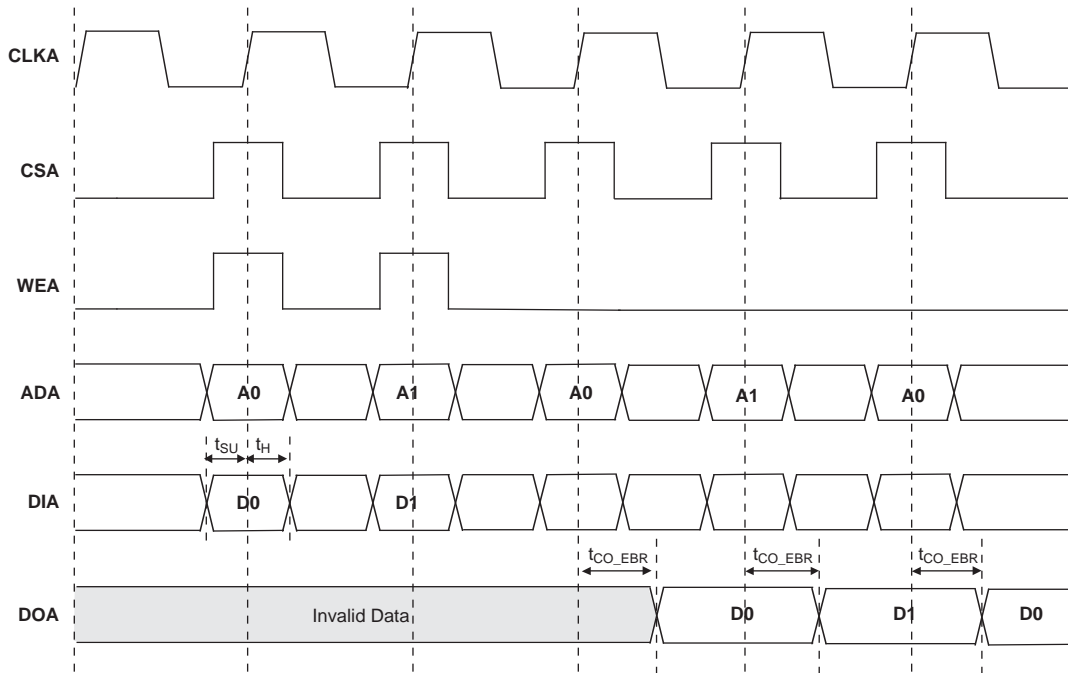
LatticeXP2 External Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HE}	Clock to Data Hold - PIO Input Register	XP2-5	1.00	—	1.30	—	1.60	—	ns
		XP2-8	1.00	—	1.30	—	1.60	—	ns
		XP2-17	1.00	—	1.30	—	1.60	—	ns
		XP2-30	1.20	—	1.60	—	1.90	—	ns
		XP2-40	1.20	—	1.60	—	1.90	—	ns
t_{SU_DELE}	Clock to Data Setup - PIO Input Register with Data Input Delay	XP2-5	1.00	—	1.30	—	1.60	—	ns
		XP2-8	1.00	—	1.30	—	1.60	—	ns
		XP2-17	1.00	—	1.30	—	1.60	—	ns
		XP2-30	1.20	—	1.60	—	1.90	—	ns
		XP2-40	1.20	—	1.60	—	1.90	—	ns
t_{H_DELE}	Clock to Data Hold - PIO Input Register with Input Data Delay	XP2-5	0.00	—	0.00	—	0.00	—	ns
		XP2-8	0.00	—	0.00	—	0.00	—	ns
		XP2-17	0.00	—	0.00	—	0.00	—	ns
		XP2-30	0.00	—	0.00	—	0.00	—	ns
		XP2-40	0.00	—	0.00	—	0.00	—	ns
f_{MAX_IOE}	Clock Frequency of I/O and PFU Register	XP2	—	420	—	357	—	311	MHz
General I/O Pin Parameters (using Primary Clock with PLL)¹									
t_{COPLL}	Clock to Output - PIO Output Register	XP2-5	—	3.00	—	3.30	—	3.70	ns
		XP2-8	—	3.00	—	3.30	—	3.70	ns
		XP2-17	—	3.00	—	3.30	—	3.70	ns
		XP2-30	—	3.00	—	3.30	—	3.70	ns
		XP2-40	—	3.00	—	3.30	—	3.70	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	XP2-5	1.00	—	1.20	—	1.40	—	ns
		XP2-8	1.00	—	1.20	—	1.40	—	ns
		XP2-17	1.00	—	1.20	—	1.40	—	ns
		XP2-30	1.00	—	1.20	—	1.40	—	ns
		XP2-40	1.00	—	1.20	—	1.40	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	XP2-5	0.90	—	1.10	—	1.30	—	ns
		XP2-8	0.90	—	1.10	—	1.30	—	ns
		XP2-17	0.90	—	1.10	—	1.30	—	ns
		XP2-30	1.00	—	1.20	—	1.40	—	ns
		XP2-40	1.00	—	1.20	—	1.40	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	XP2-5	1.90	—	2.10	—	2.30	—	ns
		XP2-8	1.90	—	2.10	—	2.30	—	ns
		XP2-17	1.90	—	2.10	—	2.30	—	ns
		XP2-30	2.00	—	2.20	—	2.40	—	ns
		XP2-40	2.00	—	2.20	—	2.40	—	ns

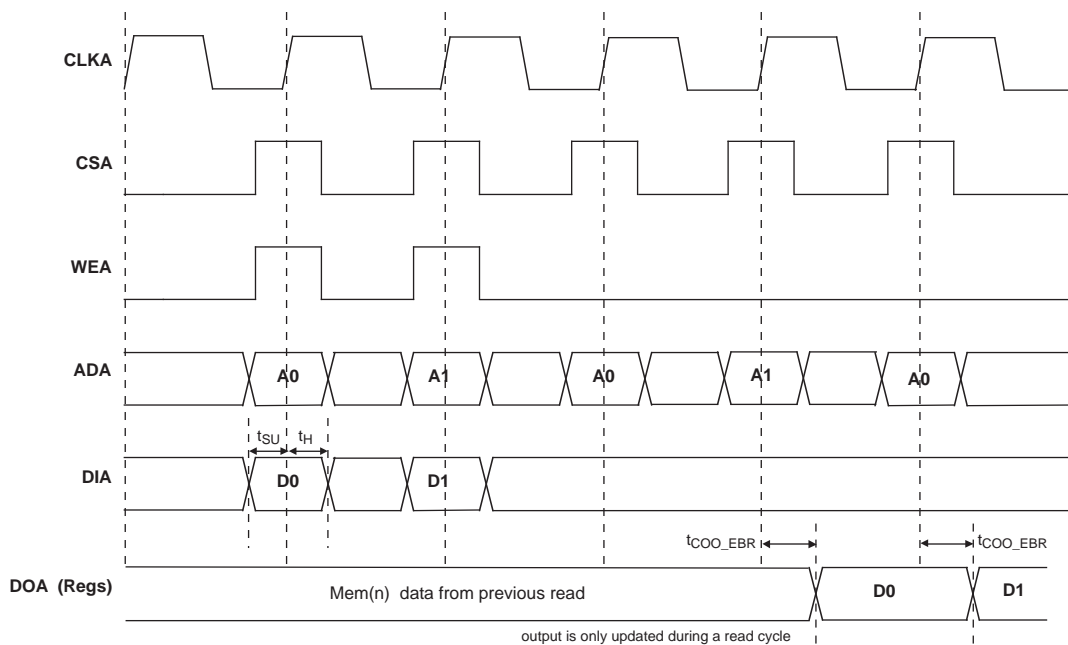
EBR Timing Diagrams

Figure 3-6. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-7. Read/Write Mode with Input and Output Registers



LatticeXP2 Family Timing Adders^{1, 2, 3, 4}
Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
Input Adjusters					
LVDS25	LVDS	-0.26	-0.11	0.04	ns
BLVDS25	BLVDS	-0.26	-0.11	0.04	ns
MLVDS	LVDS	-0.26	-0.11	0.04	ns
RSDS	RSDS	-0.26	-0.11	0.04	ns
LVPECL33	LVPECL	-0.26	-0.11	0.04	ns
HSTL18_I	HSTL_18 class I	-0.23	-0.08	0.07	ns
HSTL18_II	HSTL_18 class II	-0.23	-0.08	0.07	ns
HSTL18D_I	Differential HSTL 18 class I	-0.28	-0.13	0.02	ns
HSTL18D_II	Differential HSTL 18 class II	-0.28	-0.13	0.02	ns
HSTL15_I	HSTL_15 class I	-0.23	-0.09	0.06	ns
HSTL15D_I	Differential HSTL 15 class I	-0.28	-0.13	0.01	ns
SSTL33_I	SSTL_3 class I	-0.20	-0.04	0.12	ns
SSTL33_II	SSTL_3 class II	-0.20	-0.04	0.12	ns
SSTL33D_I	Differential SSTL_3 class I	-0.27	-0.11	0.04	ns
SSTL33D_II	Differential SSTL_3 class II	-0.27	-0.11	0.04	ns
SSTL25_I	SSTL_2 class I	-0.21	-0.06	0.10	ns
SSTL25_II	SSTL_2 class II	-0.21	-0.06	0.10	ns
SSTL25D_I	Differential SSTL_2 class I	-0.27	-0.12	0.03	ns
SSTL25D_II	Differential SSTL_2 class II	-0.27	-0.12	0.03	ns
SSTL18_I	SSTL_18 class I	-0.23	-0.08	0.07	ns
SSTL18_II	SSTL_18 class II	-0.23	-0.08	0.07	ns
SSTL18D_I	Differential SSTL_18 class I	-0.28	-0.13	0.02	ns
SSTL18D_II	Differential SSTL_18 class II	-0.28	-0.13	0.02	ns
LVTTTL33	LVTTTL	-0.09	0.05	0.18	ns
LVC MOS33	LVC MOS 3.3	-0.09	0.05	0.18	ns
LVC MOS25	LVC MOS 2.5	0.00	0.00	0.00	ns
LVC MOS18	LVC MOS 1.8	-0.23	-0.07	0.09	ns
LVC MOS15	LVC MOS 1.5	-0.20	-0.02	0.16	ns
LVC MOS12	LVC MOS 1.2	-0.35	-0.20	-0.04	ns
PCI33	3.3V PCI	-0.09	0.05	0.18	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E ⁵	-0.25	0.02	0.30	ns
LVDS25	LVDS 2.5	-0.25	0.02	0.30	ns
BLVDS25	BLVDS 2.5	-0.28	0.00	0.28	ns
MLVDS	MLVDS 2.5 ⁵	-0.28	0.00	0.28	ns
RSDS	RSDS 2.5 ⁵	-0.25	0.02	0.30	ns
LVPECL33	LVPECL 3.3 ⁵	-0.37	-0.10	0.18	ns
HSTL18_I	HSTL_18 class I 8mA drive	-0.17	0.13	0.43	ns
HSTL18_II	HSTL_18 class II	-0.29	0.00	0.29	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	-0.17	0.13	0.43	ns
HSTL18D_II	Differential HSTL 18 class II	-0.29	0.00	0.29	ns

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
For Top and Bottom Edges of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
P[Edge] [n+4]	A	DQ
	B	DQ

Notes:

1. "n" is a row PIC number.
2. The DDR interface is designed for memories that support one DQS strobe up to 16 bits of data for the left and right edges and up to 18 bits of data for the top and bottom edges. In some packages, all the potential DDR data (DQ) pins may not be available. PIC numbering definitions are provided in the "Signal Names" column of the Signal Descriptions table.

Pin Information Summary (Cont.)

Pin Type		XP2-5				XP2-8				XP2-17			XP2-30			XP2-40	
		132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
PCI capable I/Os Bonding Out per Bank	Bank0	18	20	20	26	18	20	20	28	20	28	52	28	52	70	52	70
	Bank1	4	6	18	18	4	6	18	22	18	22	36	22	36	54	36	70
	Bank2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank4	8	8	18	18	8	8	18	26	18	26	36	26	38	54	38	70
	Bank5	14	18	20	24	14	18	20	24	20	24	52	24	53	70	53	70
	Bank6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

Logic Signal Connections

Package pinout information can be found under “Data Sheets” on the LatticeXP2 product page of the Lattice website at www.latticesemi.com/products/fpga/xp2 and in the Lattice Diamond design software.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Lattice [Thermal Management](#) document to find the device/package specific thermal values.

For Further Information

- TN1139, [Power Estimation and Management for LatticeXP2 Devices](#)
- Power Calculator tool is included with the Lattice Diamond design tool or as a standalone download from www.latticesemi.com/products/designsoftware

Lead-Free Packaging
Commercial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5MN132C	1.2V	-5	Lead-Free csBGA	132	COM	5
LFXP2-5E-6MN132C	1.2V	-6	Lead-Free csBGA	132	COM	5
LFXP2-5E-7MN132C	1.2V	-7	Lead-Free csBGA	132	COM	5
LFXP2-5E-5TN144C	1.2V	-5	Lead-Free TQFP	144	COM	5
LFXP2-5E-6TN144C	1.2V	-6	Lead-Free TQFP	144	COM	5
LFXP2-5E-7TN144C	1.2V	-7	Lead-Free TQFP	144	COM	5
LFXP2-5E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	5
LFXP2-5E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	5
LFXP2-5E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	5
LFXP2-5E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	5
LFXP2-5E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	5
LFXP2-5E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5MN132C	1.2V	-5	Lead-Free csBGA	132	COM	8
LFXP2-8E-6MN132C	1.2V	-6	Lead-Free csBGA	132	COM	8
LFXP2-8E-7MN132C	1.2V	-7	Lead-Free csBGA	132	COM	8
LFXP2-8E-5TN144C	1.2V	-5	Lead-Free TQFP	144	COM	8
LFXP2-8E-6TN144C	1.2V	-6	Lead-Free TQFP	144	COM	8
LFXP2-8E-7TN144C	1.2V	-7	Lead-Free TQFP	144	COM	8
LFXP2-8E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	8
LFXP2-8E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	8
LFXP2-8E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	8
LFXP2-8E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	8
LFXP2-8E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	8
LFXP2-8E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	17
LFXP2-17E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	17
LFXP2-17E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	17
LFXP2-17E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	17
LFXP2-17E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	17
LFXP2-17E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	17
LFXP2-17E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	17
LFXP2-17E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	17
LFXP2-17E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	17

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5QN208I	1.2V	-5	Lead-Free PQFP	208	IND	17
LFXP2-17E-6QN208I	1.2V	-6	Lead-Free PQFP	208	IND	17
LFXP2-17E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	17
LFXP2-17E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	17
LFXP2-17E-5FN484I	1.2V	-5	Lead-Free fpBGA	484	IND	17
LFXP2-17E-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	17

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-30E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	30
LFXP2-30E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	30
LFXP2-30E-5FN484I	1.2V	-5	Lead-Free fpBGA	484	IND	30
LFXP2-30E-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	30
LFXP2-30E-5FN672I	1.2V	-5	Lead-Free fpBGA	672	IND	30
LFXP2-30E-6FN672I	1.2V	-6	Lead-Free fpBGA	672	IND	30

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5FN484I	1.2V	-5	Lead-Free fpBGA	484	IND	40
LFXP2-40E-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	40
LFXP2-40E-5FN672I	1.2V	-5	Lead-Free fpBGA	672	IND	40
LFXP2-40E-6FN672I	1.2V	-6	Lead-Free fpBGA	672	IND	40

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5F484I	1.2V	-5	fpBGA	484	IND	40
LFXP2-40E-6F484I	1.2V	-6	fpBGA	484	IND	40
LFXP2-40E-5F672I	1.2V	-5	fpBGA	672	IND	40
LFXP2-40E-6F672I	1.2V	-6	fpBGA	672	IND	40