# Lattice Semiconductor Corporation - LFXP2-30E-6F484C Datasheet


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

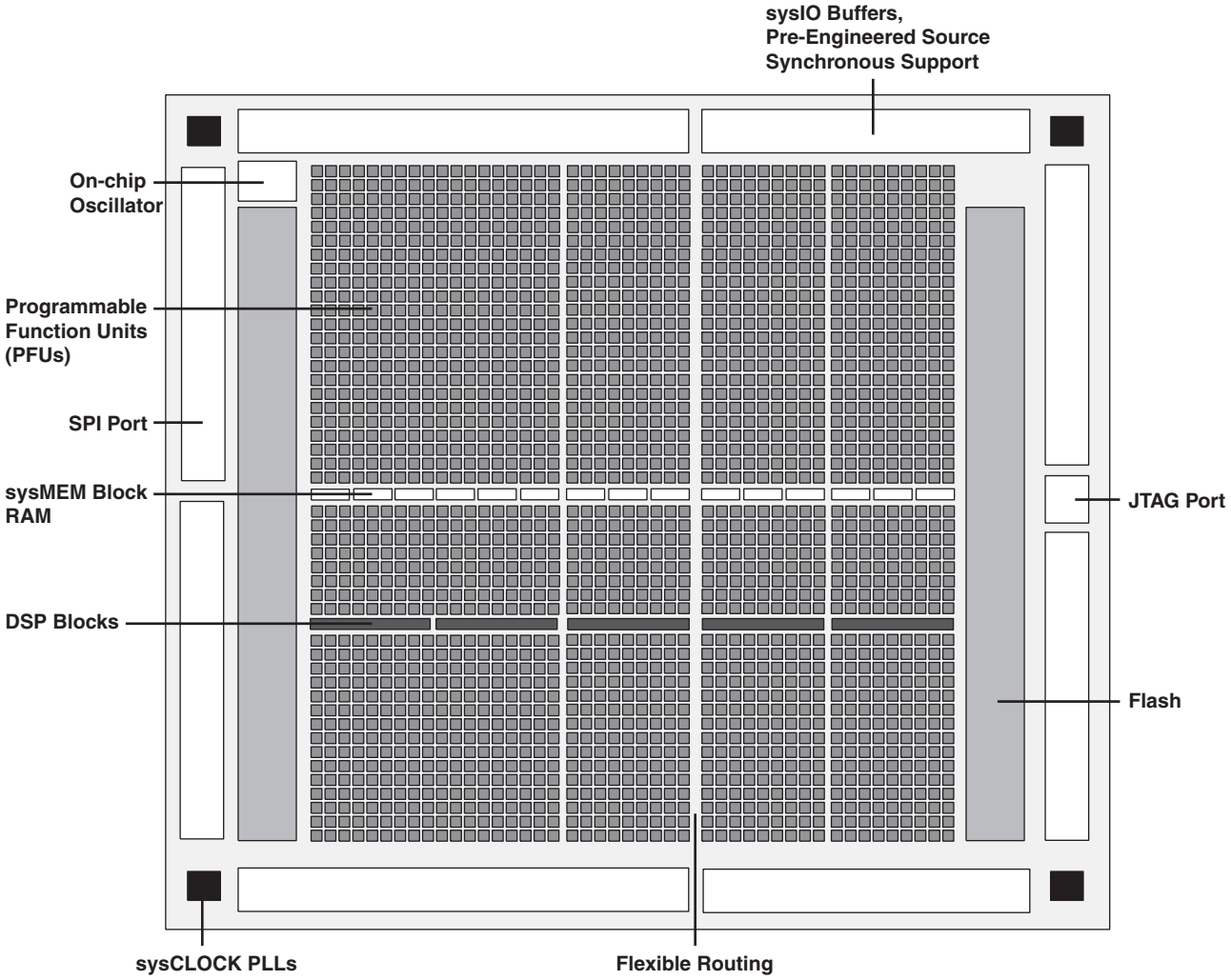
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 3625 |
| Number of Logic Elements/Cells | 29000 |
| Total RAM Bits | 396288 |
| Number of I/O | 363 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-30e-6f484c |

*Figure 2-1. Simplified Block Diagram, LatticeXP2-17 Device (Top Level)*




## PFU Blocks

The core of the LatticeXP2 device is made up of logic blocks in two forms, PFUs and PFFs. PFUs can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. PFF blocks can be programmed to perform logic, arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered Slice 0 through Slice 3, as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

## sysMEM Memory

LatticeXP2 devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of 18 Kbit RAM with dedicated input and output registers.

### sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-5. FIFOs can be implemented in sysMEM EBR blocks by using support logic with PFUs. The EBR block supports an optional parity bit for each data byte to facilitate parity checking. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths.

***Table 2-5. sysMEM Block Configurations***

| Memory Mode | Configurations |
|---|---|
| Single Port | 16,384 x 1<br>8,192 x 2<br>4,096 x 4<br>2,048 x 9<br>1,024 x 18<br>512 x 36 |
| True Dual Port | 16,384 x 1<br>8,192 x 2<br>4,096 x 4<br>2,048 x 9<br>1,024 x 18 |
| Pseudo Dual Port | 16,384 x 1<br>8,192 x 2<br>4,096 x 4<br>2,048 x 9<br>1,024 x 18<br>512 x 36 |

### Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

### FlashBAK EBR Content Storage

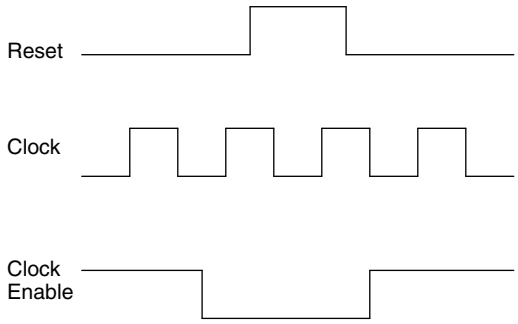
All the EBR memory in the LatticeXP2 is shadowed by Flash memory. Optionally, initialization values for the memory blocks can be defined using the Lattice Diamond design tools. The initialization values are loaded into the Flash memory during device programming and into the SRAM at power up or whenever the device is reconfigured. This feature is ideal for the storage of a variety of information such as look-up tables and microprocessor code. It is also possible to write the current contents of the EBR memory back to Flash memory. This capability is useful for the storage of data such as error codes and calibration information. For additional information on the FlashBAK capability see TN1137, LatticeXP2 Memory Usage Guide.

For further information on the sysMEM EBR block, please see TN1137, LatticeXP2 Memory Usage Guide.

### EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the low-to-high transition of the reset signal, as shown in Figure 2-18. The GSR input to the EBR is always asynchronous.

***Figure 2-18. EBR Asynchronous Reset (Including GSR) Timing Diagram***




If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

## sysDSP™ Block

The LatticeXP2 family provides a sysDSP block making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications include Bit Correlators, Fast Fourier Transform (FFT) functions, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

### sysDSP Block Approach Compare to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeXP2 family, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-19 compares the fully serial and the mixed parallel and serial implementations.

### IPexpress™

The user can access the sysDSP block via the Lattice IPexpress tool, which provides the option to configure each DSP module (or group of modules), or by direct HDL instantiation. In addition, Lattice has partnered with The MathWorks® to support instantiation in the Simulink® tool, a graphical simulation environment. Simulink works with Diamond to dramatically shorten the DSP design cycle in Lattice FPGAs.

## Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LatticeXP2 DSP include the Bit Correlator, FFT functions, FIR Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IP cores.

### Resources Available in the LatticeXP2 Family

Table 2-8 shows the maximum number of multipliers for each member of the LatticeXP2 family. Table 2-9 shows the maximum available EBR RAM Blocks and Serial TAG Memory bits in each LatticeXP2 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

***Table 2-8. Maximum Number of DSP Blocks in the LatticeXP2 Family***

| Device | DSP Block | 9x9 Multiplier | 18x18 Multiplier | 36x36 Multiplier |
|---|---|---|---|---|
| XP2-5 | 3 | 24 | 12 | 3 |
| XP2-8 | 4 | 32 | 16 | 4 |
| XP2-17 | 5 | 40 | 20 | 5 |
| XP2-30 | 7 | 56 | 28 | 7 |
| XP2-40 | 8 | 64 | 32 | 8 |

***Table 2-9. Embedded SRAM/TAG Memory in the LatticeXP2 Family***

| Device | EBR SRAM Block | Total EBR SRAM (Kbits) | TAG Memory (Bits) |
|---|---|---|---|
| XP2-5 | 9 | 166 | 632 |
| XP2-8 | 12 | 221 | 768 |
| XP2-17 | 15 | 276 | 2184 |
| XP2-30 | 21 | 387 | 2640 |
| XP2-40 | 48 | 885 | 3384 |

### LatticeXP2 DSP Performance

Table 2-10 lists the maximum performance in Millions of MAC (MMAC) operations per second for each member of the LatticeXP2 family.

***Table 2-10. DSP Performance***

| Device | DSP Block | DSP Performance MMAC |
|---|---|---|
| XP2-5 | 3 | 3,900 |
| XP2-8 | 4 | 5,200 |
| XP2-17 | 5 | 6,500 |
| XP2-30 | 7 | 9,100 |
| XP2-40 | 8 | 10,400 |

For further information on the sysDSP block, please see TN1140, LatticeXP2 sysDSP Usage Guide.

## DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock, referred to as DQS, is not free-running, and this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only, as shown in Figure 2-30) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figure 2-30 and Figure 2-31 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of 6-bit bus calibration signals from two dedicated DLLs (DDR_DLL) on opposite sides of the device. Each DLL compensates DQS delays in its half of the device as shown in Figure 2-30. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

***Figure 2-30. Edge Clock, DLL Calibration and DQS Local Bus Distribution***

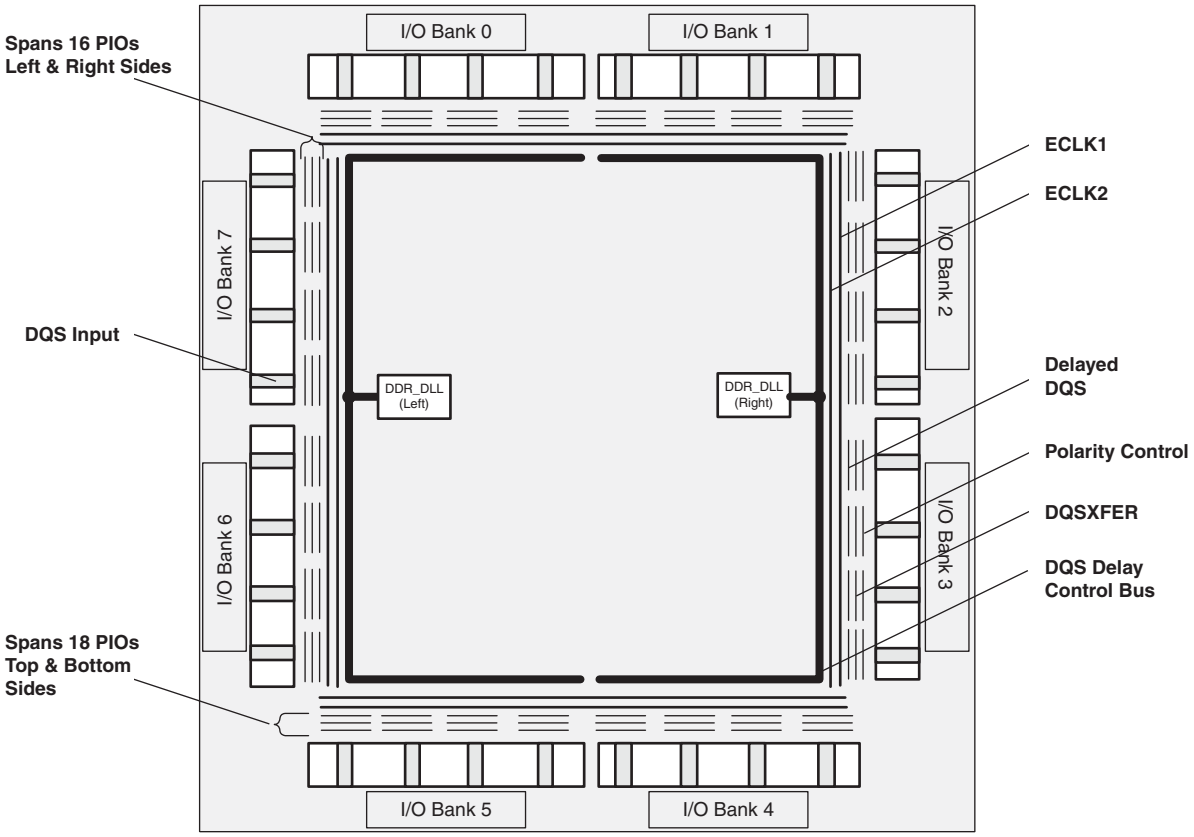
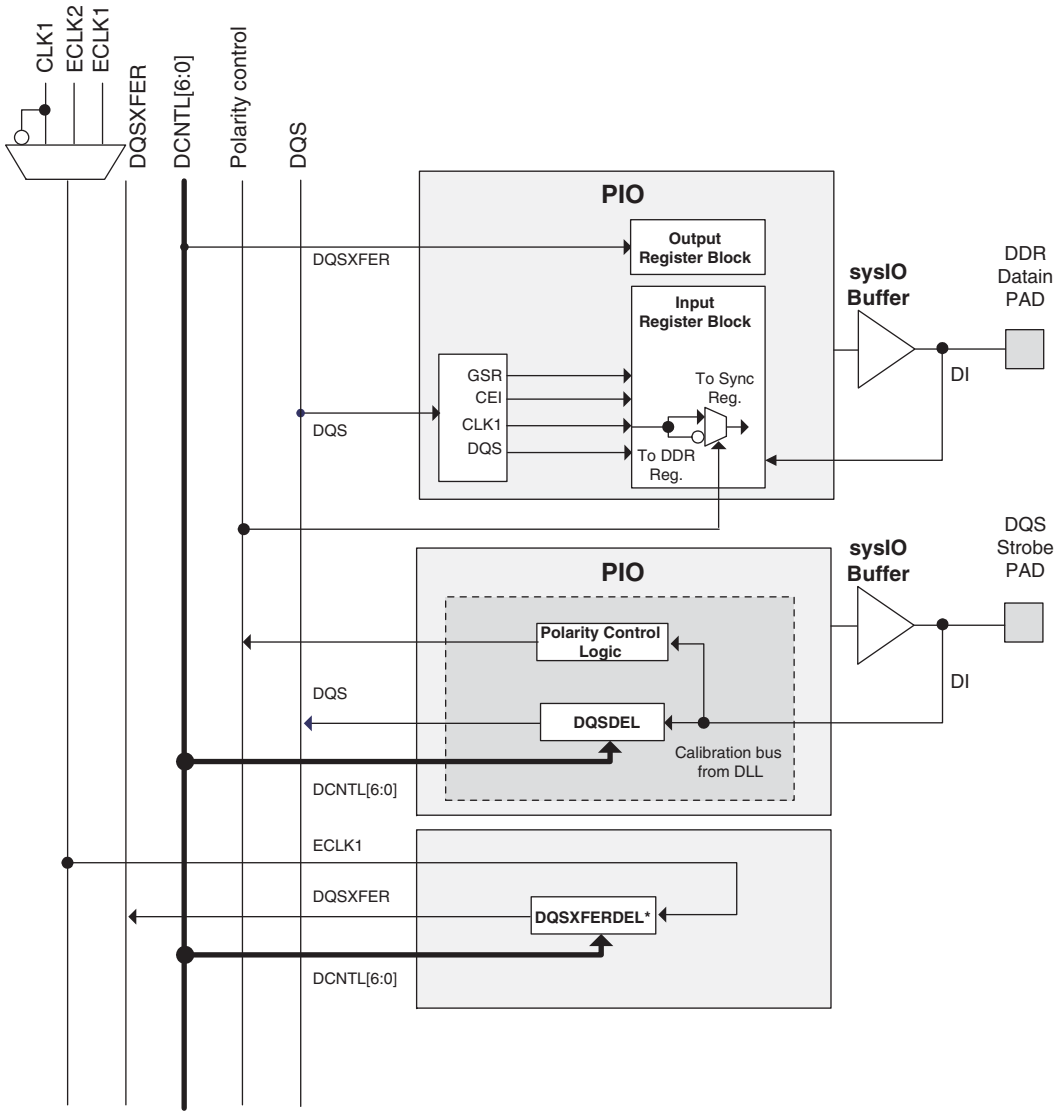


*Figure 2-31. DQS Local Bus*




*DQSXFERDEL shifts ECLK1 by 90% and is not associated with a particular PIO.

## Polarity Control Logic

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeXP2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block and requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

LatticeXP2 devices contain two types of sysIO buffer pairs.

1. **Top and Bottom (Banks 0, 1, 4 and 5) sysIO Buffer Pairs (Single-Ended Outputs Only)**
   The sysIO buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   Only the I/Os on the top and bottom banks have programmable PCI clamps.

2. **Left and Right (Banks 2, 3, 6 and 7) sysIO Buffer Pairs (50% Differential and 100% Single-Ended Outputs)**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp pad is associated with the negative side of the differential I/O.

   LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

## Typical sysIO I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when $V_{CC}$, $V_{CCCONFIG}$ ($V_{CCIO7}$) and $V_{CCAUX}$ have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other $V_{CCIO}$ banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. During power up and before the FPGA core logic becomes active, all user I/Os will be high-impedance with weak pull-up. Please refer to TN1136, LatticeXP2 sysIO Usage Guide for additional information.

The $V_{CC}$ and $V_{CCAUX}$ supply the power to the FPGA core fabric, whereas the $V_{CCIO}$ supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. $V_{CCIO}$ supplies should be powered-up before or together with the $V_{CC}$ and $V_{CCAUX}$ supplies.

## Supported sysIO Standards

The LatticeXP2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8V, 2.5V and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, MLVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-12 and 2-13 show the I/O standards (together with their supply and reference voltages) supported by LatticeXP2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1136, LatticeXP2 sysIO Usage Guide.

*Table 2-12. Supported Input Standards*

| Input Standard | $V_{REF}$ (Nom.) | $V_{CCIO}$[1] (Nom.) |
|---|---|---|
| **Single Ended Interfaces** | | |
| LVTTL | — | — |
| LVCMOS33 | — | — |
| LVCMOS25 | — | — |
| LVCMOS18 | — | 1.8 |
| LVCMOS15 | — | 1.5 |
| LVCMOS12 | — | — |
| PCI33 | — | — |
| HSTL18 Class I, II | 0.9 | — |
| HSTL15 Class I | 0.75 | — |
| SSTL33 Class I, II | 1.5 | — |
| SSTL25 Class I, II | 1.25 | — |
| SSTL18 Class I, II | 0.9 | — |
| **Differential Interfaces** | | |
| Differential SSTL18 Class I, II | — | — |
| Differential SSTL25 Class I, II | — | — |
| Differential SSTL33 Class I, II | — | — |
| Differential HSTL15 Class I | — | — |
| Differential HSTL18 Class I, II | — | — |
| LVDS, MLVDS, LVPECL, BLVDS, RSDS | — | — |

1. When not specified, $V_{CCIO}$ can be set anywhere in the valid operating range (page 3-1).

*Table 2-13. Supported Output Standards*

| Output Standard | Drive | $V_{CCIO}$ (Nom.) |
|---|---|---|
| **Single-ended Interfaces** | | |
| LVTTL | 4mA, 8mA, 12mA, 16mA, 20mA | 3.3 |
| LVCMOS33 | 4mA, 8mA, 12mA 16mA, 20mA | 3.3 |
| LVCMOS25 | 4mA, 8mA, 12mA, 16mA, 20mA | 2.5 |
| LVCMOS18 | 4mA, 8mA, 12mA, 16mA | 1.8 |
| LVCMOS15 | 4mA, 8mA | 1.5 |
| LVCMOS12 | 2mA, 6mA | 1.2 |
| LVCMOS33, Open Drain | 4mA, 8mA, 12mA 16mA, 20mA | — |
| LVCMOS25, Open Drain | 4mA, 8mA, 12mA 16mA, 20mA | — |
| LVCMOS18, Open Drain | 4mA, 8mA, 12mA 16mA | — |
| LVCMOS15, Open Drain | 4mA, 8mA | — |
| LVCMOS12, Open Drain | 2mA, 6mA | — |
| PCI33 | N/A | 3.3 |
| HSTL18 Class I, II | N/A | 1.8 |
| HSTL15 Class I | N/A | 1.5 |
| SSTL33 Class I, II | N/A | 3.3 |
| SSTL25 Class I, II | N/A | 2.5 |
| SSTL18 Class I, II | N/A | 1.8 |
| **Differential Interfaces** | | |
| Differential SSTL33, Class I, II | N/A | 3.3 |
| Differential SSTL25, Class I, II | N/A | 2.5 |
| Differential SSTL18, Class I, II | N/A | 1.8 |
| Differential HSTL18, Class I, II | N/A | 1.8 |
| Differential HSTL15, Class I | N/A | 1.5 |
| LVDS[1, 2] | N/A | 2.5 |
| MLVDS[1] | N/A | 2.5 |
| BLVDS[1] | N/A | 2.5 |
| LVPECL[1] | N/A | 3.3 |
| RSDS[1] | N/A | 2.5 |
| LVCMOS33D[1] | 4mA, 8mA, 12mA, 16mA, 20mA | 3.3 |

1. Emulated with external resistors.
2. On the left and right edges, LVDS outputs are supported with a dedicated differential output driver on 50% of the I/Os. This solution does not require external resistors at the driver.

## Hot Socketing

LatticeXP2 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the LatticeXP2 ideal for many multiple power supply and hot-swap applications.

# IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeXP2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in

original backup configuration and try again. This all can be done without power cycling the system. For more information please see TN1220, LatticeXP2 Dual Boot Feature.

For more information on device configuration, please see TN1141, LatticeXP2 sysCONFIG Usage Guide.

## Soft Error Detect (SED) Support

LatticeXP2 devices have dedicated logic to perform Cyclic Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, LatticeXP2 devices can be programmed for checking soft errors in SRAM. SED can be run on a programmed device when the user logic is not active. In the event a soft error occurs, the device can be programmed to either reload from a known good boot image (from internal Flash or external SPI memory) or generate an error signal.

For further information on SED support, please see TN1130, LatticeXP2 Soft Error Detection (SED) Usage Guide.

## On-Chip Oscillator

Every LatticeXP2 device has an internal CMOS oscillator that is used to derive a Master Clock (CCLK) for configuration. The oscillator and CCLK run continuously and are available to user logic after configuration is complete. The available CCLK frequencies are listed in Table 2-14. When a different CCLK frequency is selected during the design process, the following sequence takes place:

1. Device powers up with the default CCLK frequency.
2. During configuration, users select a different CCLK frequency.
3. CCLK frequency changes to the selected frequency after clock configuration bits are received.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1141, LatticeXP2 sysCONFIG Usage Guide.

***Table 2-14. Selectable CCLKs and Oscillator Frequencies During Configuration and User Mode***

| CCLK/Oscillator (MHz) |
|---|
| 2.5[1] |
| 3.1[2] |
| 4.3 |
| 5.4 |
| 6.9 |
| 8.1 |
| 9.2 |
| 10 |
| 13 |
| 15 |
| 20 |
| 26 |
| 32 |
| 40 |
| 54 |
| 80[3] |
| 163[3] |

1. Software default oscillator frequency.
2. Software default CCLK frequency.
3. Frequency not valid for CCLK.

## Initialization Supply Current[1, 2, 3, 4, 5]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typical (25°C, Max. Supply)[6] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply Current | XP2-5 | 20 | mA |
| | | XP2-8 | 21 | mA |
| | | XP2-17 | 44 | mA |
| | | XP2-30 | 58 | mA |
| | | XP2-40 | 62 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply Current[7] | XP2-5 | 67 | mA |
| | | XP2-8 | 74 | mA |
| | | XP2-17 | 112 | mA |
| | | XP2-30 | 124 | mA |
| | | XP2-40 | 130 | mA |
| $I_{CCPLL}$ | PLL Power Supply Current (per PLL) | | 1.8 | mA |
| $I_{CCIO}$ | Bank Power Supply Current (per Bank) | | 6.4 | mA |
| $I_{CCJ}$ | VCCJ Power Supply Current | | 1.2 | mA |

1. For further information on supply current, please see TN1139, Power Estimation and Management for LatticeXP2 Devices.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
3. Frequency 0 MHz.
4. Does not include additional current from bypass or decoupling capacitor across the supply.
5. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.
6. $T_J$ = 25°C, power supplies at nominal voltage.
7. In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of $I_{CCAUX}$ and $I_{CCPLL}$. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.

*Table 3-1. LVDS25E DC Conditions*

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $V_{CCIO}$ | Output Driver Supply (+/-5%) | 2.50 | V |
| $Z_{OUT}$ | Driver Impedance | 20 | Ω |
| $R_S$ | Driver Series Resistor (+/-1%) | 158 | Ω |
| $R_P$ | Driver Parallel Resistor (+/-1%) | 140 | Ω |
| $R_T$ | Receiver Termination (+/-1%) | 100 | Ω |
| $V_{OH}$ | Output High Voltage (after $R_P$) | 1.43 | V |
| $V_{OL}$ | Output Low Voltage (after $R_P$) | 1.07 | V |
| $V_{OD}$ | Output Differential Voltage (After $R_P$) | 0.35 | V |
| $V_{CM}$ | Output Common Mode Voltage | 1.25 | V |
| $Z_{BACK}$ | Back Impedance | 100.5 | Ω |
| $I_{DC}$ | DC Output Current | 6.03 | mA |

## LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3V VCCIO. The default drive current for LVCMOS33D output is 12mA with the option to change the device strength to 4mA, 8mA, 16mA or 20mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

## LVPECL

The LatticeXP2 devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

***Figure 3-3. Differential LVPECL***

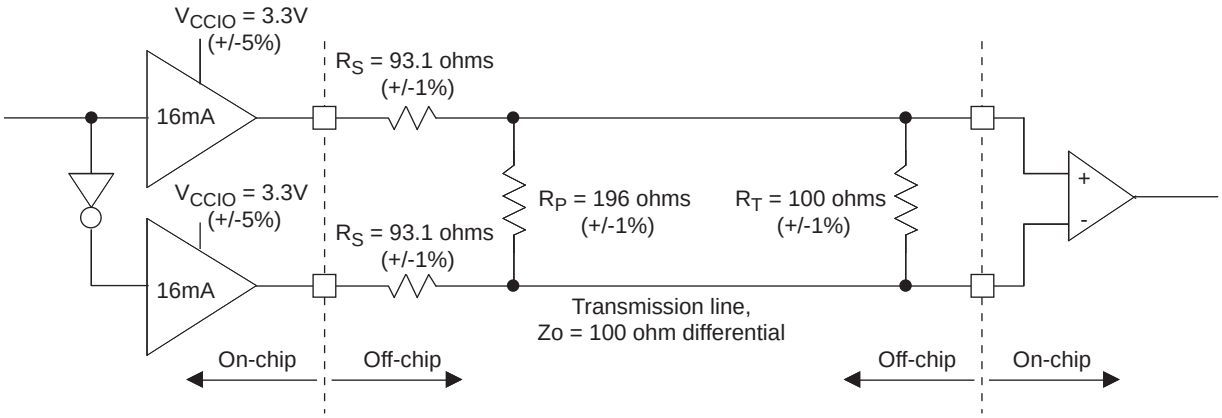



***Table 3-3. LVPECL DC Conditions[1]***

**Over Recommended Operating Conditions**

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $V_{CCIO}$ | Output Driver Supply (+/-5%) | 3.30 | V |
| $Z_{OUT}$ | Driver Impedance | 10 | Ω |
| $R_S$ | Driver Series Resistor (+/-1%) | 93 | Ω |
| $R_P$ | Driver Parallel Resistor (+/-1%) | 196 | Ω |
| $R_T$ | Receiver Termination (+/-1%) | 100 | Ω |
| $V_{OH}$ | Output High Voltage (After $R_P$) | 2.05 | V |
| $V_{OL}$ | Output Low Voltage (After $R_P$) | 1.25 | V |
| $V_{OD}$ | Output Differential Voltage (After $R_P$) | 0.80 | V |
| $V_{CM}$ | Output Common Mode Voltage | 1.65 | V |
| $Z_{BACK}$ | Back Impedance | 100.5 | Ω |
| $I_{DC}$ | DC Output Current | 12.11 | mA |

1. For input buffer, see LVDS table.

## Register-to-Register Performance (Continued)

| Function | -7 Timing | Units |
|---|---|---|
| **DSP IP Functions** | | |
| 16-Tap Fully-Parallel FIR Filter | 198 | MHz |
| 1024-pt FFT | 221 | MHz |
| 8X8 Matrix Multiplication | 196 | MHz |

1. These timing numbers were generated using the ispLEVER design tool. Exact performance may vary with device, design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

# Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

# LatticeXP2 External Switching Characteristics (Continued)

**Over Recommended Operating Conditions**

| Parameter | Description | Device | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{HE}$ | Clock to Data Hold - PIO Input Register | XP2-5 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-8 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-17 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-30 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| | | XP2-40 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| $t_{SU\_DELE}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | XP2-5 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-8 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-17 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-30 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| | | XP2-40 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| $t_{H\_DELE}$ | Clock to Data Hold - PIO Input Register with Input Data Delay | XP2-5 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-8 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-17 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-30 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-40 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| $f_{MAX\_IOE}$ | Clock Frequency of I/O and PFU Register | XP2 | — | 420 | — | 357 | — | 311 | MHz |
| **General I/O Pin Parameters (using Primary Clock with PLL)**[1] | | | | | | | | | |
| $t_{COPLL}$ | Clock to Output - PIO Output Register | XP2-5 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| | | XP2-8 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| | | XP2-17 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| | | XP2-30 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| | | XP2-40 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| $t_{SUPLL}$ | Clock to Data Setup - PIO Input Register | XP2-5 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-8 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-17 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-30 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-40 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | XP2-5 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | XP2-8 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | XP2-17 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | XP2-30 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-40 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| $t_{SU\_DELPLL}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | XP2-5 | 1.90 | — | 2.10 | — | 2.30 | — | ns |
| | | XP2-8 | 1.90 | — | 2.10 | — | 2.30 | — | ns |
| | | XP2-17 | 1.90 | — | 2.10 | — | 2.30 | — | ns |
| | | XP2-30 | 2.00 | — | 2.20 | — | 2.40 | — | ns |
| | | XP2-40 | 2.00 | — | 2.20 | — | 2.40 | — | ns |

# LatticeXP2 Internal Switching Characteristics[1]

**Over Recommended Operating Conditions**

| Parameter | Description | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **PFU/PFF Logic Mode Timing** | | | | | | | | |
| $t_{LUT4\_PFU}$ | LUT4 delay (A to D inputs to F output) | — | 0.216 | — | 0.238 | — | 0.260 | ns |
| $t_{LUT6\_PFU}$ | LUT6 delay (A to D inputs to OFX output) | — | 0.304 | — | 0.399 | — | 0.494 | ns |
| $t_{LSR\_PFU}$ | Set/Reset to output of PFU (Asynchronous) | — | 0.720 | — | 0.769 | — | 0.818 | ns |
| $t_{SUM\_PFU}$ | Clock to Mux (M0,M1) Input Setup Time | 0.154 | — | 0.151 | — | 0.148 | — | ns |
| $t_{HM\_PFU}$ | Clock to Mux (M0,M1) Input Hold Time | -0.061 | — | -0.057 | — | -0.053 | — | ns |
| $t_{SUD\_PFU}$ | Clock to D input setup time | 0.061 | — | 0.077 | — | 0.093 | — | ns |
| $t_{HD\_PFU}$ | Clock to D input hold time | 0.002 | — | 0.003 | — | 0.003 | — | ns |
| $t_{CK2Q\_PFU}$ | Clock to Q delay, (D-type Register Configuration) | — | 0.342 | — | 0.363 | — | 0.383 | ns |
| $t_{RSTREC\_PFU}$ | Asynchronous reset recovery time for PFU Logic | — | 0.520 | — | 0.634 | — | 0.748 | ns |
| $t_{RST\_PFU}$ | Asynchronous reset time for PFU Logic | — | 0.720 | — | 0.769 | — | 0.818 | ns |
| **PFU Dual Port Memory Mode Timing** | | | | | | | | |
| $t_{CORAM\_PFU}$ | Clock to Output (F Port) | — | 1.082 | — | 1.267 | — | 1.452 | ns |
| $t_{SUDATA\_PFU}$ | Data Setup Time | -0.206 | — | -0.240 | — | -0.274 | — | ns |
| $t_{HDATA\_PFU}$ | Data Hold Time | 0.239 | — | 0.275 | — | 0.312 | — | ns |
| $t_{SUADDR\_PFU}$ | Address Setup Time | -0.294 | — | -0.333 | — | -0.371 | — | ns |
| $t_{HADDR\_PFU}$ | Address Hold Time | 0.295 | — | 0.333 | — | 0.371 | — | ns |
| $t_{SUWREN\_PFU}$ | Write/Read Enable Setup Time | -0.146 | — | -0.169 | — | -0.193 | — | ns |
| $t_{HWREN\_PFU}$ | Write/Read Enable Hold Time | 0.158 | — | 0.182 | — | 0.207 | — | ns |
| **PIO Input/Output Buffer Timing** | | | | | | | | |
| $t_{IN\_PIO}$ | Input Buffer Delay (LVCMOS25) | — | 0.858 | — | 0.766 | — | 0.674 | ns |
| $t_{OUT\_PIO}$ | Output Buffer Delay (LVCMOS25) | — | 1.561 | — | 1.403 | — | 1.246 | ns |
| **IOLOGIC Input/Output Timing** | | | | | | | | |
| $t_{SUI\_PIO}$ | Input Register Setup Time (Data Before Clock) | 0.583 | — | 0.893 | — | 1.201 | — | ns |
| $t_{HI\_PIO}$ | Input Register Hold Time (Data after Clock) | 0.062 | — | 0.322 | — | 0.482 | — | ns |
| $t_{COO\_PIO}$ | Output Register Clock to Output Delay | — | 0.608 | — | 0.661 | — | 0.715 | ns |
| $t_{SUCE\_PIO}$ | Input Register Clock Enable Setup Time | 0.032 | — | 0.037 | — | 0.041 | — | ns |
| $t_{HCE\_PIO}$ | Input Register Clock Enable Hold Time | -0.022 | — | -0.025 | — | -0.028 | — | ns |
| $t_{SULSR\_PIO}$ | Set/Reset Setup Time | 0.184 | — | 0.201 | — | 0.217 | — | ns |
| $t_{HLSR\_PIO}$ | Set/Reset Hold Time | -0.080 | — | -0.086 | — | -0.093 | — | ns |
| $t_{RSTREC\_PIO}$ | Asynchronous reset recovery time for IO Logic | 0.228 | — | 0.247 | — | 0.266 | — | ns |

# sysCLOCK PLL Timing

**Over Recommended Operating Conditions**

| Parameter | Description | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Clock Frequency (CLKI, CLKFB) | | 10 | — | 435 | MHz |
| $f_{OUT}$ | Output Clock Frequency (CLKOP, CLKOS) | | 10 | — | 435 | MHz |
| $f_{OUT2}$ | K-Divider Output Frequency | CLKOK | 0.078 | — | 217.5 | MHz |
| | | CLKOK2 | 3.3 | — | 145 | MHz |
| $f_{VCO}$ | PLL VCO Frequency | | 435 | — | 870 | MHz |
| $f_{PFD}$ | Phase Detector Input Frequency | | 10 | — | 435 | MHz |
| **AC Characteristics** | | | | | | |
| $t_{DT}$ | Output Clock Duty Cycle | Default duty cycle selected [3] | 45 | 50 | 55 | % |
| $t_{CPA}$ | Coarse Phase Adjust | | -5 | 0 | 5 | % |
| $t_{PH}$ [4] | Output Phase Accuracy | | -5 | 0 | 5 | % |
| $t_{OPJIT}$ [1] | Output Clock Period Jitter | $f_{OUT}$ > 400 MHz | — | — | ±50 | ps |
| | | 100 MHz < $f_{OUT}$ < 400 MHz | — | — | ±125 | ps |
| | | $f_{OUT}$ < 100 MHz | — | — | 0.025 | UIPP |
| $t_{SK}$ | Input Clock to Output Clock Skew | N/M = integer | — | — | ±240 | ps |
| $t_{OPW}$ | Output Clock Pulse Width | At 90% or 10% | 1 | — | — | ns |
| $t_{LOCK}$ [2] | PLL Lock-in Time | 25 to 435 MHz | — | — | 50 | µs |
| | | 10 to 25 MHz | — | — | 100 | µs |
| $t_{IPJIT}$ | Input Clock Period Jitter | | — | — | ±200 | ps |
| $t_{FBKDLY}$ | External Feedback Delay | | — | — | 10 | ns |
| $t_{HI}$ | Input Clock High Time | 90% to 90% | 0.5 | — | — | ns |
| $t_{LO}$ | Input Clock Low Time | 10% to 10% | 0.5 | — | — | ns |
| $t_{RSTKW}$ | Reset Signal Pulse Width (RSTK) | | 10 | — | — | ns |
| $t_{RSTW}$ | Reset Signal Pulse Width (RST) | | 500 | — | — | ns |

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.
2. Output clock is valid after $t_{LOCK}$ for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. Relative to CLKOP.

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-17E-5QN208I | 1.2V | -5 | Lead-Free PQFP | 208 | IND | 17 |
| LFXP2-17E-6QN208I | 1.2V | -6 | Lead-Free PQFP | 208 | IND | 17 |
| LFXP2-17E-5FTN256I | 1.2V | -5 | Lead-Free ftBGA | 256 | IND | 17 |
| LFXP2-17E-6FTN256I | 1.2V | -6 | Lead-Free ftBGA | 256 | IND | 17 |
| LFXP2-17E-5FN484I | 1.2V | -5 | Lead-Free fpBGA | 484 | IND | 17 |
| LFXP2-17E-6FN484I | 1.2V | -6 | Lead-Free fpBGA | 484 | IND | 17 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-30E-5FTN256I | 1.2V | -5 | Lead-Free ftBGA | 256 | IND | 30 |
| LFXP2-30E-6FTN256I | 1.2V | -6 | Lead-Free ftBGA | 256 | IND | 30 |
| LFXP2-30E-5FN484I | 1.2V | -5 | Lead-Free fpBGA | 484 | IND | 30 |
| LFXP2-30E-6FN484I | 1.2V | -6 | Lead-Free fpBGA | 484 | IND | 30 |
| LFXP2-30E-5FN672I | 1.2V | -5 | Lead-Free fpBGA | 672 | IND | 30 |
| LFXP2-30E-6FN672I | 1.2V | -6 | Lead-Free fpBGA | 672 | IND | 30 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-40E-5FN484I | 1.2V | -5 | Lead-Free fpBGA | 484 | IND | 40 |
| LFXP2-40E-6FN484I | 1.2V | -6 | Lead-Free fpBGA | 484 | IND | 40 |
| LFXP2-40E-5FN672I | 1.2V | -5 | Lead-Free fpBGA | 672 | IND | 40 |
| LFXP2-40E-6FN672I | 1.2V | -6 | Lead-Free fpBGA | 672 | IND | 40 |

## Conventional Packaging

**Commercial**

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-5E-5M132C | 1.2V | -5 | csBGA | 132 | COM | 5 |
| LFXP2-5E-6M132C | 1.2V | -6 | csBGA | 132 | COM | 5 |
| LFXP2-5E-7M132C | 1.2V | -7 | csBGA | 132 | COM | 5 |
| LFXP2-5E-5FT256C | 1.2V | -5 | ftBGA | 256 | COM | 5 |
| LFXP2-5E-6FT256C | 1.2V | -6 | ftBGA | 256 | COM | 5 |
| LFXP2-5E-7FT256C | 1.2V | -7 | ftBGA | 256 | COM | 5 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-8E-5M132C | 1.2V | -5 | csBGA | 132 | COM | 8 |
| LFXP2-8E-6M132C | 1.2V | -6 | csBGA | 132 | COM | 8 |
| LFXP2-8E-7M132C | 1.2V | -7 | csBGA | 132 | COM | 8 |
| LFXP2-8E-5FT256C | 1.2V | -5 | ftBGA | 256 | COM | 8 |
| LFXP2-8E-6FT256C | 1.2V | -6 | ftBGA | 256 | COM | 8 |
| LFXP2-8E-7FT256C | 1.2V | -7 | ftBGA | 256 | COM | 8 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-17E-5FT256C | 1.2V | -5 | ftBGA | 256 | COM | 17 |
| LFXP2-17E-6FT256C | 1.2V | -6 | ftBGA | 256 | COM | 17 |
| LFXP2-17E-7FT256C | 1.2V | -7 | ftBGA | 256 | COM | 17 |
| LFXP2-17E-5F484C | 1.2V | -5 | fpBGA | 484 | COM | 17 |
| LFXP2-17E-6F484C | 1.2V | -6 | fpBGA | 484 | COM | 17 |
| LFXP2-17E-7F484C | 1.2V | -7 | fpBGA | 484 | COM | 17 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|---|---|---|---|---|---|---|
| LFXP2-30E-5FT256C | 1.2V | -5 | ftBGA | 256 | COM | 30 |
| LFXP2-30E-6FT256C | 1.2V | -6 | ftBGA | 256 | COM | 30 |
| LFXP2-30E-7FT256C | 1.2V | -7 | ftBGA | 256 | COM | 30 |
| LFXP2-30E-5F484C | 1.2V | -5 | fpBGA | 484 | COM | 30 |
| LFXP2-30E-6F484C | 1.2V | -6 | fpBGA | 484 | COM | 30 |
| LFXP2-30E-7F484C | 1.2V | -7 | fpBGA | 484 | COM | 30 |
| LFXP2-30E-5F672C | 1.2V | -5 | fpBGA | 672 | COM | 30 |
| LFXP2-30E-6F672C | 1.2V | -6 | fpBGA | 672 | COM | 30 |
| LFXP2-30E-7F672C | 1.2V | -7 | fpBGA | 672 | COM | 30 |

# LatticeXP2 Family Data Sheet Revision History

**September 2014** **Data Sheet DS1009**

## Revision History

| Date | Version | Section | Change Summary |
|---|---|---|---|
| May 2007 | 01.1 | — | Initial release. |
| September 2007 | 01.2 | DC and Switching Characteristics | Added JTAG Port Timing Waveforms diagram. |
| | | | Updated sysCLOCK PLL Timing table. |
| | | Pinout Information | Added Thermal Management text section. |
| February 2008 | 01.3 | Architecture | Added LVCMOS33D to Supported Output Standards table. |
| | | | Clarified: “This Flash can be programmed through either the JTAG or Slave SPI ports of the device. The SRAM configuration space can also be infinitely reconfigured through the JTAG and Master SPI ports.” |
| | | | Added External Slave SPI Port to Serial TAG Memory section. Updated Serial TAG Memory diagram. |
| | | DC and Switching Characteristics | Updated Flash Programming Specifications table. |
| | | | Added “8W” specification to Hot Socketing Specifications table. |
| | | | Updated Timing Tables |
| | | | Clarifications for IIH in DC Electrical Characteristics table. |
| | | | Added LVCMOS33D section |
| | | | Updated DOA and DOA (Regs) to EBR Timing diagrams. |
| | | | Removed Master Clock Frequency and Duty Cycle sections from the LatticeXP2 sysCONFIG Port Timing Specifications table. These are listed on the On-chip Oscillator and Configuration Master Clock Characteristics table. |
| | | | Changed CSSPIN to CSSPISN in description of $t_{SCS}$, $t_{SCSS}$, and $t_{SCSH}$ parameters. Removed $t_{SOE}$ parameter. |
| | | | Clarified On-chip Oscillator documentation |
| | | | Added Switching Test Conditions |
| | | Pinout Information | Added “True LVDS Pairs Bonding Out per Bank,” “DDR Banks Bonding Out per I/O Bank,” and “PCI capable I/Os Bonding Out per Bank” to Pin Information Summary in place of previous blank table “PCI and DDR Capabilities of the Device-Package Combinations” |
| | | | Removed pinout listing. This information is available on the LatticeXP2 product web pages |
| | | Ordering Information | Added XP2-17 “8W” and all other family OPNs. |
| April 2008 | 01.4 | DC and Switching Characteristics | Updated Absolute Maximum Ratings footnotes. |
| | | | Updated Recommended Operating Conditions Table footnotes. |
| | | | Updated Supply Current (Standby) Table |
| | | | Updated Initialization Supply Current Table |
| | | | Updated Programming and Erase Flash Supply Current Table |
| | | | Updated Register to Register Performance Table |
| | | | Updated LatticeXP2 External Switching Characteristics Table |
| | | | Updated LatticeXP2 Internal Switching Characteristics Table |
| | | | Updated sysCLOCK PLL Timing Table |