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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	3625
Number of Logic Elements/Cells	29000
Total RAM Bits	396288
Number of I/O	363
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-30e-6f484i

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PFU Blocks

The core of the LatticeXP2 device is made up of logic blocks in two forms, PFUs and PFFs. PFUs can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. PFF blocks can be programmed to perform logic, arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered Slice 0 through Slice 3, as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.



Figure 2-5. Clock Divider Connections



Clock Distribution Network

LatticeXP2 devices have eight quadrant-based primary clocks and between six and eight flexible region-based secondary clocks/control signals. Two high performance edge clocks are available on each edge of the device to support high speed interfaces. The clock inputs are selected from external I/Os, the sysCLOCK PLLs, or routing. Clock inputs are fed throughout the chip via the primary, secondary and edge clock networks.

Primary Clock Sources

LatticeXP2 devices derive primary clocks from four sources: PLL outputs, CLKDIV outputs, dedicated clock inputs and routing. LatticeXP2 devices have two to four sysCLOCK PLLs, located in the four corners of the device. There are eight dedicated clock inputs, two on each side of the device. Figure 2-6 shows the primary clock sources.



Figure 2-6. Primary Clock Sources for XP2-17



Note: This diagram shows sources for the XP2-17 device. Smaller LatticeXP2 devices have two GPLLs.



- In the 'Signed/Unsigned' options the operands can be switched between signed and unsigned on every cycle.
- In the 'Add/Sub' option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-20 shows the MULT sysDSP element.

Figure 2-20. MULT sysDSP Element





MAC sysDSP Element

In this case, the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers but the output register is always enabled. The output register is used to store the accumulated value. The Accumulators in the DSP blocks in LatticeXP2 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-21 shows the MAC sysDSP element.

Figure 2-21. MAC sysDSP





Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysIO buffers as shown in Figure 2-25. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysIO buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

Figure 2-25. PIC Diagram



Signals are available on left/right/bottom edges only.
 Selected blocks.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C") as shown in Figure 2-25. The PAD Labels "T" and "C" distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as inputs.



shows the diagram using this gearbox function. For more information on this topic, see TN1138, <u>LatticeXP2 High</u> <u>Speed I/O Interface</u>.







Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-27 shows the Tristate Register Block with the Output Block

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as Dtype or latch. In DDR mode, ONEG1 and OPOS1 are fed into registers on the positive edge of the clock. Then in the next clock the registered OPOS1 is latched. A multiplexer running off the same clock cycle selects the correct register for feeding to the output (D0).

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock signal is selected from general purpose routing, ECLK1, ECLK2 or a DQS signal (from the programmable DQS pin) and is provided to the input register block. The clock can optionally be inverted.

DDR Memory Support

PICs have additional circuitry to allow implementation of high speed source synchronous and DDR memory interfaces.

PICs have registered elements that support DDR memory interfaces. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the top and bottom are designed for memories that support 18 bits of data. One of every 16 PIOs on the left and right and one of every 18 PIOs on the top and bottom contain delay elements to facilitate the generation of DQS signals. The DQS signals feed the DQS buses which span the set of 16 or 18 PIOs. Figure 2-28 and Figure 2-29 show the DQS pin assignments in each set of PIOs.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. For additional information on using DDR memory support please see TN1138, <u>LatticeXP2 High Speed I/O Interface</u>.



LatticeXP2 devices contain two types of sysIO buffer pairs.

1. Top and Bottom (Banks 0, 1, 4 and 5) sysIO Buffer Pairs (Single-Ended Outputs Only)

The sysIO buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Only the I/Os on the top and bottom banks have programmable PCI clamps.

2. Left and Right (Banks 2, 3, 6 and 7) sysIO Buffer Pairs (50% Differential and 100% Single-Ended Outputs) The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp pad is associated with the negative side of the differential I/O.

LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

Typical sysIO I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when $V_{CC, V} C_{CCONFIG} (V_{CCIO7})$ and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. During power up and before the FPGA core logic becomes active, all user I/Os will be high-impedance with weak pull-up. Please refer to TN1136, <u>LatticeXP2 sysIO</u> Usage Guide for additional information.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported sysIO Standards

The LatticeXP2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8V, 2.5V and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, MLVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-12 and 2-13 show the I/O standards (together with their supply and reference voltages) supported by LatticeXP2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1136, LatticeXP2 sysIO Usage Guide.



and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards. For more information, please see TN1141, LatticeXP2 sysCONFIG Usage Guide.

flexiFLASH Device Configuration

The LatticeXP2 devices combine Flash and SRAM on a single chip to provide users with flexibility in device programming and configuration. Figure 2-33 provides an overview of the arrangement of Flash and SRAM configuration cells within the device. The remainder of this section provides an overview of these capabilities. See TN1141, LatticeXP2 sysCONFIG Usage Guide for a more detailed description.



Figure 2-33. Overview of Flash and SRAM Configuration Cells Within LatticeXP2 Devices

At power-up, or on user command, data is transferred from the on-chip Flash memory to the SRAM configuration cells that control the operation of the device. This is done with massively parallel buses enabling the parts to operate within microseconds of the power supplies reaching valid levels; this capability is referred to as Instant-On.

The on-chip Flash enables a single-chip solution eliminating the need for external boot memory. This Flash can be programmed through either the JTAG or Slave SPI ports of the device. The SRAM configuration space can also be infinitely reconfigured through the JTAG and Master SPI ports. The JTAG port is IEEE 1149.1 and IEEE 1532 compliant.

As described in the EBR section of the data sheet, the FlashBAK capability of the parts enables the contents of the EBR blocks to be written back into the Flash storage area without erasing or reprogramming other aspects of the device configuration. Serial TAG memory is also available to allow the storage of small amounts of data such as calibration coefficients and error codes.

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM only FPGAs. This is further enhanced by device locking. The device can be in one of three modes:



Density Shifting

The LatticeXP2 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.



Initialization Supply Current^{1, 2, 3, 4, 5}

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical (25°C, Max. Supply) ⁶	Units
		XP2-5	20	mA
		XP2-8	21	mA
I _{CC}	Core Power Supply Current	XP2-17	44	mA
		XP2-30	58	mA
		XP2-40	62	mA
I _{CCAUX}		XP2-5	67	mA
		XP2-8	74	mA
	Auxiliary Power Supply Current ⁷	XP2-17	112	mA
		XP2-30	124	mA
		XP2-40	130	mA
I _{CCPLL}	PLL Power Supply Current (per PLL)		1.8	mA
I _{CCIO}	Bank Power Supply Current (per Bank)		6.4	mA
ICCJ	VCCJ Power Supply Current		1.2	mA

1. For further information on supply current, please see TN1139, Power Estimation and Management for LatticeXP2 Devices.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

3. Frequency 0 MHz.

4. Does not include additional current from bypass or decoupling capacitor across the supply.

5. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.

6. $T_J = 25^{\circ}C$, power supplies at nominal voltage.

In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual
auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the
auxiliary power supply.



BLVDS

The LatticeXP2 devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.





Table 3-2. BLVDS DC Conditions¹

		Тур		
Parameter	Description	Ζο = 45 Ω	Ζο = 90 Ω	Units
V _{CCIO}	Output Driver Supply (+/- 5%)	2.50	2.50	V
Z _{OUT}	Driver Impedance	10.00	10.00	Ω
R _S	Driver Series Resistor (+/- 1%)	90.00	90.00	Ω
R _{TL}	Driver Parallel Resistor (+/- 1%)	45.00	90.00	Ω
R _{TR}	Receiver Termination (+/- 1%)	45.00	90.00	Ω
V _{OH}	Output High Voltage (After R _{TL})	1.38	1.48	V
V _{OL}	Output Low Voltage (After R _{TL})	1.12	1.02	V
V _{OD}	Output Differential Voltage (After R _{TL})	0.25	0.46	V
V _{CM}	Output Common Mode Voltage	1.25	1.25	V
I _{DC}	DC Output Current	11.24	10.20	mA

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.



LVPECL

The LatticeXP2 devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL



Table 3-3. LVPECL DC Conditions¹

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	3.30	V
Z _{OUT}	Driver Impedance	10	Ω
R _S	Driver Series Resistor (+/-1%)	93	Ω
R _P	Driver Parallel Resistor (+/-1%)	196	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage (After R _P)	2.05	V
V _{OL}	Output Low Voltage (After R _P)	1.25	V
V _{OD}	Output Differential Voltage (After R _P)	0.80	V
V _{CM}	Output Common Mode Voltage	1.65	V
Z _{BACK}	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	12.11	mA

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.



RSDS

The LatticeXP2 devices support differential RSDS standard. This standard is emulated using complementary LVC-MOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.



Figure 3-4. RSDS (Reduced Swing Differential Standard)

Table 3-4. RSDS DC Conditions¹

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/-1%)	294	Ω
R _P	Driver Parallel Resistor (+/-1%)	121	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage (After R _P)	1.35	V
V _{OL}	Output Low Voltage (After R _P)	1.15	V
V _{OD}	Output Differential Voltage (After R _P)	0.20	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	101.5	Ω
I _{DC}	DC Output Current	3.66	mA

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.



Typical Building Block Function Performance¹

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	4.4	ns
32-bit Decoder	5.2	ns
64-bit Decoder	5.6	ns
4:1 MUX	3.7	ns
8:1 MUX	3.9	ns
16:1 MUX	4.3	ns
32:1 MUX	4.5	ns

Register-to-Register Performance

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	521	MHz
32-bit Decoder	537	MHz
64-bit Decoder	484	MHz
4:1 MUX	744	MHz
8:1 MUX	678	MHz
16:1 MUX	616	MHz
32:1 MUX	529	MHz
8-bit Adder	570	MHz
16-bit Adder	507	MHz
64-bit Adder	293	MHz
16-bit Counter	541	MHz
32-bit Counter	440	MHz
64-bit Counter	321	MHz
64-bit Accumulator	261	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	315	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	315	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	231	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (One PFU)	760	MHz
32x2 Pseudo-Dual Port RAM	455	MHz
64x1 Pseudo-Dual Port RAM	351	MHz
DSP Functions		
18x18 Multiplier (All Registers)	342	MHz
9x9 Multiplier (All Registers)	342	MHz
36x36 Multiply (All Registers)	330	MHz
18x18 Multiply/Accumulate (Input and Output Registers)	218	MHz
18x18 Multiply-Add/Sub-Sum (All Registers)	292	MHz



FlashBAK Time (from EBR to Flash)

Over Recommended Operating Conditions

Device	EBR Density (Bits)	Time (Typ.)	Units
XP2-5	166K	1.5	S
XP2-8	221K	1.5	S
XP2-17	276K	1.5	S
XP2-30	387K	2.0	S
XP2-40	885K	3.0	S

JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	TCK Clock Frequency	—	25	MHz
t _{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t _{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t _{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t _{BTS}	TCK [BSCAN] setup time	8	—	ns
t _{BTH}	TCK [BSCAN] hold time	10	—	ns
t _{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t _{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t _{BTCODIS}	TAP controller falling edge of clock to valid disable	—	10	ns
t _{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t _{BTCRS}	BSCAN test capture register setup time	8	—	ns
t _{BTCRH}	BSCAN test capture register hold time	25	—	ns
t _{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
t _{BTUODIS}	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
t _{BTUPOEN}	BSCAN test update register, falling edge of clock to valid enable	_	25	ns



LatticeXP2 Family Data Sheet Pinout Information

February 2012

Data Sheet DS1009

Signal Descriptions		
Signal Name	I/O	Description
General Purpose		l
		[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).
P[Edge] [Bow/Column Number*] [A/B]	I/O	[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.
		[A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
GND		Ground. Dedicated pins.
V _{CC}		Power supply pins for core logic. Dedicated pins.
V _{CCAUX}	_	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers.
V _{CCPLL}		PLL supply pins. csBGA, PQFP and TQFP packages only.
V _{CCIOx}		Dedicated power supply pins for I/O bank x.
V _{REF1_x} , V _{REF2_x}	_	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V_{REF} inputs. When not used, they may be used as I/O pins.
PLL and Clock Functions (Used as us	er prog	ammable I/O pins when not in use for PLL or clock pins)
[LOC][num]_V _{CCPLL}		Power supply pin for PLL: LLC, LRC, URC, ULC, num = row from center.
[LOC][num]_GPLL[T, C]_IN_A	I	General Purpose PLL (GPLL) input pads: LLC, LRC, URC, ULC, num = row from center, $T = true$ and $C = complement$, index A,B,Cat each side.
[LOC][num]_GPLL[T, C]_FB_A	I	Optional feedback GPLL input pads: LLC, LRC, URC, ULC, num = row from center, $T =$ true and $C =$ complement, index A,B,Cat each side.
PCLK[T, C]_[n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and $0,1,2,3$ within bank.
[LOC]DQS[num]	I	DQS input pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = ball function number. Any pad can be configured to be output.
Test and Programming (Dedicated Pi	ns)	
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
тск	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
ТЛ	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up

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sequence). Pull-up is enabled during configuration.



Signal Descriptions (Cont.)

Signal Name	I/O	Description
TDO	0	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ		Power supply pin for JTAG Test Access Port.
Configuration Pads (Used during sysC	ONFIG)	
CFG[1:0]	Ι	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, an internal pull-up is enabled.
INITN ¹	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
SISPI ²	I/O	Input data pin in slave SPI mode and Output data pin in Master SPI mode.
SOSPI ²	I/O	Output data pin in slave SPI mode and Input data pin in Master SPI mode.
CSSPIN ²	0	Chip select for external SPI Flash memory in Master SPI mode. This pin has a weak internal pull-up.
CSSPISN	I	Chip select in Slave SPI mode. This pin has a weak internal pull-up.
TOE	I	Test Output Enable tristates all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to $\rm V_{\rm CC}$ is recommended.

1. If not actively driven, the internal pull-up may not be sufficient. An external pull-up resistor of 4.7k to $10k\Omega$ is recommended.

2. When using the device in Master SPI mode, it must be mutually exclusive from JTAG operations (i.e. TCK tied to GND) or the JTAG TCK must be free-running when used in a system JTAG test environment. If Master SPI mode is used in conjunction with a JTAG download cable, the device power cycle is required after the cable is unplugged.



Lead-Free Packaging

Commercial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5MN132C	1.2V	-5	Lead-Free csBGA	132	COM	5
LFXP2-5E-6MN132C	1.2V	-6	Lead-Free csBGA	132	COM	5
LFXP2-5E-7MN132C	1.2V	-7	Lead-Free csBGA	132	COM	5
LFXP2-5E-5TN144C	1.2V	-5	Lead-Free TQFP	144	COM	5
LFXP2-5E-6TN144C	1.2V	-6	Lead-Free TQFP	144	COM	5
LFXP2-5E-7TN144C	1.2V	-7	Lead-Free TQFP	144	COM	5
LFXP2-5E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	5
LFXP2-5E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	5
LFXP2-5E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	5
LFXP2-5E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	5
LFXP2-5E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	5
LFXP2-5E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5MN132C	1.2V	-5	Lead-Free csBGA	132	COM	8
LFXP2-8E-6MN132C	1.2V	-6	Lead-Free csBGA	132	COM	8
LFXP2-8E-7MN132C	1.2V	-7	Lead-Free csBGA	132	COM	8
LFXP2-8E-5TN144C	1.2V	-5	Lead-Free TQFP	144	COM	8
LFXP2-8E-6TN144C	1.2V	-6	Lead-Free TQFP	144	COM	8
LFXP2-8E-7TN144C	1.2V	-7	Lead-Free TQFP	144	COM	8
LFXP2-8E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	8
LFXP2-8E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	8
LFXP2-8E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	8
LFXP2-8E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	8
LFXP2-8E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	8
LFXP2-8E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	17
LFXP2-17E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	17
LFXP2-17E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	17
LFXP2-17E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	17
LFXP2-17E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	17
LFXP2-17E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	17
LFXP2-17E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	17
LFXP2-17E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	17
LFXP2-17E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	17