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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	3625
Number of Logic Elements/Cells	29000
Total RAM Bits	396288
Number of I/O	363
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-30e-6fn484i

Routing

There are many resources provided in the LatticeXP2 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) or x6 (spans seven PFU) connections. The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered to allow both short and long connections routing between PFUs.

The LatticeXP2 family has an enhanced routing architecture to produce a compact design. The Diamond design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Phase Locked Loops (PLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The LatticeXP2 family supports between two and four full featured General Purpose PLLs (GPLL). The architecture of the GPLL is shown in Figure 2-4.

CLKI, the PLL reference frequency, is provided either from the pin or from routing; it feeds into the Input Clock Divider block. CLKFB, the feedback signal, is generated from CLKOP (the primary clock output) or from a user clock pin/logic. CLKFB feeds into the Feedback Divider and is used to multiply the reference frequency.

Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. The phase and frequency of the VCO are determined from the input path and feedback signals. A LOCK signal is generated by the VCO to indicate that the VCO is locked with the input clock signal.

The output of the VCO feeds into the CLKOP Divider, a post-scalar divider. The duty cycle of the CLKOP Divider output can be fine tuned using the Duty Trim block, which creates the CLKOP signal. By allowing the VCO to operate at higher frequencies than CLKOP, the frequency range of the GPLL is expanded. The output of the CLKOP Divider is passed through the CLKOK Divider, a secondary clock divider, to generate lower frequencies for the CLKOK output. For applications that require even lower frequencies, the CLKOP signal is passed through a divide-by-three divider to produce the CLKOK2 output. The CLKOK2 output is provided for applications that use source synchronous logic. The Phase/Duty Cycle/Duty Trim block is used to adjust the phase and duty cycle of the CLKOP Divider output to generate the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

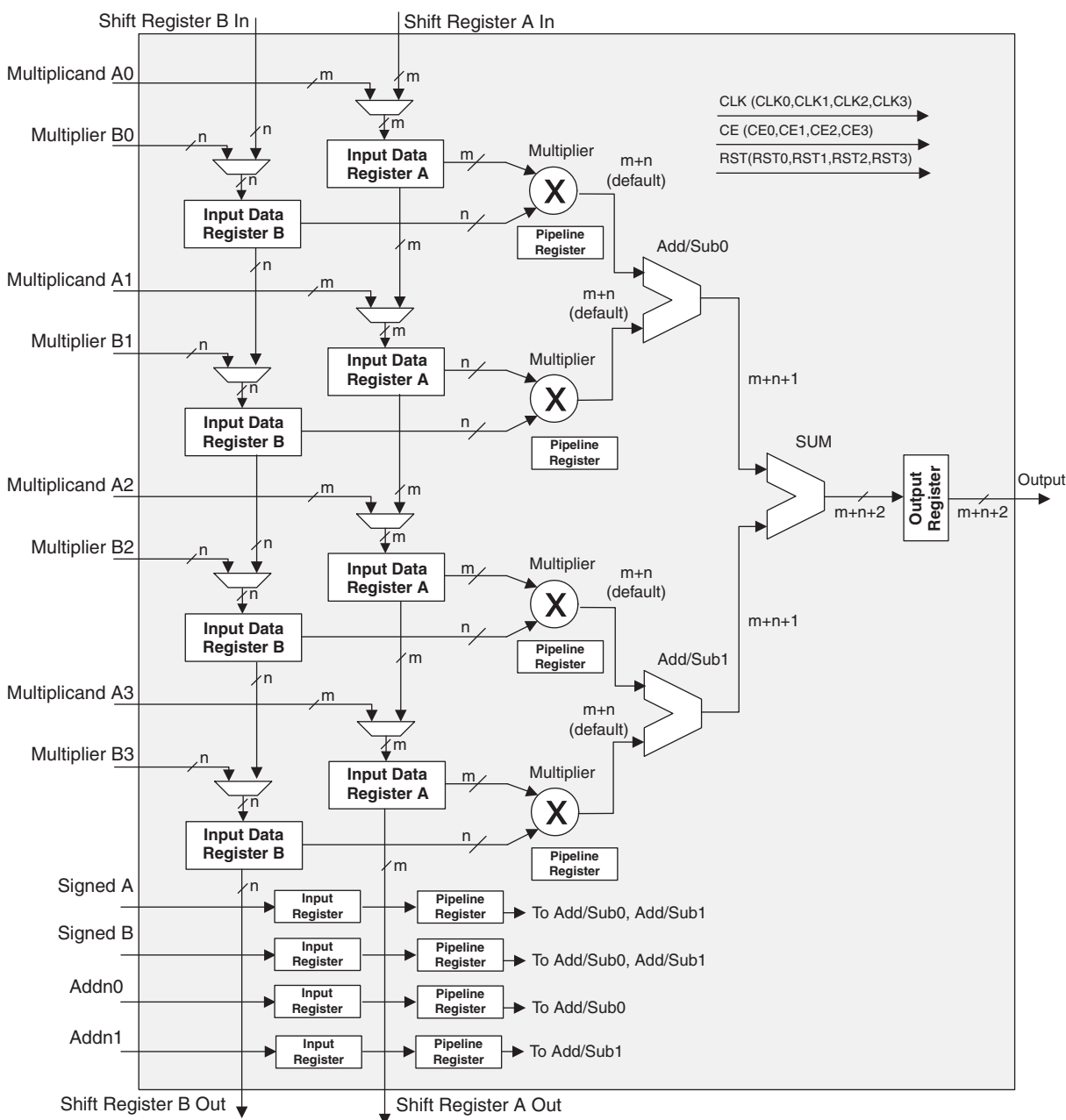
The clock outputs from the GPLL; CLKOP, CLKOK, CLKOK2 and CLKOS, are fed to the clock distribution network.

For further information on the GPLL please see TN1126, [LatticeXP2 sysCLOCK PLL Design and Usage Guide](#).

MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-23 shows the MULTADDSUBSUM sysDSP element.

Figure 2-23. MULTADDSUBSUM



Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable (CE) and Reset (RST) signals from routing are available to every DSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output

IPexpress™

The user can access the sysDSP block via the Lattice IPexpress tool, which provides the option to configure each DSP module (or group of modules), or by direct HDL instantiation. In addition, Lattice has partnered with The Math-Works® to support instantiation in the Simulink® tool, a graphical simulation environment. Simulink works with Diamond to dramatically shorten the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LatticeXP2 DSP include the Bit Correlator, FFT functions, FIR Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IP cores.

Resources Available in the LatticeXP2 Family

Table 2-8 shows the maximum number of multipliers for each member of the LatticeXP2 family. Table 2-9 shows the maximum available EBR RAM Blocks and Serial TAG Memory bits in each LatticeXP2 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2-8. Maximum Number of DSP Blocks in the LatticeXP2 Family

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
XP2-5	3	24	12	3
XP2-8	4	32	16	4
XP2-17	5	40	20	5
XP2-30	7	56	28	7
XP2-40	8	64	32	8

Table 2-9. Embedded SRAM/TAG Memory in the LatticeXP2 Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)	TAG Memory (Bits)
XP2-5	9	166	632
XP2-8	12	221	768
XP2-17	15	276	2184
XP2-30	21	387	2640
XP2-40	48	885	3384

LatticeXP2 DSP Performance

Table 2-10 lists the maximum performance in Millions of MAC (MMAC) operations per second for each member of the LatticeXP2 family.

Table 2-10. DSP Performance

Device	DSP Block	DSP Performance MMAC
XP2-5	3	3,900
XP2-8	4	5,200
XP2-17	5	6,500
XP2-30	7	9,100
XP2-40	8	10,400

For further information on the sysDSP block, please see TN1140, [LatticeXP2 sysDSP Usage Guide](#).

Table 2-11. PIO Signal List

Name	Type	Description
CE	Control from the core	Clock enables for input and output block flip-flops
CLK	Control from the core	System clocks for input and output blocks
ECLK1, ECLK2	Control from the core	Fast edge clocks
LSR	Control from the core	Local Set/Reset
GSRN	Control from routing	Global Set/Reset (active low)
INCK ²	Input to the core	Input to Primary Clock Network or PLL reference inputs
DQS	Input to PIO	DQS signal from logic (routing) to PIO
INDD	Input to the core	Unregistered data input to core
INFF	Input to the core	Registered input on positive edge of the clock (CLK0)
IPOS0, IPOS1	Input to the core	Double data rate registered inputs to the core
QPOS0 ¹ , QPOS1 ¹	Input to the core	Gearbox pipelined inputs to the core
QNEG0 ¹ , QNEG1 ¹	Input to the core	Gearbox pipelined inputs to the core
OPOS0, ONEG0, OPOS2, ONEG2	Output data from the core	Output signals from the core for SDR and DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation
DEL[3:0]	Control from the core	Dynamic input delay control bits
TD	Tristate control from the core	Tristate signal from the core used in SDR operation
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block
DQSXFER	Control from core	Controls signal to the Output block

1. Signals available on left/right/bottom only.

2. Selected I/O.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with necessary clock and selection logic.

Input Register Block

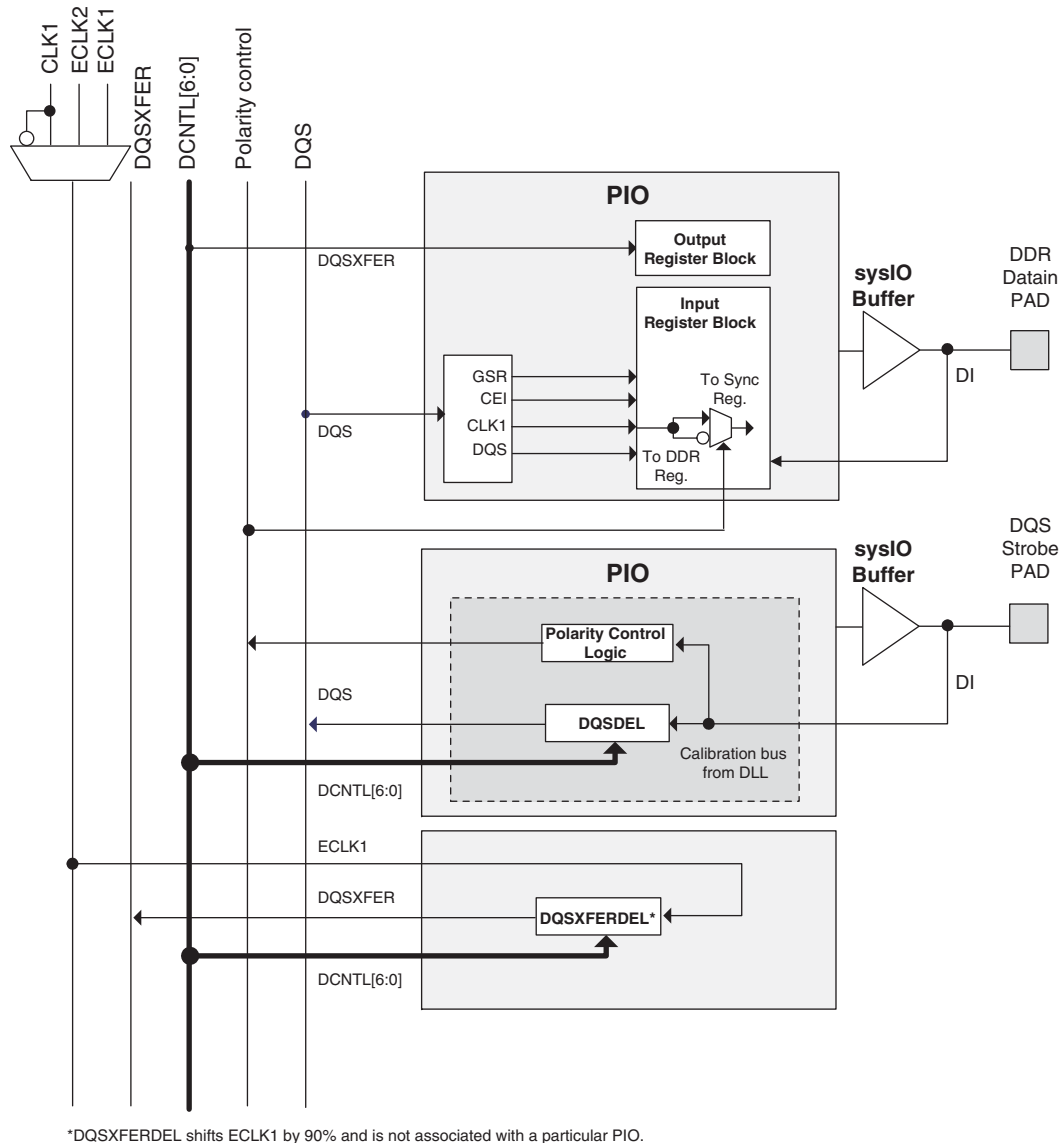
The input register blocks for PIOs contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-26 shows the diagram of the input register block.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the Single Data Rate (SDR) mode, the data is registered, by one of the registers in the SDR Sync register block, with the system clock. In DDR mode two registers are used to sample the data on the positive and negative edges of the DQS signal which creates two data streams, D0 and D2. D0 and D2 are synchronized with the system clock before entering the core. Further information on this topic can be found in the DDR Memory Support section of this data sheet.

By combining input blocks of the complementary PIOs and sharing registers from output blocks, a gearbox function can be implemented, that takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-26 shows the diagram using this gearbox function. For more information on this topic, please see TN1138, [LatticeXP2 High Speed I/O Interface](#).

Figure 2-31. DQS Local Bus



*DQSXFERDEL shifts ECLK1 by 90° and is not associated with a particular PIO.

Polarity Control Logic

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeXP2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block and requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

LatticeXP2 devices contain two types of sysIO buffer pairs.

1. Top and Bottom (Banks 0, 1, 4 and 5) sysIO Buffer Pairs (Single-Ended Outputs Only)

The sysIO buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Only the I/Os on the top and bottom banks have programmable PCI clamps.

2. Left and Right (Banks 2, 3, 6 and 7) sysIO Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp pad is associated with the negative side of the differential I/O.

LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

Typical sysIO I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} , $V_{CCCONFIG}$ (V_{CCIO7}) and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. During power up and before the FPGA core logic becomes active, all user I/Os will be high-impedance with weak pull-up. Please refer to TN1136, [LatticeXP2 sysIO Usage Guide](#) for additional information.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported sysIO Standards

The LatticeXP2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8V, 2.5V and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, MLVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-12 and 2-13 show the I/O standards (together with their supply and reference voltages) supported by LatticeXP2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1136, [LatticeXP2 sysIO Usage Guide](#).

Density Shifting

The LatticeXP2 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Programming and Erase Flash Supply Current^{1, 2, 3, 4, 5}

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical (25°C, Max. Supply) ⁶	Units
I_{CC}	Core Power Supply Current	XP2-5	17	mA
		XP2-8	21	mA
		XP2-17	28	mA
		XP2-30	36	mA
		XP2-40	50	mA
I_{CCAUX}	Auxiliary Power Supply Current ⁷	XP2-5	64	mA
		XP2-8	66	mA
		XP2-17	83	mA
		XP2-30	87	mA
		XP2-40	88	mA
I_{CCPLL}	PLL Power Supply Current (per PLL)		0.1	mA
I_{CCIO}	Bank Power Supply Current (per Bank)		5	mA
I_{CCJ}	V_{CCJ} Power Supply Current ⁸		14	mA

- For further information on supply current, please see TN1139, [Power Estimation and Management for LatticeXP2 Devices](#).
- Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
- Frequency 0 MHz (excludes dynamic power from FPGA operation).
- A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.
- Bypass or decoupling capacitor across the supply.
- $T_J = 25^\circ\text{C}$, power supplies at nominal voltage.
- In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL} . For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.
- When programming via JTAG.

sysIO Single-Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL} ¹ (mA)	I _{OH} ¹ (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)	Max. (V)	Min. (V)		
LVCMOS33	-0.3	0.8	2.0	3.6	0.4	V _{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V _{CCIO} - 0.2	0.1	-0.1
LVTTTL33	-0.3	0.8	2.0	3.6	0.4	V _{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V _{CCIO} - 0.2	0.1	-0.1
LVCMOS25	-0.3	0.7	1.7	3.6	0.4	V _{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V _{CCIO} - 0.2	0.1	-0.1
LVCMOS18	-0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.6	0.4	V _{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V _{CCIO} - 0.2	0.1	-0.1
LVCMOS15	-0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.6	0.4	V _{CCIO} - 0.4	8, 4	-8, -4
					0.2	V _{CCIO} - 0.2	0.1	-0.1
LVCMOS12	-0.3	0.35 V _{CC}	0.65 V _{CC}	3.6	0.4	V _{CCIO} - 0.4	6, 2	-6, -2
					0.2	V _{CCIO} - 0.2	0.1	-0.1
PCI33	-0.3	0.3 V _{CCIO}	0.5 V _{CCIO}	3.6	0.1 V _{CCIO}	0.9 V _{CCIO}	1.5	-0.5
SSTL33_I	-0.3	V _{REF} - 0.2	V _{REF} + 0.2	3.6	0.7	V _{CCIO} - 1.1	8	-8
SSTL33_II	-0.3	V _{REF} - 0.2	V _{REF} + 0.2	3.6	0.5	V _{CCIO} - 0.9	16	-16
SSTL25_I	-0.3	V _{REF} - 0.18	V _{REF} + 0.18	3.6	0.54	V _{CCIO} - 0.62	7.6	-7.6
							12	-12
SSTL25_II	-0.3	V _{REF} - 0.18	V _{REF} + 0.18	3.6	0.35	V _{CCIO} - 0.43	15.2	-15.2
							20	-20
SSTL18_I	-0.3	V _{REF} - 0.125	V _{REF} + 0.125	3.6	0.4	V _{CCIO} - 0.4	6.7	-6.7
SSTL18_II	-0.3	V _{REF} - 0.125	V _{REF} + 0.125	3.6	0.28	V _{CCIO} - 0.28	8	-8
							11	-11
HSTL15_I	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.6	0.4	V _{CCIO} - 0.4	4	-4
							8	-8
HSTL18_I	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.6	0.4	V _{CCIO} - 0.4	8	-8
							12	-12
HSTL18_II	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.6	0.4	V _{CCIO} - 0.4	16	-16

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed $n \cdot 8\text{mA}$, where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

RSDS

The LatticeXP2 devices support differential RSDS standard. This standard is emulated using complementary LVC-MOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

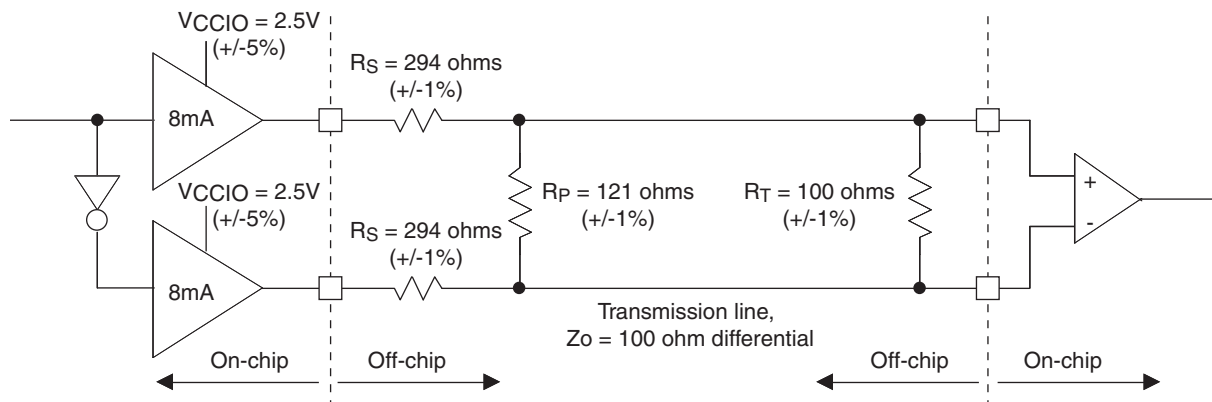


Table 3-4. RSDS DC Conditions¹

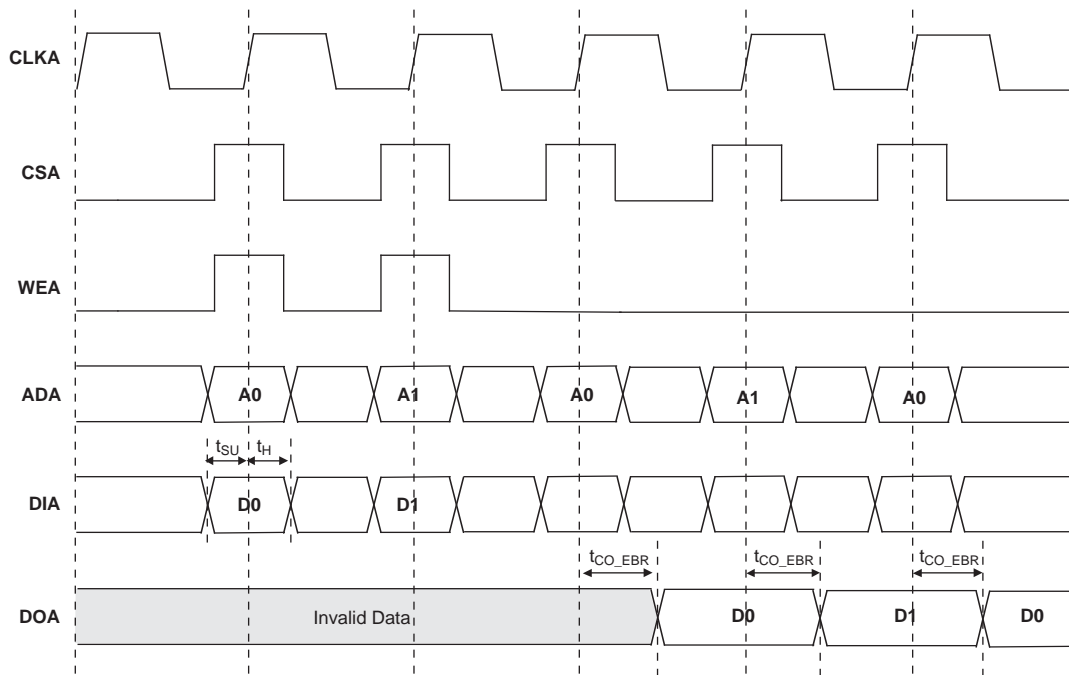
Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/-1%)	294	Ω
R _P	Driver Parallel Resistor (+/-1%)	121	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage (After R _P)	1.35	V
V _{OL}	Output Low Voltage (After R _P)	1.15	V
V _{OD}	Output Differential Voltage (After R _P)	0.20	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	101.5	Ω
I _{DC}	DC Output Current	3.66	mA

1. For input buffer, see LVDS table.

EBR Timing Diagrams

Figure 3-6. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-7. Read/Write Mode with Input and Output Registers

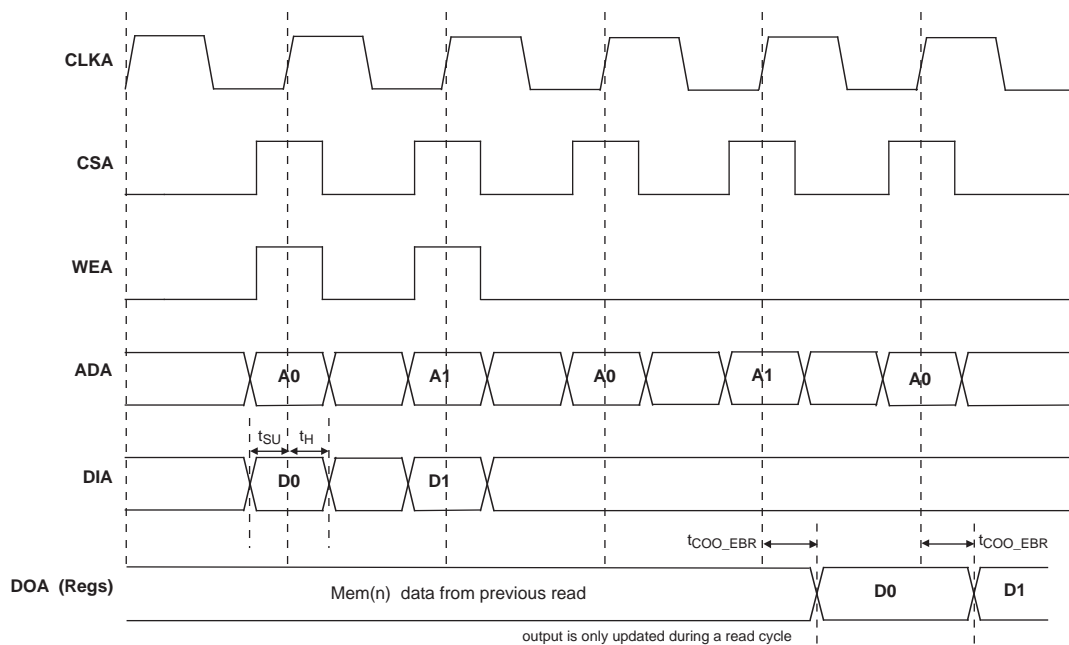
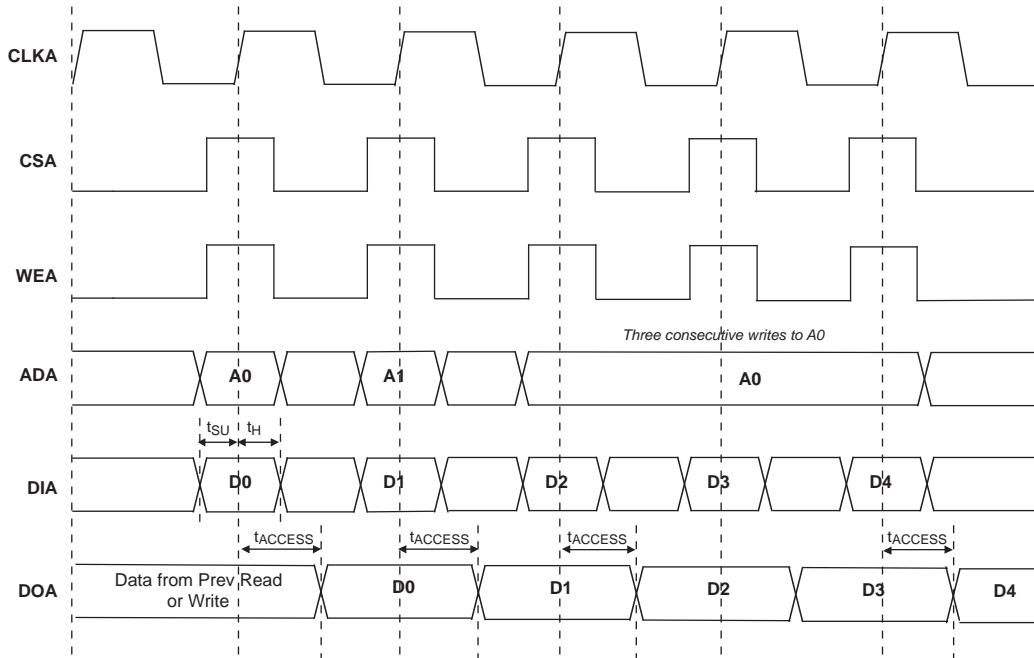


Figure 3-8. Write Through (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		10	—	435	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		10	—	435	MHz
f_{OUT2}	K-Divider Output Frequency	CLKOK	0.078	—	217.5	MHz
		CLKOK2	3.3	—	145	MHz
f_{VCO}	PLL VCO Frequency		435	—	870	MHz
f_{PFD}	Phase Detector Input Frequency		10	—	435	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected ³	45	50	55	%
t_{CPA}	Coarse Phase Adjust		-5	0	5	%
t_{PH} ⁴	Output Phase Accuracy		-5	0	5	%
t_{OPJIT} ¹	Output Clock Period Jitter	$f_{OUT} > 400$ MHz	—	—	±50	ps
		$100 \text{ MHz} < f_{OUT} < 400$ MHz	—	—	±125	ps
		$f_{OUT} < 100$ MHz	—	—	0.025	UIPP
t_{SK}	Input Clock to Output Clock Skew	N/M = integer	—	—	±240	ps
t_{OPW}	Output Clock Pulse Width	At 90% or 10%	1	—	—	ns
t_{LOCK} ²	PLL Lock-in Time	25 to 435 MHz	—	—	50	μs
		10 to 25 MHz	—	—	100	μs
t_{IPJIT}	Input Clock Period Jitter		—	—	±200	ps
t_{FBKDL}	External Feedback Delay		—	—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_{RSTKW}	Reset Signal Pulse Width (RSTK)		10	—	—	ns
t_{RSTW}	Reset Signal Pulse Width (RST)		500	—	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

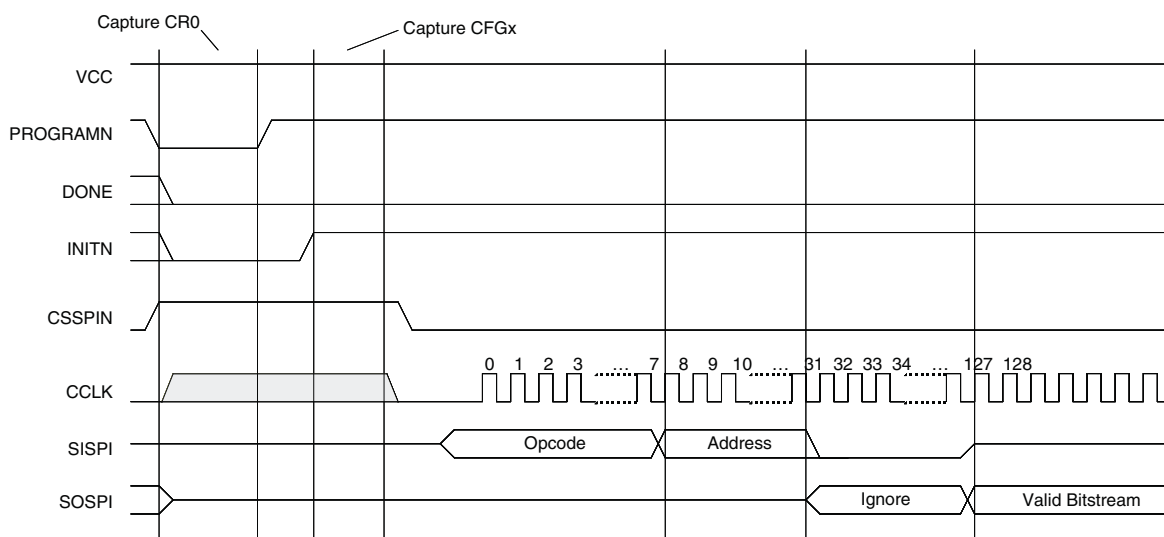
4. Relative to CLKOP.

On-Chip Oscillator and Configuration Master Clock Characteristics

Over Recommended Operating Conditions

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value -30%	Selected value +30%	MHz
Duty Cycle	40	60	%

Figure 3-9. Master SPI Configuration Waveforms



Flash Download Time (from On-Chip Flash to SRAM)

Over Recommended Operating Conditions

Symbol	Parameter		Min.	Typ.	Max.	Units
t_{REFRESH}	PROGRAMN Low-to-High. Transition to Done High.	XP2-5	—	1.8	2.1	ms
		XP2-8	—	1.9	2.3	ms
		XP2-17	—	1.7	2.0	ms
		XP2-30	—	2.0	2.1	ms
		XP2-40	—	2.0	2.3	ms
	Power-up refresh when PROGRAMN is pulled up to V_{CC} ($V_{CC}=V_{CC}$ Min)	XP2-5	—	1.8	2.1	ms
		XP2-8	—	1.9	2.3	ms
		XP2-17	—	1.7	2.0	ms
		XP2-30	—	2.0	2.1	ms
		XP2-40	—	2.0	2.3	ms

Flash Program Time

Over Recommended Operating Conditions

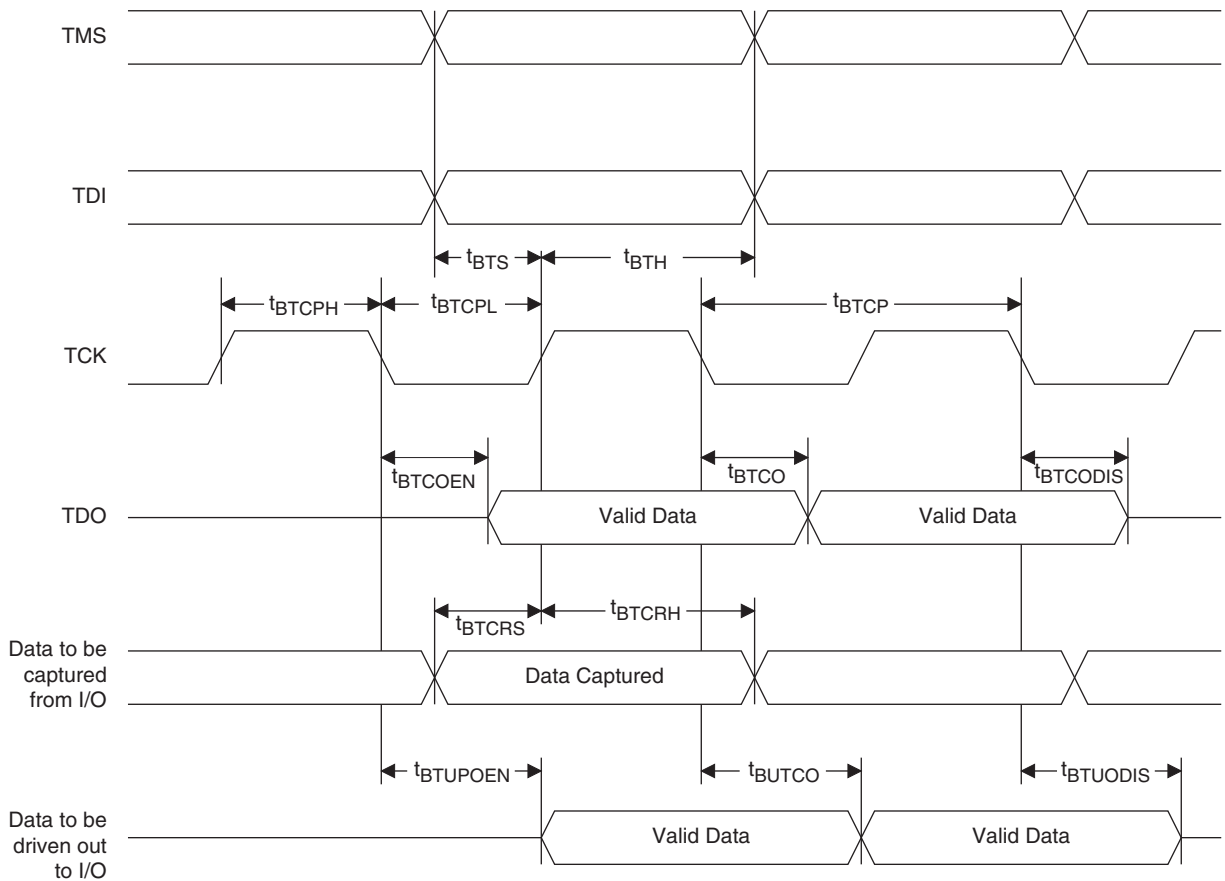
Device	Flash Density		Program Time	Units
			Typ.	
XP2-5	1.2M	TAG	1.0	ms
		Main Array	1.1	s
XP2-8	2.0M	TAG	1.0	ms
		Main Array	1.4	s
XP2-17	3.6M	TAG	1.0	ms
		Main Array	1.8	s
XP2-30	6.0M	TAG	2.0	ms
		Main Array	3.0	s
XP2-40	8.0M	TAG	2.0	ms
		Main Array	4.0	s

Flash Erase Time

Over Recommended Operating Conditions

Device	Flash Density		Erase Time	Units
			Typ.	
XP2-5	1.2M	TAG	1.0	s
		Main Array	3.0	s
XP2-8	2.0M	TAG	1.0	s
		Main Array	4.0	s
XP2-17	3.6M	TAG	1.0	s
		Main Array	5.0	s
XP2-30	6.0M	TAG	2.0	s
		Main Array	7.0	s
XP2-40	8.0M	TAG	2.0	s
		Main Array	9.0	s

Figure 3-10. JTAG Port Timing Waveforms



Signal Descriptions (Cont.)

Signal Name	I/O	Description
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used during sysCONFIG)		
CFG[1:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, an internal pull-up is enabled.
INITN ¹	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
SISPI ²	I/O	Input data pin in slave SPI mode and Output data pin in Master SPI mode.
SOSPI ²	I/O	Output data pin in slave SPI mode and Input data pin in Master SPI mode.
CSSPIN ²	O	Chip select for external SPI Flash memory in Master SPI mode. This pin has a weak internal pull-up.
CSSPISN	I	Chip select in Slave SPI mode. This pin has a weak internal pull-up.
TOE	I	Test Output Enable tristates all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to V _{CC} is recommended.

1. If not actively driven, the internal pull-up may not be sufficient. An external pull-up resistor of 4.7k to 10k Ω is recommended.
2. When using the device in Master SPI mode, it must be mutually exclusive from JTAG operations (i.e. TCK tied to GND) or the JTAG TCK must be free-running when used in a system JTAG test environment. If Master SPI mode is used in conjunction with a JTAG download cable, the device power cycle is required after the cable is unplugged.

Lead-Free Packaging

Commercial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5MN132C	1.2V	-5	Lead-Free csBGA	132	COM	5
LFXP2-5E-6MN132C	1.2V	-6	Lead-Free csBGA	132	COM	5
LFXP2-5E-7MN132C	1.2V	-7	Lead-Free csBGA	132	COM	5
LFXP2-5E-5TN144C	1.2V	-5	Lead-Free TQFP	144	COM	5
LFXP2-5E-6TN144C	1.2V	-6	Lead-Free TQFP	144	COM	5
LFXP2-5E-7TN144C	1.2V	-7	Lead-Free TQFP	144	COM	5
LFXP2-5E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	5
LFXP2-5E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	5
LFXP2-5E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	5
LFXP2-5E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	5
LFXP2-5E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	5
LFXP2-5E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5MN132C	1.2V	-5	Lead-Free csBGA	132	COM	8
LFXP2-8E-6MN132C	1.2V	-6	Lead-Free csBGA	132	COM	8
LFXP2-8E-7MN132C	1.2V	-7	Lead-Free csBGA	132	COM	8
LFXP2-8E-5TN144C	1.2V	-5	Lead-Free TQFP	144	COM	8
LFXP2-8E-6TN144C	1.2V	-6	Lead-Free TQFP	144	COM	8
LFXP2-8E-7TN144C	1.2V	-7	Lead-Free TQFP	144	COM	8
LFXP2-8E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	8
LFXP2-8E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	8
LFXP2-8E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	8
LFXP2-8E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	8
LFXP2-8E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	8
LFXP2-8E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	17
LFXP2-17E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	17
LFXP2-17E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	17
LFXP2-17E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	17
LFXP2-17E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	17
LFXP2-17E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	17
LFXP2-17E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	17
LFXP2-17E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	17
LFXP2-17E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	17

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5F484I	1.2V	-5	fpBGA	484	IND	40
LFXP2-40E-6F484I	1.2V	-6	fpBGA	484	IND	40
LFXP2-40E-5F672I	1.2V	-5	fpBGA	672	IND	40
LFXP2-40E-6F672I	1.2V	-6	fpBGA	672	IND	40

Date	Version	Section	Change Summary
April 2008 (cont.)	01.4 (cont.)	DC and Switching Characteristics (cont.)	Updated Flash Download Time (From On-Chip Flash to SRAM) Table
			Updated Flash Program Time Table
			Updated Flash Erase Time Table
			Updated FlashBAK (from EBR to Flash) Table
			Updated Hot Socketing Specifications Table footnotes
June 2008	01.5	Pinout Information	Updated Signal Descriptions Table
		Architecture	Removed Read-Before-Write sysMEM EBR mode.
			Clarification of the operation of the secondary clock regions.
		DC and Switching Characteristics	Removed Read-Before-Write sysMEM EBR mode.
August 2008	01.6	Pinout Information	Updated DDR Banks Bonding Out per I/O Bank section of Pin Information Summary Table.
		—	Data sheet status changed from preliminary to final.
		Architecture	Clarification of the operation of the secondary clock regions.
		DC and Switching Characteristics	Removed “8W” specification from Hot Socketing Specifications table.
			Removed “8W” footnote from DC Electrical Characteristics table.
			Updated Register-to-Register Performance table.
		Ordering Information	Removed “8W” option from Part Number Description.
			Removed XP2-17 “8W” OPNs.
April 2011	01.7	DC and Switching Characteristics	Recommended Operating Conditions table, added footnote 5.
			On-Chip Flash Memory Specifications table, added footnote 1.
			BLVDS DC Conditions, corrected column title to be Z0 = 90 ohms.
			sysCONFIG Port Timing Specifications table, added footnote 1 for t_{DINIT} .
January 2012	01.8	Multiple	Added support for Lattice Diamond design software.
		Architecture	Corrected information regarding SED support.
		DC and Switching Characteristics	Added reference to ESD Performance Qualification Summary information.
May 2013	01.9	All	Updated document with new corporate logo.
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.
			Added information regarding SED support.
		DC and Switching Characteristics	Removed Input Clock Rise/Fall Time 1ns max from the sysCLOCK PLL Timing table.
March 2014	02.0	Architecture	Updated topside mark in Ordering Information diagram.
			Updated Typical sysIO I/O Behavior During Power-up section. Added information on POR signal deactivation.
August 2014	02.1	Architecture	Updated Typical sysIO I/O Behavior During Power-up section. Described user I/Os during power up and before FPGA core logic is active.
September 2014	2.2	DC and Switching Characteristics	Updated Switching Test Conditions section. Re-linked missing figure.