E.J. Lattice Semiconductor Corporation - <u>LFXP2-30E-6FN672C Datasheet</u>



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	3625
Number of Logic Elements/Cells	29000
Total RAM Bits	396288
Number of I/O	472
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-30e-6fn672c

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Introduction

LatticeXP2 devices combine a Look-up Table (LUT) based FPGA fabric with non-volatile Flash cells in an architecture referred to as flexiFLASH.

The flexiFLASH approach provides benefits including instant-on, infinite reconfigurability, on chip storage with FlashBAK embedded block memory and Serial TAG memory and design security. The parts also support Live Update technology with TransFR, 128-bit AES Encryption and Dual-boot technologies.

The LatticeXP2 FPGA fabric was optimized for the new technology from the outset with high performance and low cost in mind. LatticeXP2 devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support and enhanced sysDSP blocks.

Lattice Diamond[®] design software allows large and complex designs to be efficiently implemented using the LatticeXP2 family of FPGA devices. Synthesis library support for LatticeXP2 is available for popular logic synthesis tools. The Diamond software uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeXP2 device. The Diamond tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed Intellectual Property (IP) LatticeCORE[™] modules for the LatticeXP2 family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.



LatticeXP2 Family Data Sheet Architecture

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Data Sheet DS1009

Architecture Overview

Each LatticeXP2 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM[™] Embedded Block RAM (EBR) and a row of sys-DSP[™] Digital Signal Processing blocks as shown in Figure 2-1.

On the left and right sides of the Programmable Functional Unit (PFU) array, there are Non-volatile Memory Blocks. In configuration mode the nonvolatile memory is programmed via the IEEE 1149.1 TAP port or the sysCONFIG[™] peripheral port. On power up, the configuration data is transferred from the Non-volatile Memory Blocks to the configuration SRAM. With this technology, expensive external configuration memory is not required, and designs are secured from unauthorized read-back. This transfer of data from non-volatile memory to configuration SRAM via wide busses happens in microseconds, providing an "instant-on" capability that allows easy interfacing in many applications. LatticeXP2 devices can also transfer data from the sysMEM EBR blocks to the Non-volatile Memory Blocks at user request.

There are two kinds of logic blocks, the PFU and the PFU without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

LatticeXP2 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large dedicated 18Kbit memory blocks. Each sysMEM block can be configured in a variety of depths and widths of RAM or ROM. In addition, LatticeXP2 devices contain up to two rows of DSP Blocks. Each DSP block has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysIO buffers. The sysIO buffers of the LatticeXP2 devices are arranged into eight banks, allowing the implementation of a wide variety of I/O standards. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as 7:1 LVDS interfaces, found in many display applications, and memory interfaces including DDR and DDR2.

The LatticeXP2 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

Other blocks provided include PLLs and configuration functions. The LatticeXP2 architecture provides up to four General Purpose PLLs (GPLL) per device. The GPLL blocks are located in the corners of the device.

The configuration block that supports features such as configuration bit-stream de-encryption, transparent updates and dual boot support is located between banks two and three. Every device in the LatticeXP2 family supports a sysCONFIG port, muxed with bank seven I/Os, which supports serial device configuration. A JTAG port is provided between banks two and three.

This family also provides an on-chip oscillator. LatticeXP2 devices use 1.2V as their core voltage.

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PFU Blocks

The core of the LatticeXP2 device is made up of logic blocks in two forms, PFUs and PFFs. PFUs can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. PFF blocks can be programmed to perform logic, arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered Slice 0 through Slice 3, as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.



Routing

There are many resources provided in the LatticeXP2 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) or x6 (spans seven PFU) connections. The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered to allow both short and long connections routing between PFUs.

The LatticeXP2 family has an enhanced routing architecture to produce a compact design. The Diamond design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Phase Locked Loops (PLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The LatticeXP2 family supports between two and four full featured General Purpose PLLs (GPLL). The architecture of the GPLL is shown in Figure 2-4.

CLKI, the PLL reference frequency, is provided either from the pin or from routing; it feeds into the Input Clock Divider block. CLKFB, the feedback signal, is generated from CLKOP (the primary clock output) or from a user clock pin/logic. CLKFB feeds into the Feedback Divider and is used to multiply the reference frequency.

Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. The phase and frequency of the VCO are determined from the input path and feedback signals. A LOCK signal is generated by the VCO to indicate that the VCO is locked with the input clock signal.

The output of the VCO feeds into the CLKOP Divider, a post-scalar divider. The duty cycle of the CLKOP Divider output can be fine tuned using the Duty Trim block, which creates the CLKOP signal. By allowing the VCO to operate at higher frequencies than CLKOP, the frequency range of the GPLL is expanded. The output of the CLKOP Divider is passed through the CLKOK Divider, a secondary clock divider, to generate lower frequencies for the CLKOK output. For applications that require even lower frequencies, the CLKOP signal is passed through a divide-by-three divider to produce the CLKOK2 output. The CLKOK2 output is provided for applications that use source synchronous logic. The Phase/Duty Cycle/Duty Trim block is used to adjust the phase and duty cycle of the CLKOP Divider output to generate the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The clock outputs from the GPLL; CLKOP, CLKOK, CLKOK2 and CLKOS, are fed to the clock distribution network.

For further information on the GPLL please see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide.



Secondary Clock/Control Sources

LatticeXP2 devices derive secondary clocks (SC0 through SC7) from eight dedicated clock input pads and the rest from routing. Figure 2-7 shows the secondary clock sources.

Figure 2-7. Secondary Clock Sources





Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs and clock dividers as shown in Figure 2-8.

Figure 2-8. Edge Clock Sources



Note: This diagram shows sources for the XP2-17 device. Smaller LatticeXP2 devices have two GPLLs.



Figure 2-12. Secondary Clock Selection



Slice Clock Selection

Figure 2-13 shows the clock selections and Figure 2-14 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals, via routing, can be used as clock inputs to the slices. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control, then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-13. Slice0 through Slice2 Clock Selection





Figure 2-16. FlashBAK Technology



Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports two forms of write behavior for single port or dual port operation:

- 1. Normal Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- 2. Write Through A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. GSRN, the global reset signal, resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-17.

Figure 2-17. Memory Core Reset





MULTADDSUB sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. The user can enable the input, output and pipeline registers. Figure 2-22 shows the MULTADDSUB sysDSP element.

Figure 2-22. MULTADDSUB





register. Similarly, CE and RST are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

Signed and Unsigned with Different Widths

The DSP block supports other widths, in addition to x9, x18 and x36 widths, of signed and unsigned multipliers. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2-7 provides an example of this.

Table 2-7. Sign Extension Example

Number	Unsigned	Unsigned 9-bit	Unsigned 18-bit	Signed	Two's Complement Signed 9 Bits	Two's Complement Signed 18 Bits
+5	0101	000000101	00000000000000101	0101	00000101	00000000000000101
-6	N/A	N/A	N/A	1010	111111010	1111111111111111010

OVERFLOW Flag from MAC

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. "Roll-over" occurs and an overflow signal is indicated when any of the following is true: two unsigned numbers are added and the result is a smaller number than the accumulator, two positive numbers are added with a negative sum or two negative numbers are added with a positive sum. Note that when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions for the overflow signal for signed and unsigned operands are listed in Figure 2-24.

Figure 2-24. Accumulator Overflow/Underflow





DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock, referred to as DQS, is not free-running, and this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only, as shown in Figure 2-30) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figure 2-30 and Figure 2-31 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of 6-bit bus calibration signals from two dedicated DLLs (DDR_DLL) on opposite sides of the device. Each DLL compensates DQS delays in its half of the device as shown in Figure 2-30. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.



Figure 2-30. Edge Clock, DLL Calibration and DQS Local Bus Distribution



Programming and Erase Flash Supply Current^{1, 2, 3, 4, 5}

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical (25°C, Max. Supply) ⁶	Units
		XP2-5	17	mA
		XP2-8	21	mA
I _{CC}	Core Power Supply Current	XP2-17	28	mA
		XP2-30	36	mA
		XP2-40	50	mA
		XP2-5	64	mA
		XP2-8	66	mA
I _{CCAUX}	Auxiliary Power Supply Current ⁷	XP2-17	83	mA
		XP2-30	87	mA
		XP2-40	88	mA
I _{CCPLL}	PLL Power Supply Current (per PLL)		0.1	mA
I _{CCIO}	Bank Power Supply Current (per Bank)		5	mA
I _{CCJ}	V _{CCJ} Power Supply Current ⁸		14	mA

1. For further information on supply current, please see TN1139, Power Estimation and Management for LatticeXP2 Devices.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

3. Frequency 0 MHz (excludes dynamic power from FPGA operation).

4. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.

5. Bypass or decoupling capacitor across the supply.

6. $T_J = 25^{\circ}C$, power supplies at nominal voltage.

 In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.

8. When programming via JTAG.



sysIO Single-Ended DC Electrical Characteristics

Input/Output		V _{IL}	VII	1	V _{OL}	V _{OH}		
Standard	Min. (V)	Max. (V)	Min. (V)	Max. (V)	Max. (V)	Min. (V)	l _{OL} 1 (mA)	l _{OH} ¹ (mA)
LVCMOS33	-0.3	0.8	2.0	3.6	0.4	V _{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V _{CCIO} - 0.2	0.1	-0.1
LVTTL33	-0.3	0.8	2.0	3.6	0.4	V _{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V _{CCIO} - 0.2	0.1	-0.1
LVCMOS25	-0.3	0.7	1.7	3.6	0.4	V _{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V _{CCIO} - 0.2	0.1	-0.1
LVCMOS18	-0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.6	0.4	V _{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V _{CCIO} - 0.2	0.1	-0.1
	0.2	0.25 \/	0.65 \	2.6	0.4	V _{CCIO} - 0.4	8, 4	-8, -4
	-0.5	0.35 VCCIO	0.03 V CCIO	3.0	0.2	V _{CCIO} - 0.2	0.1	-0.1
	-0.3	0.35 V	0.65 V	3.6	0.4	V _{CCIO} - 0.4	6, 2	-6, -2
	-0.5	0.35 V _{CC}	0.05 V _{CC}	3.0	0.2	V _{CCIO} - 0.2	0.1	-0.1
PCI33	-0.3	0.3 V _{CCIO}	0.5 V _{CCIO}	3.6	0.1 V _{CCIO}	0.9 V _{CCIO}	1.5	-0.5
SSTL33_I	-0.3	V _{REF} - 0.2	V _{REF} + 0.2	3.6	0.7	V _{CCIO} - 1.1	8	-8
SSTL33_II	-0.3	V _{REF} - 0.2	V _{REF} + 0.2	3.6	0.5	V _{CCIO} - 0.9	16	-16
SSTI 25 I	-0.3	Vpcc - 0 18	Vp== ± 0.18	3.6	0.54	Vacua - 0.62	7.6	-7.6
001220_1	-0.0	VREF - 0.10	VREF + 0.10	0.0	0.04	ACCIO - 0.05	12	-12
SSTI 25 II	-0.3	V0 18	V+0 18	36	0.35	Vac: a 0.43	15.2	-15.2
001225_11	-0.0	VREF - 0.10	VREF + 0.10	0.0	0.00	ACCIO - 0.42	20	-20
SSTL18_I	-0.3	V _{REF} - 0.125	V _{REF} + 0.125	3.6	0.4	V _{CCIO} - 0.4	6.7	-6.7
	-0.3	V 0 125	V ± 0 125	36	0.28	Vac 0.28	8	-8
001210_1	-0.0	VREF - 0.120	VREF + 0.120	0.0	0.20	VCCIO - 0.20	11	-11
HSTI 15 I	-0.3	Vpcc - 0 1		3.6	0.4		4	-4
	0.0	VREF 0.1	VREF 1 0.1	0.0	0.4	VCCID 0.4	8	-8
HSTI 18 I	-0.3	Vp== - 0 1		3.6	0.4		8	-8
	0.0	KEF - 0.1		0.0	U.7		12	-12
HSTL18_II	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.6	0.4	V _{CCIO} - 0.4	16	-16

Over Recommended Operating Conditions

 The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA, where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.



sysIO Differential Electrical Characteristics LVDS

Parameter	Description	Test Conditions	Min.	Тур.	Max.	Units
V _{INP} , V _{INM}	Input Voltage		0		2.4	V
V _{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	_	2.35	V
V _{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	_	—	mV
I _{IN}	Input Current	Power On or Power Off			+/-10	μA
V _{OH}	Output High Voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	_	1.38	1.60	V
V _{OL}	Output Low Voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	0.9V	1.03	—	V
V _{OD}	Output Voltage Differential	(V _{OP} - V _{OM}), R _T = 100 Ohm	250	350	450	mV
ΔV _{OD}	Change in V _{OD} Between High and Low		_	_	50	mV
V _{OS}	Output Voltage Offset	(V _{OP} + V _{OM})/2, R _T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V _{OS} Between H and L			_	50	mV
I _{SA}	Output Short Circuit Current	V _{OD} = 0V Driver Outputs Shorted to Ground	_	_	24	mA
I _{SAB}	Output Short Circuit Current	V _{OD} = 0V Driver Outputs Shorted to Each Other	_	_	12	mA

Over Recommended Operating Conditions

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see details in additional technical notes listed at the end of this data sheet.

LVDS25E

The top and bottom sides of LatticeXP2 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.







RSDS

The LatticeXP2 devices support differential RSDS standard. This standard is emulated using complementary LVC-MOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.



Figure 3-4. RSDS (Reduced Swing Differential Standard)

Table 3-4. RSDS DC Conditions¹

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/-1%)	294	Ω
R _P	Driver Parallel Resistor (+/-1%)	121	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage (After R _P)	1.35	V
V _{OL}	Output Low Voltage (After R _P)	1.15	V
V _{OD}	Output Differential Voltage (After R _P)	0.20	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	101.5	Ω
I _{DC}	DC Output Current	3.66	mA

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.



LatticeXP2 External Switching Characteristics (Continued)

			-7 -6 -5		-6		5		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
		XP2-5	1.00		1.30	_	1.60		ns
t _{HE}		XP2-8	1.00	_	1.30	_	1.60	_	ns
	Clock to Data Hold - PIO Input Register	XP2-17	1.00		1.30	_	1.60		ns
		XP2-30	1.20		1.60	_	1.90		ns
ParametertCloctCloctsu_DELECloctCloctClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfClocfCl		XP2-40	1.20		1.60		1.90		ns
		XP2-5	1.00		1.30	_	1.60		ns
		XP2-8	1.00		1.30	_	1.60		ns
t _{SU_DELE}	Clock to Data Setup - PIO Input Begister with Data Input Delay	XP2-17	1.00		1.30	_	1.60		ns
'SU_DELE		XP2-30	1.20		1.60		1.90		ns
		XP2-40	1.20		1.60		1.90		ns
		XP2-5	0.00		0.00		0.00		ns
		XP2-8	0.00	—	0.00	—	0.00	—	ns
t _{H_DELE}	Clock to Data Hold - PIO Input Begister with Input Data Delay	XP2-17	0.00	—	0.00	—	0.00	—	ns
'H_DELE		XP2-30	0.00		0.00		0.00		ns
		XP2-40	0.00		0.00		0.00		ns
f _{MAX_IOE}	Clock Frequency of I/O and PFU Register	XP2	_	420	_	357	_	311	MHz
General I/O Pir	Parameters (using Primary Clo	ck with PLL)1	1	1	1	1	1	
	Clock to Output - PIO Output Register	XP2-5	—	3.00	—	3.30	—	3.70	ns
		XP2-8		3.00		3.30		3.70	ns
t _{COPLL}		XP2-17		3.00		3.30		3.70	ns
		XP2-30	_	3.00		3.30		3.70	ns
		XP2-40		3.00		3.30		3.70	ns
		XP2-5	1.00		1.20		1.40		ns
		XP2-8	1.00		1.20		1.40		ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	XP2-17	1.00		1.20		1.40		ns
		XP2-30	1.00		1.20		1.40		ns
		XP2-40	1.00		1.20	_	1.40		ns
		XP2-5	0.90		1.10		1.30		ns
		XP2-8	0.90		1.10		1.30		ns
t _{HPLL}	Clock to Data Hold - PIO Input	XP2-17	0.90		1.10		1.30		ns
		XP2-30	1.00	—	1.20	—	1.40	—	ns
		XP2-40	1.00	—	1.20	—	1.40	—	ns
		XP2-5	1.90	—	2.10	—	2.30	—	ns
		XP2-8	1.90		2.10	—	2.30	_	ns
t _{SU_DELPLL}	Clock to Data Setup - PIO Input Begister with Data Input Delay	XP2-17	1.90	—	2.10	—	2.30	—	ns
	lingibion with Data input Delay	XP2-30	2.00	—	2.20	—	2.40	—	ns
		XP2-40	2.00	—	2.20	—	2.40	—	ns

Over Recommended Operating Conditions



LatticeXP2 Internal Switching Characteristics¹ (Continued)

		-7 -6 -5			-6				
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units	
t _{RST_PIO}	Asynchronous reset time for PFU Logic	—	0.386	—	0.419	—	0.452	ns	
t _{DEL}	Dynamic Delay Step Size	0.035	0.035	0.035	0.035	0.035	0.035	ns	
EBR Timing	EBR Timing								
t _{CO_EBR}	Clock (Read) to Output from Address or Data	_	2.774	_	3.142	_	3.510	ns	
t _{COO_EBR}	Clock (Write) to Output from EBR Output Register	_	0.360	_	0.408	—	0.456	ns	
^t SUDATA_EBR	Setup Data to EBR Memory (Write Clk)	-0.167	—	-0.198	_	-0.229	—	ns	
t _{HDATA_EBR}	Hold Data to EBR Memory (Write Clk)	0.194	—	0.231	_	0.267	_	ns	
t _{SUADDR_EBR}	Setup Address to EBR Memory (Write Clk)	-0.117	—	-0.137	_	-0.157	—	ns	
t _{HADDR_EBR}	Hold Address to EBR Memory (Write Clk)	0.157	_	0.182	_	0.207	_	ns	
t _{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory (Write/Read Clk)	-0.135	_	-0.159	_	-0.182	_	ns	
t _{HWREN_EBR}	Hold Write/Read Enable to EBR Memory (Write/Read Clk)	0.158	—	0.186	_	0.214	_	ns	
t _{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register (Read Clk)	0.144	—	0.160	_	0.176	_	ns	
t _{HCE_EBR}	Clock Enable Hold Time to EBR Output Register (Read Clk)	-0.097	—	-0.113	_	-0.129	_	ns	
t _{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register (Asynchro- nous)	_	1.156	_	1.341	_	1.526	ns	
t _{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.117	—	-0.137	_	-0.157	_	ns	
t _{HBE_EBR}	Byte Enable Hold Time to EBR Output Register Dynamic Delay on Each PIO	0.157	_	0.182	_	0.207	_	ns	
t _{RSTREC_EBR}	Asynchronous reset recovery time for EBR	0.233	—	0.291		0.347	—	ns	
t _{RST_EBR}	Asynchronous reset time for EBR	—	1.156	—	1.341	_	1.526	ns	
PLL Paramete	ers								
t _{RSTKREC_PLL}	After RSTK De-assert, Recovery Time Before Next Clock Edge Can Toggle K-divider Counter	1.000	_	1.000	_	1.000	_	ns	
t _{RSTREC_PLL}	After RST De-assert, Recovery Time Before Next Clock Edge Can Toggle M-divider Counter (Applies to M-Divider Portion of RST Only ²)	1.000	_	1.000		1.000	_	ns	
DSP Block Tir	ning								
t _{SUI_DSP}	Input Register Setup Time	0.135		0.151		0.166		ns	
t _{HI_DSP}	Input Register Hold Time	0.021	—	-0.006	—	-0.031		ns	
t _{SUP_DSP}	Pipeline Register Setup Time	2.505	—	2.784	—	3.064	—	ns	

Over Recommended Operating Conditions



sysCLOCK PLL Timing

Parameter	Description	Conditions	Min.	Тур.	Max.	Units
f _{IN}	Input Clock Frequency (CLKI, CLKFB)		10		435	MHz
fout	Output Clock Frequency (CLKOP, CLKOS)		10	—	435	MHz
f	K-Divider Output Frequency	CLKOK	0.078	_	217.5	MHz
'OUT2		CLKOK2	3.3		145	MHz
f _{VCO}	PLL VCO Frequency		435	_	870	MHz
f _{PFD}	Phase Detector Input Frequency		10	_	435	MHz
AC Characte	eristics					
t _{DT}	Output Clock Duty Cycle	Default duty cycle selected ³	45	50	55	%
t _{CPA}	Coarse Phase Adjust		-5	0	5	%
t _{PH} ⁴	Output Phase Accuracy		-5	0	5	%
		f _{OUT} > 400 MHz	—		±50	ps
t _{OPJIT} 1	Output Clock Period Jitter	100 MHz < f _{OUT} < 400 MHz	—	_	±125	ps
		f _{OUT} < 100 MHz	—	_	0.025	UIPP
t _{SK}	Input Clock to Output Clock Skew	N/M = integer	—		±240	ps
t _{OPW}	Output Clock Pulse Width	At 90% or 10%	1	_	—	ns
+ 2	PLL Look in Time	25 to 435 MHz	_		50	μs
LOCK		10 to 25 MHz	—	_	100	μs
t _{IPJIT}	Input Clock Period Jitter		_		±200	ps
t _{FBKDLY}	External Feedback Delay		_		10	ns
t _{HI}	Input Clock High Time	90% to 90%	0.5		_	ns
t _{LO}	Input Clock Low Time	10% to 10%	0.5		_	ns
t _{RSTKW}	Reset Signal Pulse Width (RSTK)		10	—	—	ns
t _{RSTW}	Reset Signal Pulse Width (RST)		500		—	ns

Over Recommended Operating Conditions

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. Relative to CLKOP.



FlashBAK Time (from EBR to Flash)

Over Recommended Operating Conditions

Device	EBR Density (Bits)	Time (Typ.)	Units
XP2-5	166K	1.5	S
XP2-8	221K	1.5	S
XP2-17	276K	1.5	S
XP2-30	387K	2.0	S
XP2-40	885K	3.0	S

JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	TCK Clock Frequency	—	25	MHz
t _{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t _{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t _{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t _{BTS}	TCK [BSCAN] setup time	8	—	ns
t _{BTH}	TCK [BSCAN] hold time	10	—	ns
t _{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t _{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t _{BTCODIS}	TAP controller falling edge of clock to valid disable	—	10	ns
t _{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t _{BTCRS}	BSCAN test capture register setup time	8	—	ns
t _{BTCRH}	BSCAN test capture register hold time	25	—	ns
t _{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
t _{BTUODIS}	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
t _{BTUPOEN}	BSCAN test update register, falling edge of clock to valid enable	_	25	ns



Lead-Free Packaging

Commercial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5MN132C	1.2V	-5	Lead-Free csBGA	132	COM	5
LFXP2-5E-6MN132C	1.2V	-6	Lead-Free csBGA	132	COM	5
LFXP2-5E-7MN132C	1.2V	-7	Lead-Free csBGA	132	COM	5
LFXP2-5E-5TN144C	1.2V	-5	Lead-Free TQFP	144	COM	5
LFXP2-5E-6TN144C	1.2V	-6	Lead-Free TQFP	144	COM	5
LFXP2-5E-7TN144C	1.2V	-7	Lead-Free TQFP	144	COM	5
LFXP2-5E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	5
LFXP2-5E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	5
LFXP2-5E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	5
LFXP2-5E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	5
LFXP2-5E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	5
LFXP2-5E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5MN132C	1.2V	-5	Lead-Free csBGA	132	COM	8
LFXP2-8E-6MN132C	1.2V	-6	Lead-Free csBGA	132	COM	8
LFXP2-8E-7MN132C	1.2V	-7	Lead-Free csBGA	132	COM	8
LFXP2-8E-5TN144C	1.2V	-5	Lead-Free TQFP	144	COM	8
LFXP2-8E-6TN144C	1.2V	-6	Lead-Free TQFP	144	COM	8
LFXP2-8E-7TN144C	1.2V	-7	Lead-Free TQFP	144	COM	8
LFXP2-8E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	8
LFXP2-8E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	8
LFXP2-8E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	8
LFXP2-8E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	8
LFXP2-8E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	8
LFXP2-8E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	17
LFXP2-17E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	17
LFXP2-17E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	17
LFXP2-17E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	17
LFXP2-17E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	17
LFXP2-17E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	17
LFXP2-17E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	17
LFXP2-17E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	17
LFXP2-17E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	17