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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	3625
Number of Logic Elements/Cells	29000
Total RAM Bits	396288
Number of I/O	201
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-30e-6ft256c

Architecture Overview

Each LatticeXP2 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and a row of sys-DSP™ Digital Signal Processing blocks as shown in Figure 2-1.

On the left and right sides of the Programmable Functional Unit (PFU) array, there are Non-volatile Memory Blocks. In configuration mode the nonvolatile memory is programmed via the IEEE 1149.1 TAP port or the sysCONFIG™ peripheral port. On power up, the configuration data is transferred from the Non-volatile Memory Blocks to the configuration SRAM. With this technology, expensive external configuration memory is not required, and designs are secured from unauthorized read-back. This transfer of data from non-volatile memory to configuration SRAM via wide busses happens in microseconds, providing an “instant-on” capability that allows easy interfacing in many applications. LatticeXP2 devices can also transfer data from the sysMEM EBR blocks to the Non-volatile Memory Blocks at user request.

There are two kinds of logic blocks, the PFU and the PFU without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

LatticeXP2 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large dedicated 18Kbit memory blocks. Each sysMEM block can be configured in a variety of depths and widths of RAM or ROM. In addition, LatticeXP2 devices contain up to two rows of DSP Blocks. Each DSP block has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysIO buffers. The sysIO buffers of the LatticeXP2 devices are arranged into eight banks, allowing the implementation of a wide variety of I/O standards. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as 7:1 LVDS interfaces, found in many display applications, and memory interfaces including DDR and DDR2.

The LatticeXP2 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

Other blocks provided include PLLs and configuration functions. The LatticeXP2 architecture provides up to four General Purpose PLLs (GPLL) per device. The GPLL blocks are located in the corners of the device.

The configuration block that supports features such as configuration bit-stream de-encryption, transparent updates and dual boot support is located between banks two and three. Every device in the LatticeXP2 family supports a sysCONFIG port, muxed with bank seven I/Os, which supports serial device configuration. A JTAG port is provided between banks two and three.

This family also provides an on-chip oscillator. LatticeXP2 devices use 1.2V as their core voltage.

Figure 2-4. General Purpose PLL (GPLL) Diagram

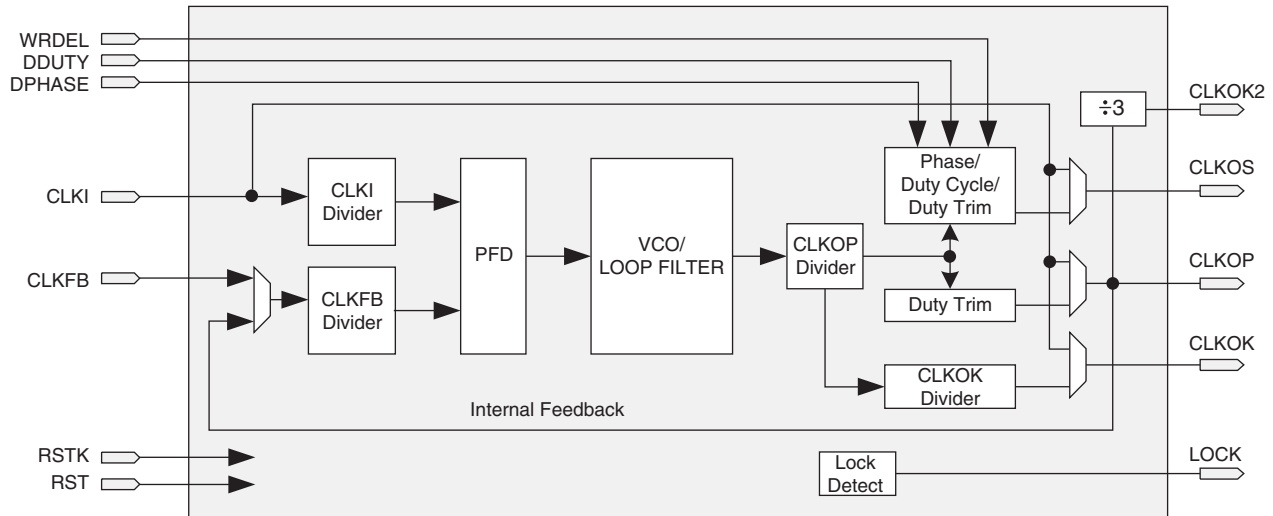


Table 2-4 provides a description of the signals in the GPLL blocks.

Table 2-4. GPLL Block Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
DPHASE [3:0]	I	DPA Phase Adjust input
DDUTY [3:0]	I	DPA Duty Cycle Select input
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
CLKOK2	O	PLL output to clock tree (CLKOP divided by 3)
LOCK	O	"1" indicates PLL LOCK to CLKI

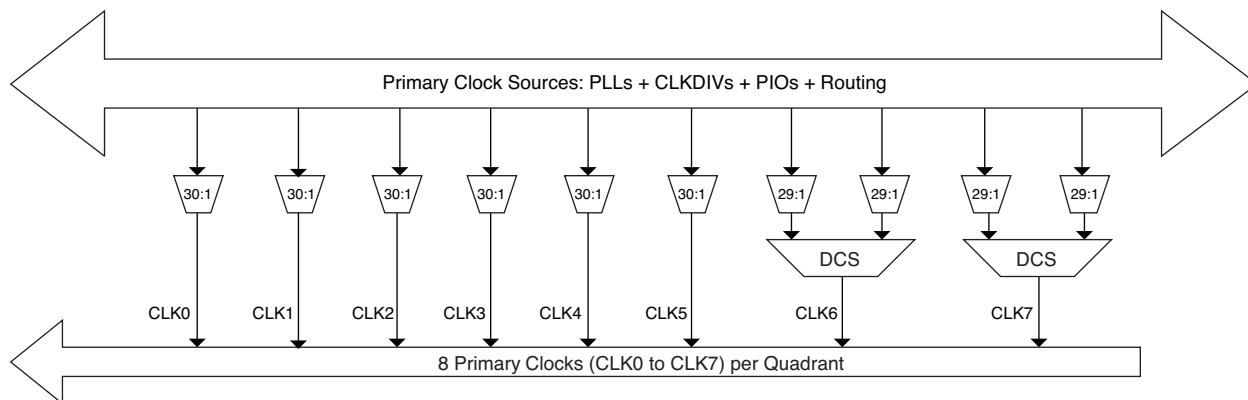
Clock Dividers

LatticeXP2 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a $\div 2$, $\div 4$ or $\div 8$ mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from the CLKOP output from the GPLLs or from the Edge Clocks (ECLK). The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets the input and forces all outputs to low. The RELEASE signal releases outputs to the input clock. For further information on clock dividers, please see TN1126, [LatticeXP2 sysCLOCK PLL Design and Usage Guide](#). Figure 2-5 shows the clock divider connections.

Primary Clock Routing

The clock routing structure in LatticeXP2 devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-9 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally.

Figure 2-9. Per Quadrant Primary Clock Selection

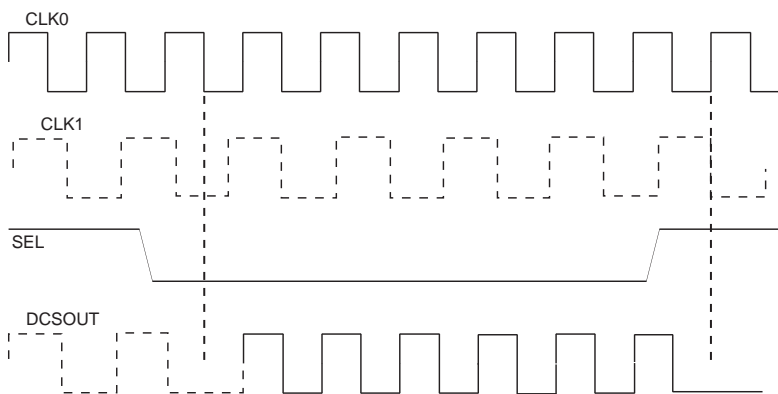


Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved irrespective of when the select signal is toggled. There are two DCS blocks per quadrant; in total, eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-9).

Figure 2-10 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, please see TN1126, [LatticeXP2 sysCLOCK PLL Design and Usage Guide](#).

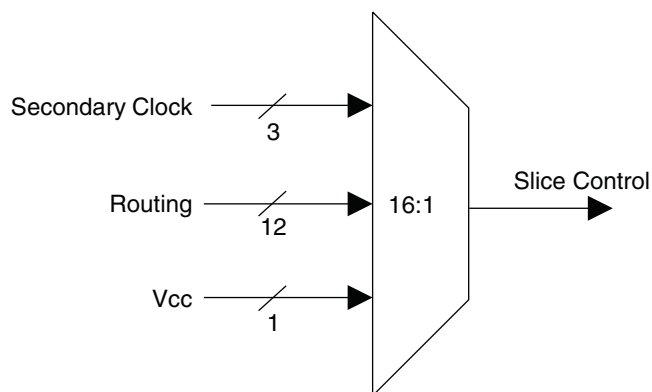
Figure 2-10. DCS Waveforms



Secondary Clock/Control Routing

Secondary clocks in the LatticeXP2 devices are region-based resources. The benefit of region-based resources is the relatively low injection delay and skew within the region, as compared to primary clocks. EBR rows, DSP rows and a special vertical routing channel bound the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP block in the DSP row or the center of the DSP row. Figure 2-11 shows this special vertical routing channel and the eight secondary clock regions for the LatticeXP2-40.

Figure 2-14. Slice0 through Slice2 Control Selection



Edge Clock Routing

LatticeXP2 devices have eight high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. Each device has two edge clocks per edge. Figure 2-15 shows the selection muxes for these clocks.

Figure 2-15. Edge Clock Mux Connections

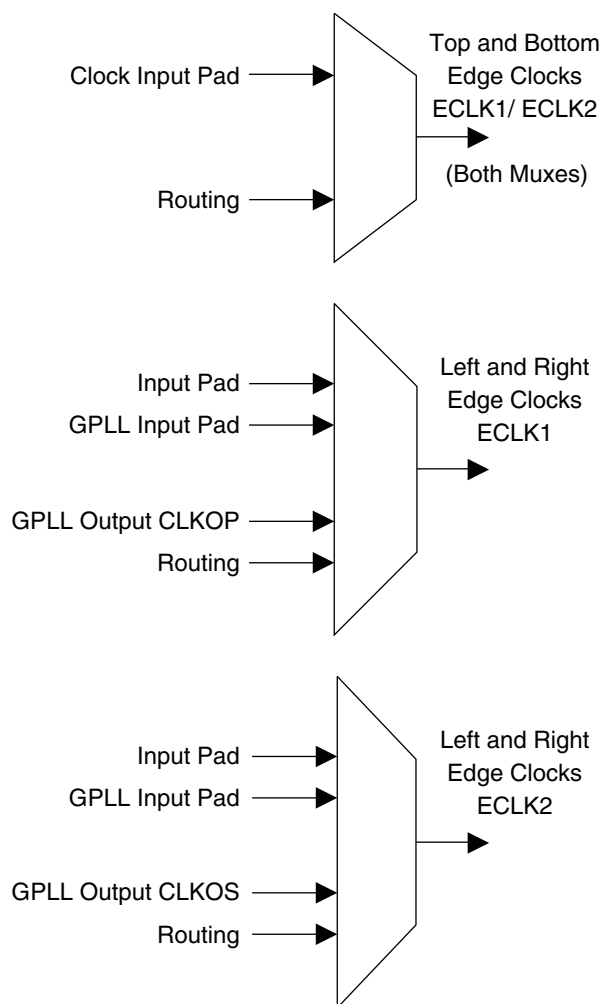
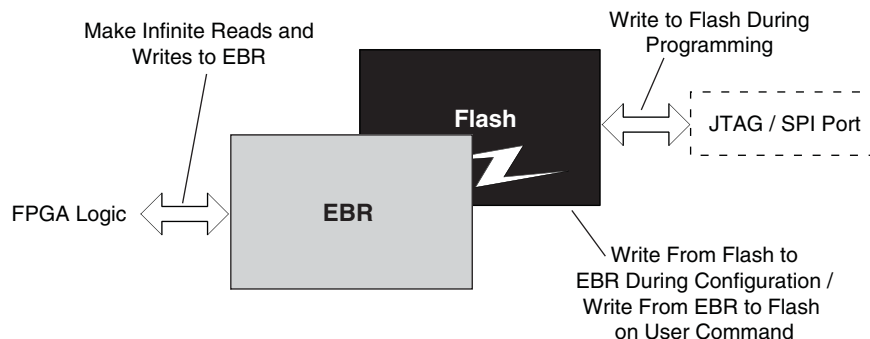


Figure 2-16. FlashBAK Technology



Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

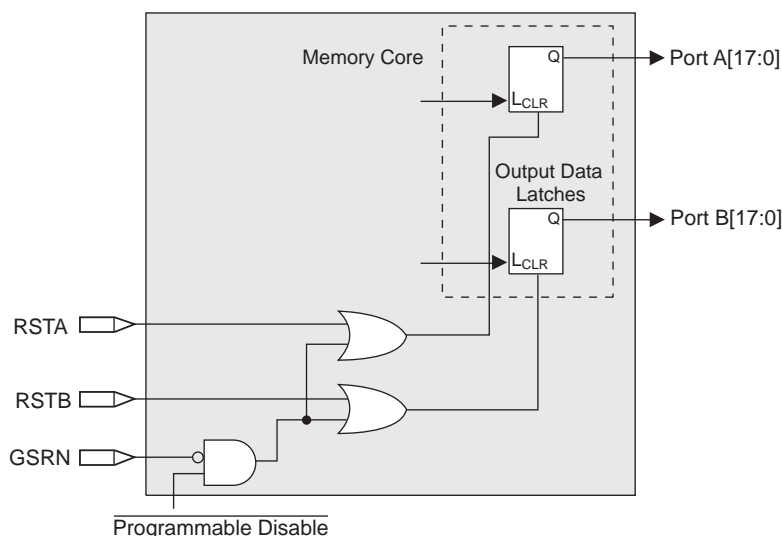
EBR memory supports two forms of write behavior for single port or dual port operation:

1. Normal – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. Write Through – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

Memory Core Reset

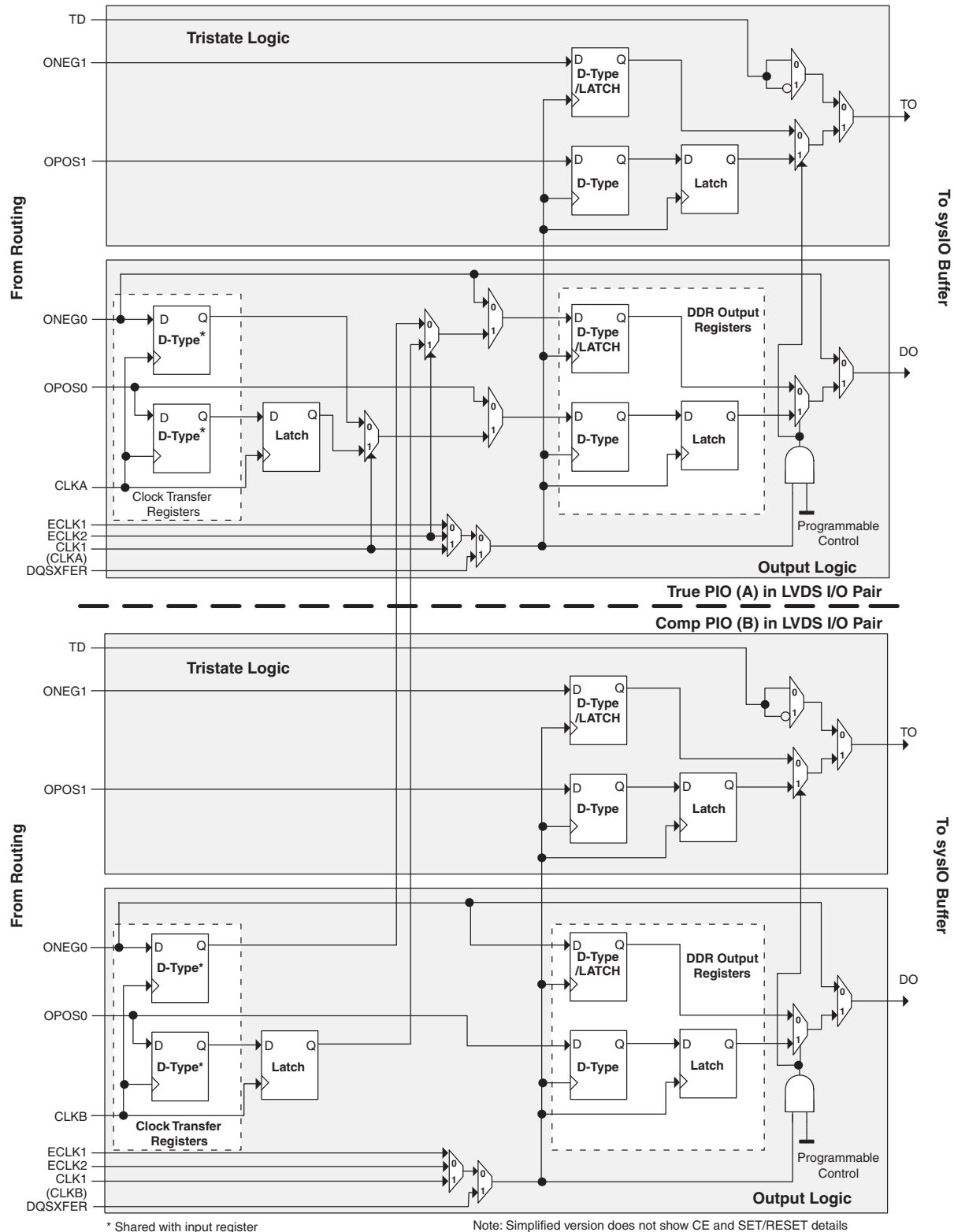
The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. GSRN, the global reset signal, resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-17.

Figure 2-17. Memory Core Reset



shows the diagram using this gearbox function. For more information on this topic, see TN1138, [LatticeXP2 High Speed I/O Interface](#).

Figure 2-27. Output and Tristate Block



LatticeXP2 devices contain two types of sysIO buffer pairs.

1. Top and Bottom (Banks 0, 1, 4 and 5) sysIO Buffer Pairs (Single-Ended Outputs Only)

The sysIO buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Only the I/Os on the top and bottom banks have programmable PCI clamps.

2. Left and Right (Banks 2, 3, 6 and 7) sysIO Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp pad is associated with the negative side of the differential I/O.

LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

Typical sysIO I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} , $V_{CCCONFIG}$ (V_{CCIO7}) and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. During power up and before the FPGA core logic becomes active, all user I/Os will be high-impedance with weak pull-up. Please refer to TN1136, [LatticeXP2 sysIO Usage Guide](#) for additional information.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported sysIO Standards

The LatticeXP2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8V, 2.5V and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, MLVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-12 and 2-13 show the I/O standards (together with their supply and reference voltages) supported by LatticeXP2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1136, [LatticeXP2 sysIO Usage Guide](#).

Absolute Maximum Ratings^{1, 2, 3}

Supply Voltage V_{CC} -0.5 to 1.32V

Supply Voltage V_{CCAUX} -0.5 to 3.75V

Supply Voltage V_{CCJ} -0.5 to 3.75V

Supply Voltage V_{CCPLL} ⁴ -0.5 to 3.75V

Output Supply Voltage V_{CCIO} -0.5 to 3.75V

Input or I/O Tristate Voltage Applied⁵ -0.5 to 3.75V

Storage Temperature (Ambient) -65 to 150°C

Junction Temperature Under Bias (T_j) +125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. V_{CCPLL} only available on csBGA, PQFP and TQFP packages.
5. Overshoot and undershoot of -2V to ($V_{IHMAX} + 2$) volts is permitted for a duration of <20 ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage	1.14	1.26	V
V_{CCAUX} ^{4, 5}	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCPLL} ¹	PLL Supply Voltage	3.135	3.465	V
V_{CCIO} ^{2, 3, 4}	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ} ²	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C

1. V_{CCPLL} only available on csBGA, PQFP and TQFP packages.
2. If V_{CCIO} or V_{CCJ} is set to 1.2 V, they must be connected to the same power supply as V_{CC} . If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX} .
3. See recommended voltages by I/O standard in subsequent table.
4. To ensure proper I/O behavior, V_{CCIO} must be turned off at the same time or earlier than V_{CCAUX} .
5. In fpBGA and ftBGA packages, the PLLs are connected to, and powered from, the auxiliary power supply.

On-Chip Flash Memory Specifications

Symbol	Parameter	Max.	Units
N_{PROG}	Flash Programming Cycles per $t_{RETENTION}$ ¹	10,000	Cycles
	Flash Functional Programming Cycles	100,000	

1. The minimum data retention, $t_{RETENTION}$, is 20 years.

Table 3-1. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/-1%)	158	Ω
R _P	Driver Parallel Resistor (+/-1%)	140	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage (after R _P)	1.43	V
V _{OL}	Output Low Voltage (after R _P)	1.07	V
V _{OD}	Output Differential Voltage (After R _P)	0.35	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	6.03	mA

LVC MOS33D

All I/O banks support emulated differential I/O using the LVC MOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3V V_{CCIO}. The default drive current for LVC MOS33D output is 12mA with the option to change the device strength to 4mA, 8mA, 16mA or 20mA. Follow the LVC MOS33 specifications for the DC characteristics of the LVC MOS33D.

LatticeXP2 External Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HE}	Clock to Data Hold - PIO Input Register	XP2-5	1.00	—	1.30	—	1.60	—	ns
		XP2-8	1.00	—	1.30	—	1.60	—	ns
		XP2-17	1.00	—	1.30	—	1.60	—	ns
		XP2-30	1.20	—	1.60	—	1.90	—	ns
		XP2-40	1.20	—	1.60	—	1.90	—	ns
t_{SU_DELE}	Clock to Data Setup - PIO Input Register with Data Input Delay	XP2-5	1.00	—	1.30	—	1.60	—	ns
		XP2-8	1.00	—	1.30	—	1.60	—	ns
		XP2-17	1.00	—	1.30	—	1.60	—	ns
		XP2-30	1.20	—	1.60	—	1.90	—	ns
		XP2-40	1.20	—	1.60	—	1.90	—	ns
t_{H_DELE}	Clock to Data Hold - PIO Input Register with Input Data Delay	XP2-5	0.00	—	0.00	—	0.00	—	ns
		XP2-8	0.00	—	0.00	—	0.00	—	ns
		XP2-17	0.00	—	0.00	—	0.00	—	ns
		XP2-30	0.00	—	0.00	—	0.00	—	ns
		XP2-40	0.00	—	0.00	—	0.00	—	ns
f_{MAX_IOE}	Clock Frequency of I/O and PFU Register	XP2	—	420	—	357	—	311	MHz
General I/O Pin Parameters (using Primary Clock with PLL)¹									
t_{COPLL}	Clock to Output - PIO Output Register	XP2-5	—	3.00	—	3.30	—	3.70	ns
		XP2-8	—	3.00	—	3.30	—	3.70	ns
		XP2-17	—	3.00	—	3.30	—	3.70	ns
		XP2-30	—	3.00	—	3.30	—	3.70	ns
		XP2-40	—	3.00	—	3.30	—	3.70	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	XP2-5	1.00	—	1.20	—	1.40	—	ns
		XP2-8	1.00	—	1.20	—	1.40	—	ns
		XP2-17	1.00	—	1.20	—	1.40	—	ns
		XP2-30	1.00	—	1.20	—	1.40	—	ns
		XP2-40	1.00	—	1.20	—	1.40	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	XP2-5	0.90	—	1.10	—	1.30	—	ns
		XP2-8	0.90	—	1.10	—	1.30	—	ns
		XP2-17	0.90	—	1.10	—	1.30	—	ns
		XP2-30	1.00	—	1.20	—	1.40	—	ns
		XP2-40	1.00	—	1.20	—	1.40	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	XP2-5	1.90	—	2.10	—	2.30	—	ns
		XP2-8	1.90	—	2.10	—	2.30	—	ns
		XP2-17	1.90	—	2.10	—	2.30	—	ns
		XP2-30	2.00	—	2.20	—	2.40	—	ns
		XP2-40	2.00	—	2.20	—	2.40	—	ns

LatticeXP2 Internal Switching Characteristics¹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RST_PIO}	Asynchronous reset time for PFU Logic	—	0.386	—	0.419	—	0.452	ns
t_{DEL}	Dynamic Delay Step Size	0.035	0.035	0.035	0.035	0.035	0.035	ns
EBR Timing								
t_{CO_EBR}	Clock (Read) to Output from Address or Data	—	2.774	—	3.142	—	3.510	ns
t_{COO_EBR}	Clock (Write) to Output from EBR Output Register	—	0.360	—	0.408	—	0.456	ns
t_{SUDATA_EBR}	Setup Data to EBR Memory (Write Clk)	-0.167	—	-0.198	—	-0.229	—	ns
t_{HDATA_EBR}	Hold Data to EBR Memory (Write Clk)	0.194	—	0.231	—	0.267	—	ns
t_{SUADDR_EBR}	Setup Address to EBR Memory (Write Clk)	-0.117	—	-0.137	—	-0.157	—	ns
t_{HADDR_EBR}	Hold Address to EBR Memory (Write Clk)	0.157	—	0.182	—	0.207	—	ns
t_{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory (Write/Read Clk)	-0.135	—	-0.159	—	-0.182	—	ns
t_{HWREN_EBR}	Hold Write/Read Enable to EBR Memory (Write/Read Clk)	0.158	—	0.186	—	0.214	—	ns
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register (Read Clk)	0.144	—	0.160	—	0.176	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register (Read Clk)	-0.097	—	-0.113	—	-0.129	—	ns
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register (Asynchronous)	—	1.156	—	1.341	—	1.526	ns
t_{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.117	—	-0.137	—	-0.157	—	ns
t_{HBE_EBR}	Byte Enable Hold Time to EBR Output Register Dynamic Delay on Each PIO	0.157	—	0.182	—	0.207	—	ns
t_{RSTREC_EBR}	Asynchronous reset recovery time for EBR	0.233	—	0.291	—	0.347	—	ns
t_{RST_EBR}	Asynchronous reset time for EBR	—	1.156	—	1.341	—	1.526	ns
PLL Parameters								
$t_{RSTKREC_PLL}$	After RSTK De-assert, Recovery Time Before Next Clock Edge Can Toggle K-divider Counter	1.000	—	1.000	—	1.000	—	ns
t_{RSTREC_PLL}	After RST De-assert, Recovery Time Before Next Clock Edge Can Toggle M-divider Counter (Applies to M-Divider Portion of RST Only ²)	1.000	—	1.000	—	1.000	—	ns
DSP Block Timing								
t_{SUI_DSP}	Input Register Setup Time	0.135	—	0.151	—	0.166	—	ns
t_{HI_DSP}	Input Register Hold Time	0.021	—	-0.006	—	-0.031	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	2.505	—	2.784	—	3.064	—	ns

LatticeXP2 Internal Switching Characteristics¹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HP_DSP}	Pipeline Register Hold Time	-0.787	—	-0.890	—	-0.994	—	ns
t_{SUO_DSP}	Output Register Setup Time	4.896	—	5.413	—	5.931	—	ns
t_{HO_DSP}	Output Register Hold Time	-1.439	—	-1.604	—	-1.770	—	ns
$t_{COI_DSP}^3$	Input Register Clock to Output Time	—	4.513	—	4.947	—	5.382	ns
$t_{COP_DSP}^3$	Pipeline Register Clock to Output Time	—	2.153	—	2.272	—	2.391	ns
$t_{COO_DSP}^3$	Output Register Clock to Output Time	—	0.569	—	0.600	—	0.631	ns
$t_{SUADSUB}$	AdSub Input Register Setup Time	-0.270	—	-0.298	—	-0.327	—	ns
t_{HADSUB}	AdSub Input Register Hold Time	0.306	—	0.338	—	0.371	—	ns

1. Internal parameters are characterized, but not tested on every device.

2. RST resets VCO and all counters in PLL.

3. These parameters include the Adder Subtractor block in the path.

Flash Download Time (from On-Chip Flash to SRAM)

Over Recommended Operating Conditions

Symbol	Parameter		Min.	Typ.	Max.	Units
t_{REFRESH}	PROGRAMN Low-to-High. Transition to Done High.	XP2-5	—	1.8	2.1	ms
		XP2-8	—	1.9	2.3	ms
		XP2-17	—	1.7	2.0	ms
		XP2-30	—	2.0	2.1	ms
		XP2-40	—	2.0	2.3	ms
	Power-up refresh when PROGRAMN is pulled up to V_{CC} ($V_{CC}=V_{CC}$ Min)	XP2-5	—	1.8	2.1	ms
		XP2-8	—	1.9	2.3	ms
		XP2-17	—	1.7	2.0	ms
		XP2-30	—	2.0	2.1	ms
		XP2-40	—	2.0	2.3	ms

Flash Program Time

Over Recommended Operating Conditions

Device	Flash Density		Program Time	Units
			Typ.	
XP2-5	1.2M	TAG	1.0	ms
		Main Array	1.1	s
XP2-8	2.0M	TAG	1.0	ms
		Main Array	1.4	s
XP2-17	3.6M	TAG	1.0	ms
		Main Array	1.8	s
XP2-30	6.0M	TAG	2.0	ms
		Main Array	3.0	s
XP2-40	8.0M	TAG	2.0	ms
		Main Array	4.0	s

Flash Erase Time

Over Recommended Operating Conditions

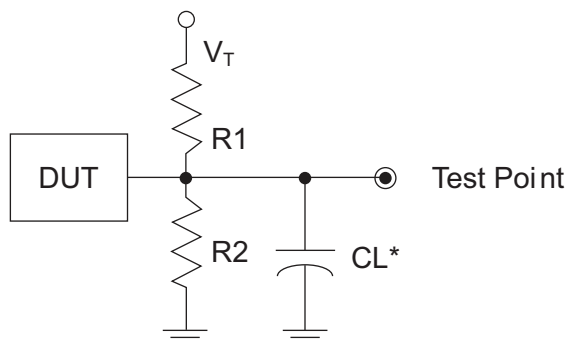
Device	Flash Density		Erase Time	Units
			Typ.	
XP2-5	1.2M	TAG	1.0	s
		Main Array	3.0	s
XP2-8	2.0M	TAG	1.0	s
		Main Array	4.0	s
XP2-17	3.6M	TAG	1.0	s
		Main Array	5.0	s
XP2-30	6.0M	TAG	2.0	s
		Main Array	7.0	s
XP2-40	8.0M	TAG	2.0	s
		Main Array	9.0	s

[illegible]

Switching Test Conditions

Figure 3-11 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

Figure 3-11. Output Test Load, LVTTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-6. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R ₁	R ₂	C _L	Timing Ref.	V _T
LVTTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.5 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	∞	1M Ω		$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> L)	1M Ω	∞		$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H -> Z)	∞	100		$V_{OH} - 0.10$	—
LVCMOS 2.5 I/O (L -> Z)	100	∞		$V_{OL} + 0.10$	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

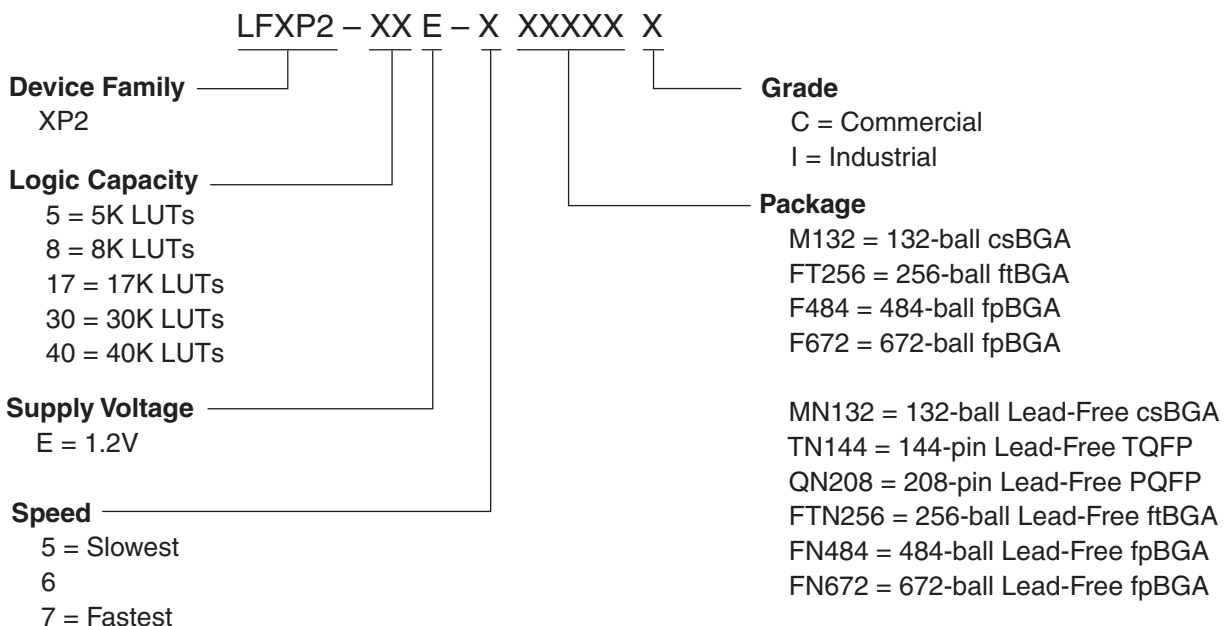
Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	<p>[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).</p> <p>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.</p> <p>[A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.</p>
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
GND	—	Ground. Dedicated pins.
V _{CC}	—	Power supply pins for core logic. Dedicated pins.
V _{CCAUX}	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers.
V _{CCPLL}	—	PLL supply pins. csBGA, PQFP and TQFP packages only.
V _{CCIOx}	—	Dedicated power supply pins for I/O bank x.
V _{REF1_x} , V _{REF2_x}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V _{REF} inputs. When not used, they may be used as I/O pins.
PLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_V _{CCPLL}	—	Power supply pin for PLL: LLC, LRC, URC, ULC, num = row from center.
[LOC][num]_GPLL[T, C]_IN_A	I	General Purpose PLL (GPLL) input pads: LLC, LRC, URC, ULC, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_GPLL[T, C]_FB_A	I	Optional feedback GPLL input pads: LLC, LRC, URC, ULC, num = row from center, T = true and C = complement, index A,B,C...at each side.
PCLK[T, C]_[n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank.
[LOC]DQS[num]	I	DQS input pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = ball function number. Any pad can be configured to be output.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.

Pin Information Summary

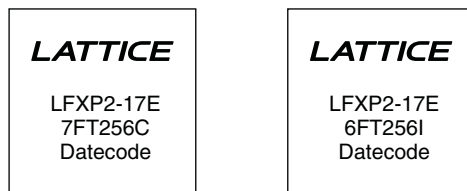
Pin Type		XP2-5				XP2-8				XP2-17			XP2-30			XP2-40	
		132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
Single Ended User I/O		86	100	146	172	86	100	146	201	146	201	358	201	363	472	363	540
Differential Pair User I/O	Normal	35	39	57	66	35	39	57	77	57	77	135	77	137	180	137	204
	Highspeed	8	11	16	20	8	11	16	23	16	23	44	23	44	56	44	66
Configuration	TAP	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
	Muxed	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9
	Dedicated	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Non Configuration	Muxed	5	5	7	7	7	7	9	9	11	11	21	7	11	13	11	13
	Dedicated	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Vcc		6	4	9	6	6	4	9	6	9	6	16	6	16	20	16	20
Vccaux		4	4	4	4	4	4	4	4	4	4	8	4	8	8	8	8
VCCPLL		2	2	2	-	2	2	2	-	4	-	-	-	-	-	-	-
VCCIO	Bank0	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
	Bank1	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank2	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
	Bank3	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank4	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank5	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
	Bank6	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank7	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
GND, GND0-GND7		15	15	20	20	15	15	22	20	22	20	56	20	56	64	56	64
NC		-	-	4	31	-	-	2	2	-	2	7	2	2	69	2	1
Single Ended/ Differential I/O per Bank	Bank0	18/9	20/10	20/10	26/13	18/9	20/10	20/10	28/14	20/10	28/14	52/26	28/14	52/26	70/35	52/26	70/35
	Bank1	4/2	6/3	18/9	18/9	4/2	6/3	18/9	22/11	18/9	22/11	36/18	22/11	36/18	54/27	36/18	70/35
	Bank2	16/8	18/9	18/9	22/11	16/8	18/9	18/9	26/13	18/9	26/13	46/23	26/13	46/23	56/28	46/23	64/32
	Bank3	4/2	4/2	16/8	20/10	4/2	4/2	16/8	24/12	16/8	24/12	44/22	24/12	46/23	56/28	46/23	66/33
	Bank4	8/4	8/4	18/9	18/9	8/4	8/4	18/9	26/13	18/9	26/13	36/18	26/13	38/19	54/27	38/19	70/35
	Bank5	14/7	18/9	20/10	24/12	14/7	18/9	20/10	24/12	20/10	24/12	52/26	24/12	53/26	70/35	53/26	70/35
	Bank6	6/3	8/4	18/9	22/11	6/3	8/4	18/9	27/13	18/9	27/13	46/23	27/13	46/23	56/28	46/23	66/33
	Bank7	16/8	18/9	18/9	22/11	16/8	18/9	18/9	24/12	18/9	24/12	46/23	24/12	46/23	56/28	46/23	64/32
True LVDS Pairs Bonding Out per Bank	Bank0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank2	3	4	4	5	3	4	4	6	4	6	11	6	11	14	11	16
	Bank3	1	1	4	5	1	1	4	6	4	6	11	6	11	14	11	17
	Bank4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank6	1	2	4	5	1	2	4	6	4	6	11	6	11	14	11	17
	Bank7	3	4	4	5	3	4	4	5	4	5	11	5	11	14	11	16
DDR Banks Bonding Out per I/O Bank ¹	Bank0	1	1	1	1	1	1	1	1	1	1	3	1	2	4	2	4
	Bank1	0	0	1	1	0	0	1	1	1	1	2	1	2	3	2	4
	Bank2	1	1	1	1	1	1	1	1	1	1	2	1	3	3	3	4
	Bank3	0	0	1	1	0	0	1	1	1	1	2	1	3	3	3	4
	Bank4	0	0	1	1	0	0	1	1	1	1	2	1	2	3	2	4
	Bank5	1	1	1	1	1	1	1	1	1	1	3	1	2	4	2	4
	Bank6	0	0	1	1	0	0	1	1	1	1	2	1	3	3	3	4
	Bank7	1	1	1	1	1	1	1	1	1	1	2	1	3	3	3	4

Part Number Description



Ordering Information

The LatticeXP2 devices are marked with a single temperature grade, either Commercial or Industrial, as shown below.



For Further Information

A variety of technical notes for the LatticeXP2 FPGA family are available on the Lattice Semiconductor web site at www.latticesemi.com.

- TN1136, [LatticeXP2 sysIO Usage Guide](#)
- TN1137, [LatticeXP2 Memory Usage Guide](#)
- TN1138, [LatticeXP2 High Speed I/O Interface](#)
- TN1126, [LatticeXP2 sysCLOCK PLL Design and Usage Guide](#)
- TN1139, [Power Estimation and Management for LatticeXP2 Devices](#)
- TN1140, [LatticeXP2 sysDSP Usage Guide](#)
- TN1141, [LatticeXP2 sysCONFIG Usage Guide](#)
- TN1142, [LatticeXP2 Configuration Encryption and Security Usage Guide](#)
- TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#)
- TN1220, [LatticeXP2 Dual Boot Feature](#)
- TN1130, [LatticeXP2 Soft Error Detection \(SED\) Usage Guide](#)
- TN1143, [LatticeXP2 Hardware Checklist](#)

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com

Revision History

Date	Version	Section	Change Summary
May 2007	01.1	—	Initial release.
September 2007	01.2	DC and Switching Characteristics	Added JTAG Port Timing Waveforms diagram.
			Updated sysCLOCK PLL Timing table.
		Pinout Information	Added Thermal Management text section.
February 2008	01.3	Architecture	Added LVC MOS33D to Supported Output Standards table.
			Clarified: "This Flash can be programmed through either the JTAG or Slave SPI ports of the device. The SRAM configuration space can also be infinitely reconfigured through the JTAG and Master SPI ports."
			Added External Slave SPI Port to Serial TAG Memory section. Updated Serial TAG Memory diagram.
		DC and Switching Characteristics	Updated Flash Programming Specifications table.
			Added "8W" specification to Hot Socketing Specifications table.
			Updated Timing Tables
			Clarifications for IIH in DC Electrical Characteristics table.
			Added LVC MOS33D section
			Updated DOA and DOA (Regs) to EBR Timing diagrams.
			Removed Master Clock Frequency and Duty Cycle sections from the LatticeXP2 sysCONFIG Port Timing Specifications table. These are listed on the On-chip Oscillator and Configuration Master Clock Characteristics table.
			Changed CSSPIN to CSSPISN in description of t_{SCS} , t_{SCSS} , and t_{SCSH} parameters. Removed t_{SOE} parameter.
			Clarified On-chip Oscillator documentation
			Added Switching Test Conditions
		Pinout Information	Added "True LVDS Pairs Bonding Out per Bank," "DDR Banks Bonding Out per I/O Bank," and "PCI capable I/Os Bonding Out per Bank" to Pin Information Summary in place of previous blank table "PCI and DDR Capabilities of the Device-Package Combinations"
			Removed pinout listing. This information is available on the LatticeXP2 product web pages
		Ordering Information	Added XP2-17 "8W" and all other family OPNs.
April 2008	01.4	DC and Switching Characteristics	Updated Absolute Maximum Ratings footnotes.
			Updated Recommended Operating Conditions Table footnotes.
			Updated Supply Current (Standby) Table
			Updated Initialization Supply Current Table
			Updated Programming and Erase Flash Supply Current Table
			Updated Register to Register Performance Table
			Updated LatticeXP2 External Switching Characteristics Table
			Updated LatticeXP2 Internal Switching Characteristics Table
			Updated sysCLOCK PLL Timing Table