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**Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

**Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

## Details

| | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 5000 |
| Number of Logic Elements/Cells | 40000 |
| Total RAM Bits | 906240 |
| Number of I/O | 540 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 672-BBGA |
| Supplier Device Package | 672-FPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-40e-5fn672c |

## Architecture Overview

Each LatticeXP2 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and a row of sysDSP™ Digital Signal Processing blocks as shown in Figure 2-1.

On the left and right sides of the Programmable Functional Unit (PFU) array, there are Non-volatile Memory Blocks. In configuration mode the nonvolatile memory is programmed via the IEEE 1149.1 TAP port or the sysCONFIG™ peripheral port. On power up, the configuration data is transferred from the Non-volatile Memory Blocks to the configuration SRAM. With this technology, expensive external configuration memory is not required, and designs are secured from unauthorized read-back. This transfer of data from non-volatile memory to configuration SRAM via wide busses happens in microseconds, providing an "instant-on" capability that allows easy interfacing in many applications. LatticeXP2 devices can also transfer data from the sysMEM EBR blocks to the Non-volatile Memory Blocks at user request.

There are two kinds of logic blocks, the PFU and the PFU without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

LatticeXP2 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large dedicated 18Kbit memory blocks. Each sysMEM block can be configured in a variety of depths and widths of RAM or ROM. In addition, LatticeXP2 devices contain up to two rows of DSP Blocks. Each DSP block has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysIO buffers. The sysIO buffers of the LatticeXP2 devices are arranged into eight banks, allowing the implementation of a wide variety of I/O standards. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as 7:1 LVDS interfaces, found in many display applications, and memory interfaces including DDR and DDR2.
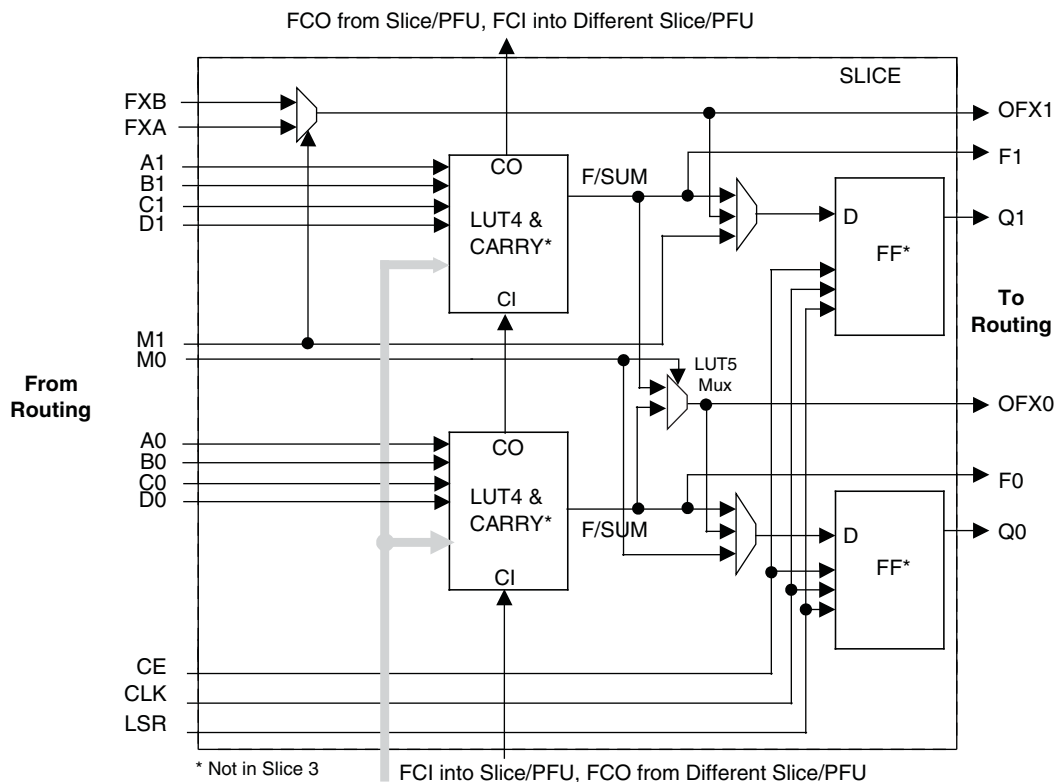
The LatticeXP2 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

Other blocks provided include PLLs and configuration functions. The LatticeXP2 architecture provides up to four General Purpose PLLs (GPLL) per device. The GPLL blocks are located in the corners of the device.

The configuration block that supports features such as configuration bit-stream de-encryption, transparent updates and dual boot support is located between banks two and three. Every device in the LatticeXP2 family supports a sysCONFIG port, muxed with bank seven I/Os, which supports serial device configuration. A JTAG port is provided between banks two and three.

This family also provides an on-chip oscillator. LatticeXP2 devices use 1.2V as their core voltage.

*Figure 2-3. Slice Diagram*



FCO from Slice/PFU, FCI into Different Slice/PFU

SLICE

* Not in Slice 3

FCI into Slice/PFU, FCO from Different Slice/PFU

For Slices 0 and 2, memory control signals are generated from Slice 1 as follows:
WCK is CLK
WRE is from LSR
DI[3:2] for Slice 2 and DI[1:0] for Slice 0 data
WAD [A:D] is a 4bit address from slice 1 LUT input

*Table 2-2. Slice Signal Descriptions*

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Multi-purpose | M0 | Multipurpose Input |
| Input | Multi-purpose | M1 | Multipurpose Input |
| Input | Control signal | CE | Clock Enable |
| Input | Control signal | LSR | Local Set/Reset |
| Input | Control signal | CLK | System Clock |
| Input | Inter-PFU signal | FCI | Fast Carry-In[1] |
| Input | Inter-slice signal | FXA | Intermediate signal to generate LUT6 and LUT7 |
| Input | Inter-slice signal | FXB | Intermediate signal to generate LUT6 and LUT7 |
| Output | Data signals | F0, F1 | LUT4 output register bypass signals |
| Output | Data signals | Q0, Q1 | Register outputs |
| Output | Data signals | OFX0 | Output of a LUT5 MUX |
| Output | Data signals | OFX1 | Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice |
| Output | Inter-PFU signal | FCO | Slice 2 of each PFU is the fast carry chain output[1] |

1. See Figure 2-3 for connection details.
2. Requires two PFUs.
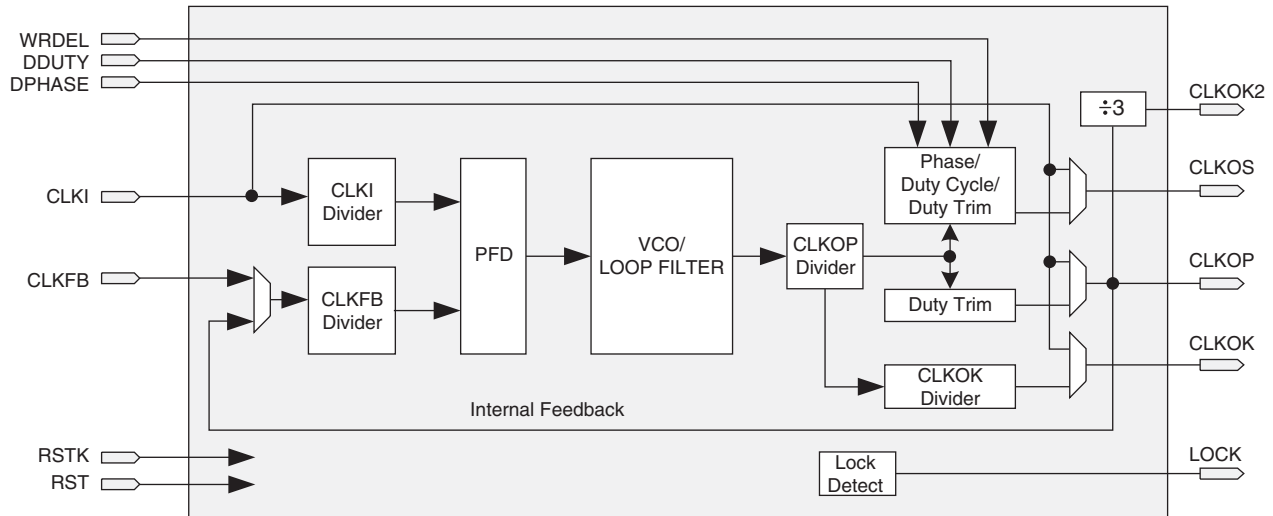
*Figure 2-4. General Purpose PLL (GPLL) Diagram*



Table 2-4 provides a description of the signals in the GPLL blocks.

*Table 2-4. GPLL Block Signal Descriptions*

| Signal | I/O | Description |
|---|---|---|
| CLKI | I | Clock input from external pin or routing |
| CLKFB | I | PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic) |
| RST | I | "1" to reset PLL counters, VCO, charge pumps and M-dividers |
| RSTK | I | "1" to reset K-divider |
| DPHASE [3:0] | I | DPA Phase Adjust input |
| DDDUTY [3:0] | I | DPA Duty Cycle Select input |
| WRDEL | I | DPA Fine Delay Adjust input |
| CLKOS | O | PLL output clock to clock tree (phase shifted/duty cycle changed) |
| CLKOP | O | PLL output clock to clock tree (no phase shift) |
| CLKOK | O | PLL output to clock tree through secondary clock divider |
| CLKOK2 | O | PLL output to clock tree (CLKOP divided by 3) |
| LOCK | O | "1" indicates PLL LOCK to CLKI |

# Clock Dividers

LatticeXP2 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from the CLKOP output from the GPLLs or from the Edge Clocks (ECLK). The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets the input and forces all outputs to low. The RELEASE signal releases outputs to the input clock. For further information on clock dividers, please see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide. Figure 2-5 shows the clock divider connections.

*Figure 2-6. Primary Clock Sources for XP2-17*



**Primary Clock Sources
to Eight Quadrant Clock Selection**
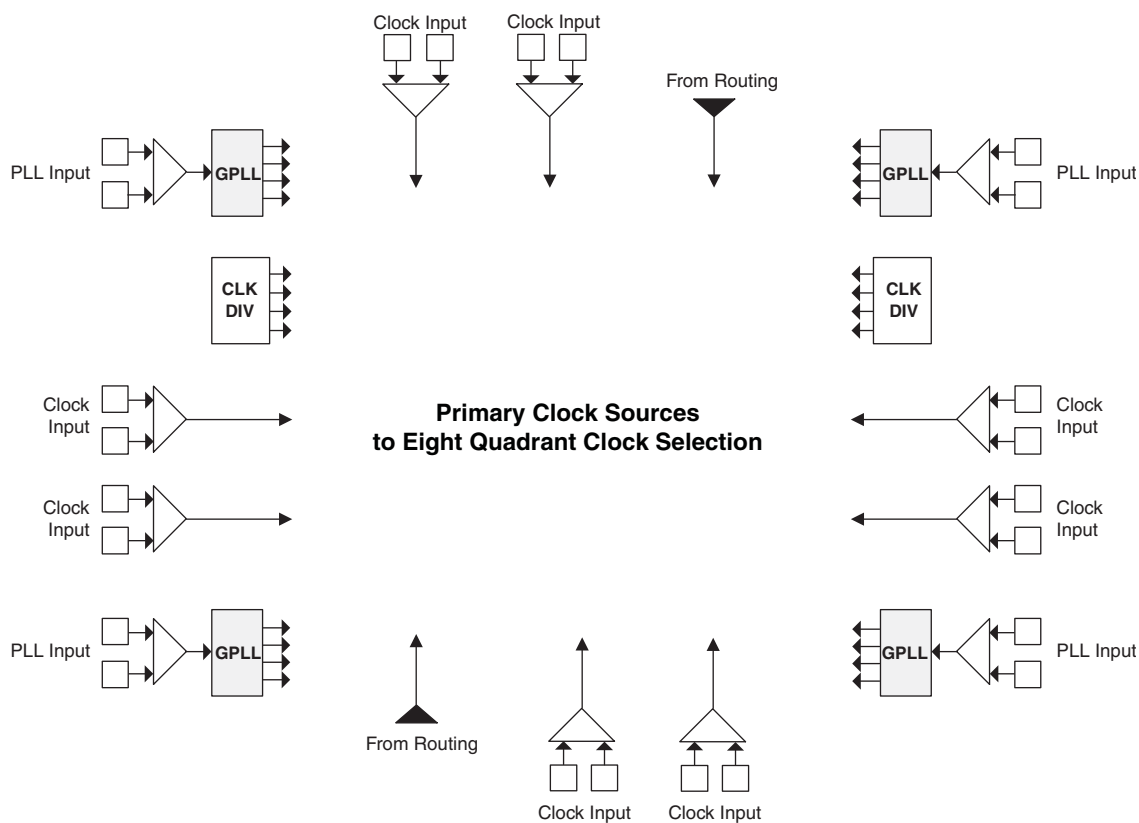
Note: This diagram shows sources for the XP2-17 device. Smaller LatticeXP2 devices have two GPLLs.

## MAC sysDSP Element

In this case, the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers but the output register is always enabled. The output register is used to store the accumulated value. The Accumulators in the DSP blocks in LatticeXP2 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-21 shows the MAC sysDSP element.

*Figure 2-21. MAC sysDSP*
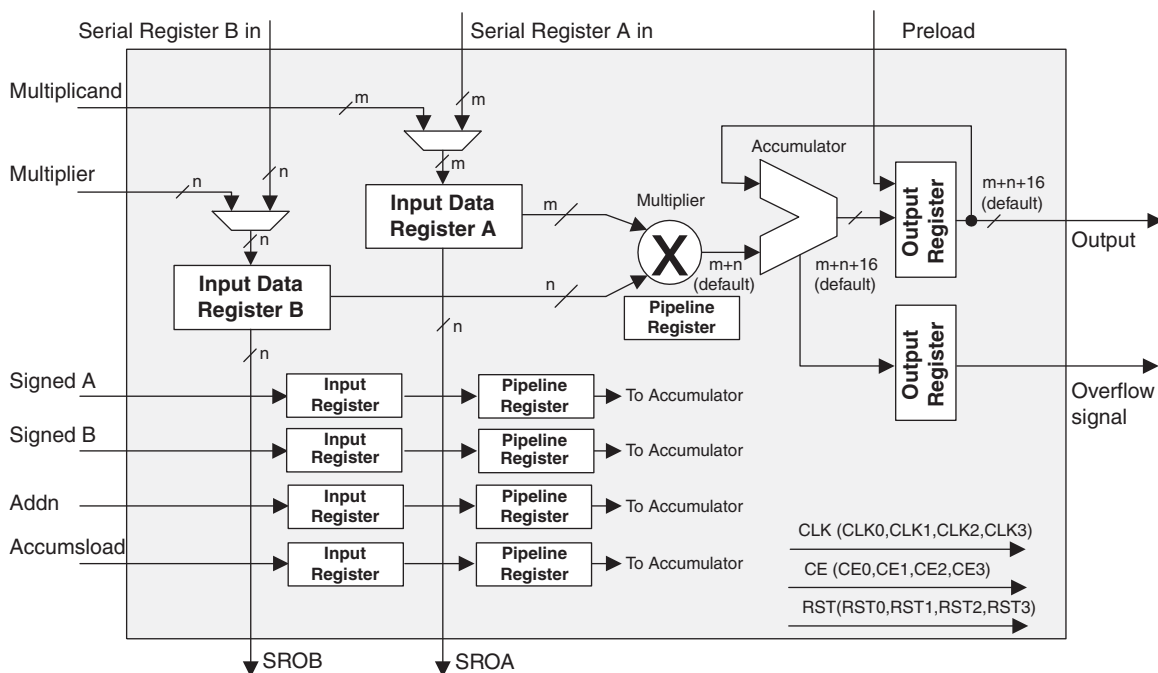
## IPexpress™

The user can access the sysDSP block via the Lattice IPexpress tool, which provides the option to configure each DSP module (or group of modules), or by direct HDL instantiation. In addition, Lattice has partnered with The Math-Works® to support instantiation in the Simulink® tool, a graphical simulation environment. Simulink works with Diamond to dramatically shorten the DSP design cycle in Lattice FPGAs.

# Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LatticeXP2 DSP include the Bit Correlator, FFT functions, FIR Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IP cores.

## Resources Available in the LatticeXP2 Family

Table 2-8 shows the maximum number of multipliers for each member of the LatticeXP2 family. Table 2-9 shows the maximum available EBR RAM Blocks and Serial TAG Memory bits in each LatticeXP2 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

*Table 2-8. Maximum Number of DSP Blocks in the LatticeXP2 Family*

| Device | DSP Block | 9x9 Multiplier | 18x18 Multiplier | 36x36 Multiplier |
|--------|-----------|----------------|------------------|------------------|
| XP2-5  | 3 | 24 | 12 | 3 |
| XP2-8  | 4 | 32 | 16 | 4 |
| XP2-17 | 5 | 40 | 20 | 5 |
| XP2-30 | 7 | 56 | 28 | 7 |
| XP2-40 | 8 | 64 | 32 | 8 |

*Table 2-9. Embedded SRAM/TAG Memory in the LatticeXP2 Family*

| Device | EBR SRAM Block | Total EBR SRAM (Kbits) | TAG Memory (Bits) |
|--------|----------------|------------------------|-------------------|
| XP2-5  | 9  | 166 | 632 |
| XP2-8  | 12 | 221 | 768 |
| XP2-17 | 15 | 276 | 2184 |
| XP2-30 | 21 | 387 | 2640 |
| XP2-40 | 48 | 885 | 3384 |

## LatticeXP2 DSP Performance

Table 2-10 lists the maximum performance in Millions of MAC (MMAC) operations per second for each member of the LatticeXP2 family.

*Table 2-10. DSP Performance*

| Device | DSP Block | DSP Performance MMAC |
|--------|-----------|----------------------|
| XP2-5  | 3 | 3,900 |
| XP2-8  | 4 | 5,200 |
| XP2-17 | 5 | 6,500 |
| XP2-30 | 7 | 9,100 |
| XP2-40 | 8 | 10,400 |

For further information on the sysDSP block, please see TN1140, LatticeXP2 sysDSP Usage Guide.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.

*Figure 2-26. Input Register Block*



1. Shared with output register
2. Selected PIO.

Note: Simplified version does not show CE and SET/RESET details
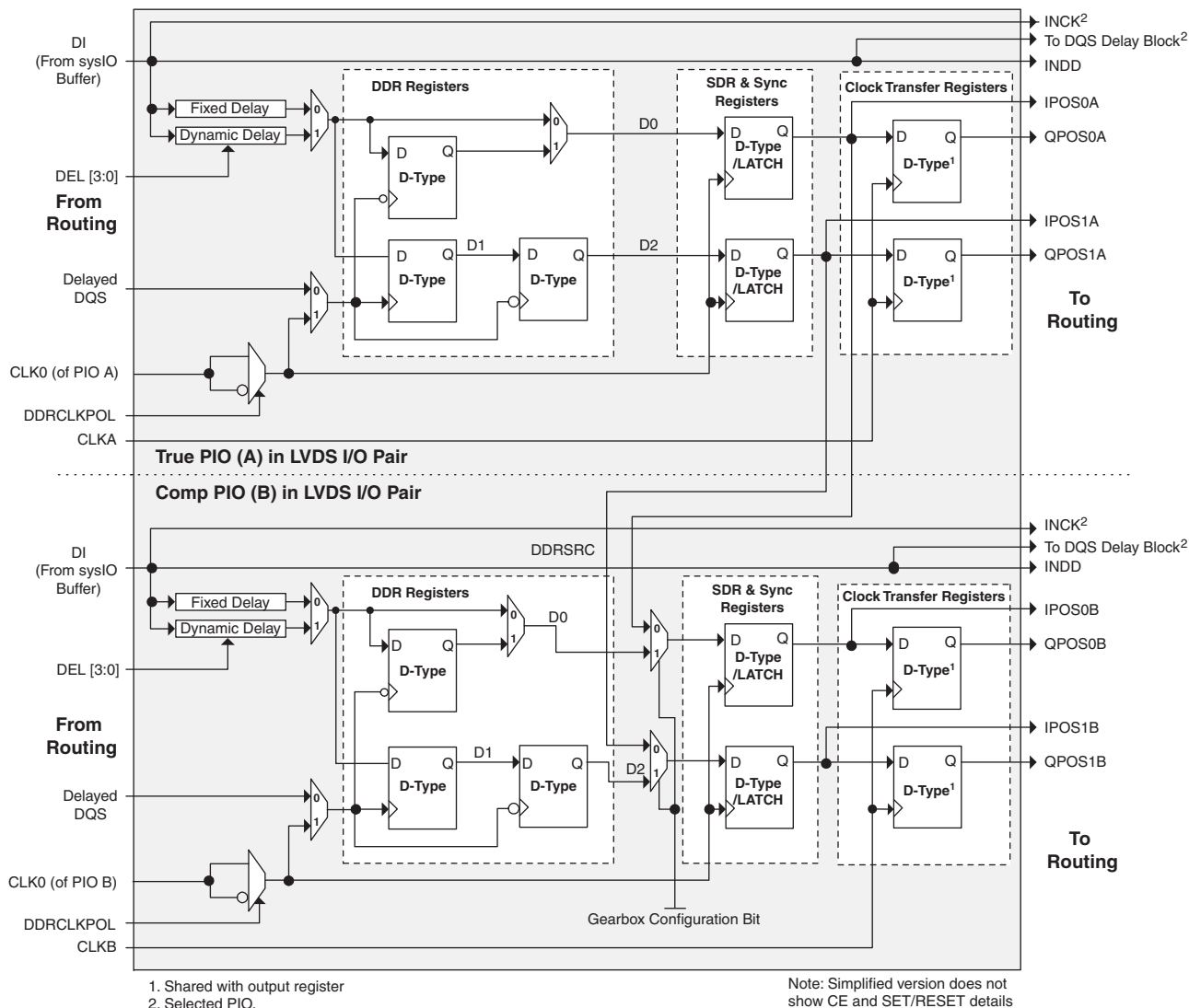
## Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The blocks on the PIOs on the left, right and bottom contain registers for SDR operation that are combined with an additional latch for DDR operation. Figure 2-27 shows the diagram of the Output Register Block for PIOs.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or latch. In DDR mode, ONEG0 and OPOS0 are fed into registers on the positive edge of the clock. At the next clock cycle the registered OPOS0 is latched. A multiplexer running off the same clock cycle selects the correct register to feed the output (D0).

By combining output blocks of the complementary PIOs and sharing some registers from input blocks, a gearbox function can be implemented, to take four data streams ONEG0A, ONEG1A, ONEG1B and ONEG1B. Figure 2-27

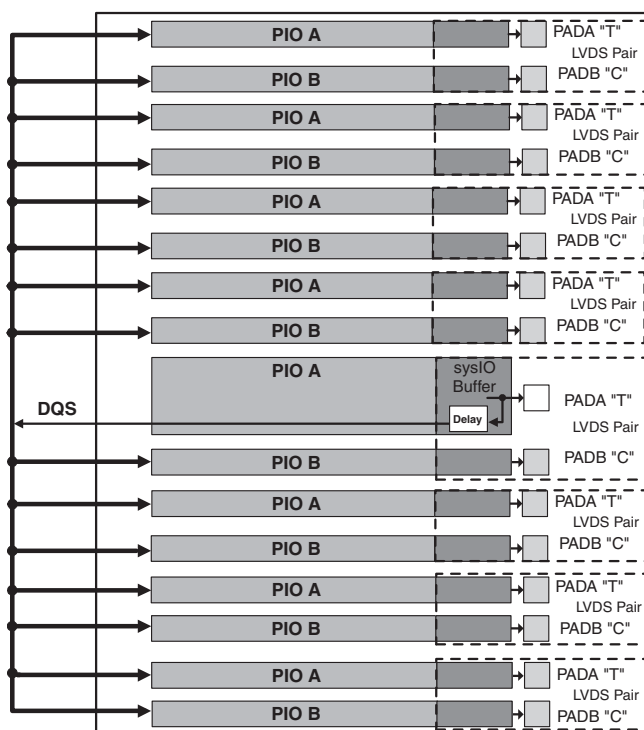*Figure 2-28. DQS Input Routing (Left and Right)*



*Figure 2-29. DQS Input Routing (Top and Bottom)*
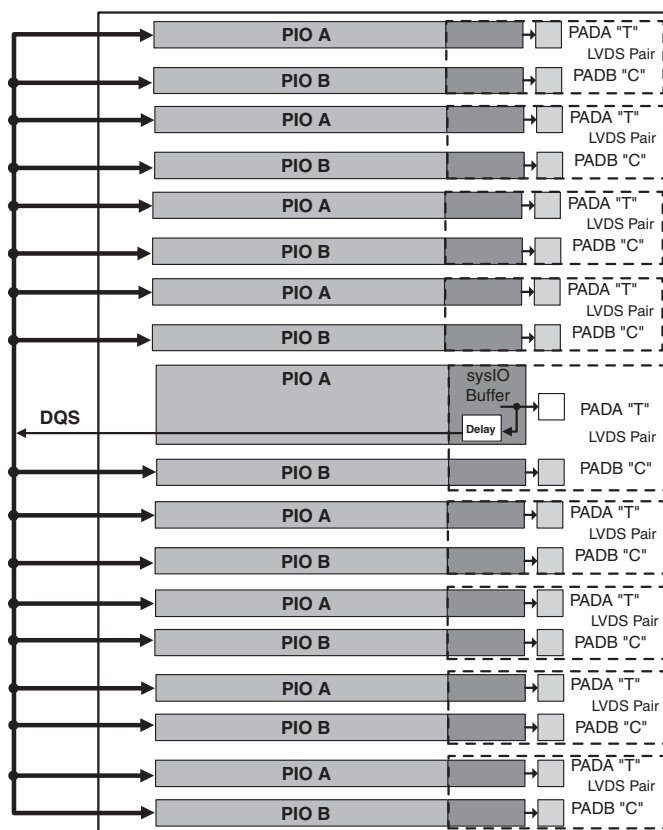
*Table 2-12. Supported Input Standards*

| Input Standard | $V_{REF}$ (Nom.) | $V_{CCIO}$[1] (Nom.) |
|---|---|---|
| **Single Ended Interfaces** | | |
| LVTTL | — | — |
| LVCMOS33 | — | — |
| LVCMOS25 | — | — |
| LVCMOS18 | — | 1.8 |
| LVCMOS15 | — | 1.5 |
| LVCMOS12 | — | — |
| PCI33 | — | — |
| HSTL18 Class I, II | 0.9 | — |
| HSTL15 Class I | 0.75 | — |
| SSTL33 Class I, II | 1.5 | — |
| SSTL25 Class I, II | 1.25 | — |
| SSTL18 Class I, II | 0.9 | — |
| **Differential Interfaces** | | |
| Differential SSTL18 Class I, II | — | — |
| Differential SSTL25 Class I, II | — | — |
| Differential SSTL33 Class I, II | — | — |
| Differential HSTL15 Class I | — | — |
| Differential HSTL18 Class I, II | — | — |
| LVDS, MLVDS, LVPECL, BLVDS, RSDS | — | — |

1. When not specified, $V_{CCIO}$ can be set anywhere in the valid operating range (page 3-1).

and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage $V_{CCJ}$ and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards. For more information, please see TN1141, LatticeXP2 sysCONFIG Usage Guide.

# flexiFLASH Device Configuration

The LatticeXP2 devices combine Flash and SRAM on a single chip to provide users with flexibility in device programming and configuration. Figure 2-33 provides an overview of the arrangement of Flash and SRAM configuration cells within the device. The remainder of this section provides an overview of these capabilities. See TN1141, LatticeXP2 sysCONFIG Usage Guide for a more detailed description.

*Figure 2-33. Overview of Flash and SRAM Configuration Cells Within LatticeXP2 Devices*
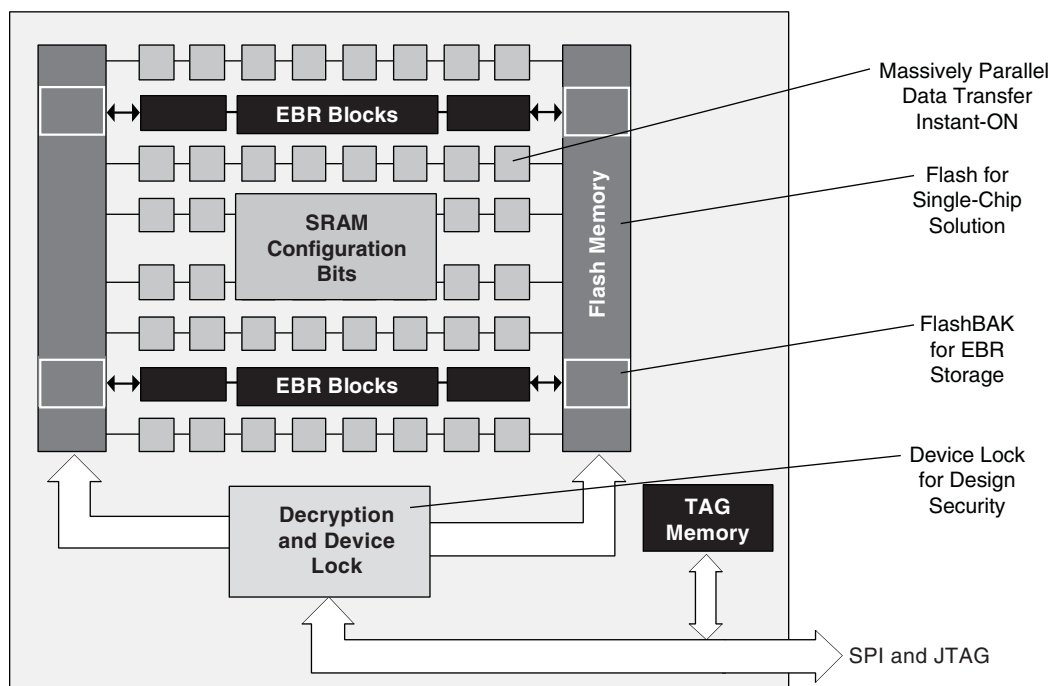


At power-up, or on user command, data is transferred from the on-chip Flash memory to the SRAM configuration cells that control the operation of the device. This is done with massively parallel buses enabling the parts to operate within microseconds of the power supplies reaching valid levels; this capability is referred to as Instant-On.

The on-chip Flash enables a single-chip solution eliminating the need for external boot memory. This Flash can be programmed through either the JTAG or Slave SPI ports of the device. The SRAM configuration space can also be infinitely reconfigured through the JTAG and Master SPI ports. The JTAG port is IEEE 1149.1 and IEEE 1532 compliant.

As described in the EBR section of the data sheet, the FlashBAK capability of the parts enables the contents of the EBR blocks to be written back into the Flash storage area without erasing or reprogramming other aspects of the device configuration. Serial TAG memory is also available to allow the storage of small amounts of data such as calibration coefficients and error codes.

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM only FPGAs. This is further enhanced by device locking. The device can be in one of three modes:

1. Unlocked

2. Key Locked – Presenting the key through the programming interface allows the device to be unlocked.

3. Permanently Locked – The device is permanently locked.

To further complement the security of the device a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash portion of the device.

## Serial TAG Memory

LatticeXP2 devices offer 0.6 to 3.3kbits of Flash memory in the form of Serial TAG memory. The TAG memory is an area of the on-chip Flash that can be used for non-volatile storage including electronic ID codes, version codes, date stamps, asset IDs and calibration settings. A block diagram of the TAG memory is shown in Figure 2-34. The TAG memory is accessed in the same way as external SPI Flash and it can be read or programmed either through JTAG, an external Slave SPI Port, or directly from FPGA logic. To read the TAG memory, a start address is specified and the entire TAG memory contents are read sequentially in a first-in-first-out manner. The TAG memory is independent of the Flash used for device configuration and given its use for general-purpose storage functions is always accessible regardless of the device security settings. For more information, see TN1137, LatticeXP2 Memory Usage Guide and TN1141, LatticeXP2 sysCONFIG Usage Guide.

*Figure 2-34. Serial TAG Memory Diagram*
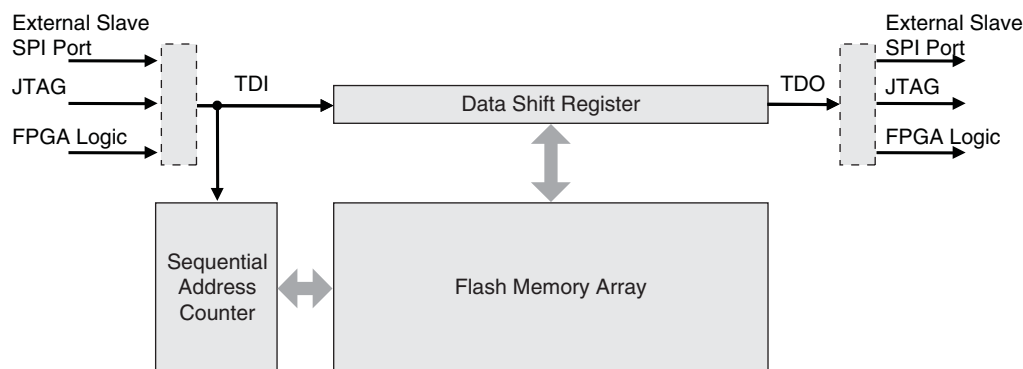


## Live Update Technology

Many applications require field updates of the FPGA. LatticeXP2 devices provide three features that enable this configuration to be done in a secure and failsafe manner while minimizing impact on system operation.

1. **Decryption Support**
   LatticeXP2 devices provide on-chip, non-volatile key storage to support decryption of a 128-bit AES encrypted bitstream, securing designs and deterring design piracy.

2. **TransFR (Transparent Field Reconfiguration)**
   TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. For more information please see TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

3. **Dual Boot Image Support**
   Dual boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeXP2 can be re-booted from this new configuration file. If there is a problem such as corrupt data during download or incorrect version number with this new boot image, the LatticeXP2 device can revert back to the

original backup configuration and try again. This all can be done without power cycling the system. For more information please see TN1220, LatticeXP2 Dual Boot Feature.

For more information on device configuration, please see TN1141, LatticeXP2 sysCONFIG Usage Guide.

## Soft Error Detect (SED) Support

LatticeXP2 devices have dedicated logic to perform Cyclic Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, LatticeXP2 devices can be programmed for checking soft errors in SRAM. SED can be run on a programmed device when the user logic is not active. In the event a soft error occurs, the device can be programmed to either reload from a known good boot image (from internal Flash or external SPI memory) or generate an error signal.

For further information on SED support, please see TN1130, LatticeXP2 Soft Error Detection (SED) Usage Guide.

## On-Chip Oscillator

Every LatticeXP2 device has an internal CMOS oscillator that is used to derive a Master Clock (CCLK) for configuration. The oscillator and CCLK run continuously and are available to user logic after configuration is complete. The available CCLK frequencies are listed in Table 2-14. When a different CCLK frequency is selected during the design process, the following sequence takes place:

1. Device powers up with the default CCLK frequency.

2. During configuration, users select a different CCLK frequency.

3. CCLK frequency changes to the selected frequency after clock configuration bits are received.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1141, LatticeXP2 sysCONFIG Usage Guide.

*Table 2-14. Selectable CCLKs and Oscillator Frequencies During Configuration and User Mode*

| CCLK/Oscillator (MHz) |
|:---:|
| 2.5[1] |
| 3.1[2] |
| 4.3 |
| 5.4 |
| 6.9 |
| 8.1 |
| 9.2 |
| 10 |
| 13 |
| 15 |
| 20 |
| 26 |
| 32 |
| 40 |
| 54 |
| 80[3] |
| 163[3] |

1. Software default oscillator frequency.
2. Software default CCLK frequency.
3. Frequency not valid for CCLK.

## BLVDS

The LatticeXP2 devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

*Figure 3-2. BLVDS Multi-point Output Example*

Heavily loaded backplane, effective Zo ~ 45 to 90 ohms differential
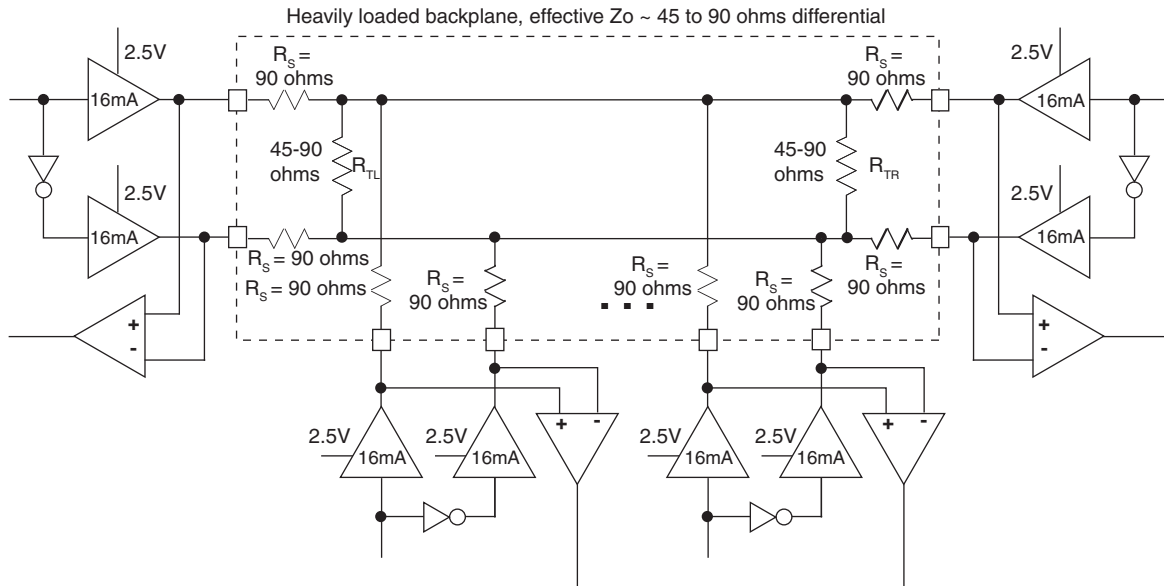
*Table 3-2. BLVDS DC Conditions[1]*

**Over Recommended Operating Conditions**

| Parameter | Description | Typical | | Units |
|---|---|---|---|---|
| | | Zo = 45$\Omega$ | Zo = 90$\Omega$ | |
| $V_{CCIO}$ | Output Driver Supply (+/- 5%) | 2.50 | 2.50 | V |
| $Z_{OUT}$ | Driver Impedance | 10.00 | 10.00 | $\Omega$ |
| $R_S$ | Driver Series Resistor (+/- 1%) | 90.00 | 90.00 | $\Omega$ |
| $R_{TL}$ | Driver Parallel Resistor (+/- 1%) | 45.00 | 90.00 | $\Omega$ |
| $R_{TR}$ | Receiver Termination (+/- 1%) | 45.00 | 90.00 | $\Omega$ |
| $V_{OH}$ | Output High Voltage (After $R_{TL}$) | 1.38 | 1.48 | V |
| $V_{OL}$ | Output Low Voltage (After $R_{TL}$) | 1.12 | 1.02 | V |
| $V_{OD}$ | Output Differential Voltage (After $R_{TL}$) | 0.25 | 0.46 | V |
| $V_{CM}$ | Output Common Mode Voltage | 1.25 | 1.25 | V |
| $I_{DC}$ | DC Output Current | 11.24 | 10.20 | mA |

1. For input buffer, see LVDS table.

## LatticeXP2 External Switching Characteristics (Continued)

### Over Recommended Operating Conditions

| Parameter | Description | Device | -7 Min. | -7 Max. | -6 Min. | -6 Max. | -5 Min. | -5 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{HE}$ | Clock to Data Hold - PIO Input Register | XP2-5 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-8 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-17 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-30 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| | | XP2-40 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| $t_{SU\_DELE}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | XP2-5 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-8 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-17 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-30 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| | | XP2-40 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| $t_{H\_DELE}$ | Clock to Data Hold - PIO Input Register with Input Data Delay | XP2-5 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-8 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-17 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-30 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-40 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| $f_{MAX\_IOE}$ | Clock Frequency of I/O and PFU Register | XP2 | — | 420 | — | 357 | — | 311 | MHz |
| **General I/O Pin Parameters (using Primary Clock with PLL)[1]** | | | | | | | | | |
| $t_{COPLL}$ | Clock to Output - PIO Output Register | XP2-5 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| | | XP2-8 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| | | XP2-17 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| | | XP2-30 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| | | XP2-40 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| $t_{SUPLL}$ | Clock to Data Setup - PIO Input Register | XP2-5 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-8 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-17 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-30 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-40 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | XP2-5 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | XP2-8 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | XP2-17 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | XP2-30 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-40 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| $t_{SU\_DELPLL}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | XP2-5 | 1.90 | — | 2.10 | — | 2.30 | — | ns |
| | | XP2-8 | 1.90 | — | 2.10 | — | 2.30 | — | ns |
| | | XP2-17 | 1.90 | — | 2.10 | — | 2.30 | — | ns |
| | | XP2-30 | 2.00 | — | 2.20 | — | 2.40 | — | ns |
| | | XP2-40 | 2.00 | — | 2.20 | — | 2.40 | — | ns |

## LatticeXP2 Internal Switching Characteristics[1] (Continued)

### Over Recommended Operating Conditions

| Parameter | Description | -7 Min. | -7 Max. | -6 Min. | -6 Max. | -5 Min. | -5 Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{RST\_PIO}$ | Asynchronous reset time for PFU Logic | — | 0.386 | — | 0.419 | — | 0.452 | ns |
| $t_{DEL}$ | Dynamic Delay Step Size | 0.035 | 0.035 | 0.035 | 0.035 | 0.035 | 0.035 | ns |
| **EBR Timing** | | | | | | | | |
| $t_{CO\_EBR}$ | Clock (Read) to Output from Address or Data | — | 2.774 | — | 3.142 | — | 3.510 | ns |
| $t_{COO\_EBR}$ | Clock (Write) to Output from EBR Output Register | — | 0.360 | — | 0.408 | — | 0.456 | ns |
| $t_{SUDATA\_EBR}$ | Setup Data to EBR Memory (Write Clk) | -0.167 | — | -0.198 | — | -0.229 | — | ns |
| $t_{HDATA\_EBR}$ | Hold Data to EBR Memory (Write Clk) | 0.194 | — | 0.231 | — | 0.267 | — | ns |
| $t_{SUADDR\_EBR}$ | Setup Address to EBR Memory (Write Clk) | -0.117 | — | -0.137 | — | -0.157 | — | ns |
| $t_{HADDR\_EBR}$ | Hold Address to EBR Memory (Write Clk) | 0.157 | — | 0.182 | — | 0.207 | — | ns |
| $t_{SUWREN\_EBR}$ | Setup Write/Read Enable to EBR Memory (Write/Read Clk) | -0.135 | — | -0.159 | — | -0.182 | — | ns |
| $t_{HWREN\_EBR}$ | Hold Write/Read Enable to EBR Memory (Write/Read Clk) | 0.158 | — | 0.186 | — | 0.214 | — | ns |
| $t_{SUCE\_EBR}$ | Clock Enable Setup Time to EBR Output Register (Read Clk) | 0.144 | — | 0.160 | — | 0.176 | — | ns |
| $t_{HCE\_EBR}$ | Clock Enable Hold Time to EBR Output Register (Read Clk) | -0.097 | — | -0.113 | — | -0.129 | — | ns |
| $t_{RSTO\_EBR}$ | Reset To Output Delay Time from EBR Output Register (Asynchronous) | — | 1.156 | — | 1.341 | — | 1.526 | ns |
| $t_{SUBE\_EBR}$ | Byte Enable Set-Up Time to EBR Output Register | -0.117 | — | -0.137 | — | -0.157 | — | ns |
| $t_{HBE\_EBR}$ | Byte Enable Hold Time to EBR Output Register Dynamic Delay on Each PIO | 0.157 | — | 0.182 | — | 0.207 | — | ns |
| $t_{RSTREC\_EBR}$ | Asynchronous reset recovery time for EBR | 0.233 | — | 0.291 | — | 0.347 | — | ns |
| $t_{RST\_EBR}$ | Asynchronous reset time for EBR | — | 1.156 | — | 1.341 | — | 1.526 | ns |
| **PLL Parameters** | | | | | | | | |
| $t_{RSTKREC\_PLL}$ | After RSTK De-assert, Recovery Time Before Next Clock Edge Can Toggle K-divider Counter | 1.000 | — | 1.000 | — | 1.000 | — | ns |
| $t_{RSTREC\_PLL}$ | After RST De-assert, Recovery Time Before Next Clock Edge Can Toggle M-divider Counter (Applies to M-Divider Portion of RST Only[2]) | 1.000 | — | 1.000 | — | 1.000 | — | ns |
| **DSP Block Timing** | | | | | | | | |
| $t_{SUI\_DSP}$ | Input Register Setup Time | 0.135 | — | 0.151 | — | 0.166 | — | ns |
| $t_{HI\_DSP}$ | Input Register Hold Time | 0.021 | — | -0.006 | — | -0.031 | — | ns |
| $t_{SUP\_DSP}$ | Pipeline Register Setup Time | 2.505 | — | 2.784 | — | 3.064 | — | ns |

## FlashBAK Time (from EBR to Flash)

### Over Recommended Operating Conditions

| Device | EBR Density (Bits) | Time (Typ.) | Units |
|--------|-------------------|-------------|-------|
| XP2-5  | 166K | 1.5 | s |
| XP2-8  | 221K | 1.5 | s |
| XP2-17 | 276K | 1.5 | s |
| XP2-30 | 387K | 2.0 | s |
| XP2-40 | 885K | 3.0 | s |

## JTAG Port Timing Specifications

### Over Recommended Operating Conditions

| Symbol | Parameter | Min. | Max. | Units |
|--------|-----------|------|------|-------|
| $f_{MAX}$ | TCK Clock Frequency | — | 25 | MHz |
| $t_{BTCP}$ | TCK [BSCAN] clock pulse width | 40 | — | ns |
| $t_{BTCPH}$ | TCK [BSCAN] clock pulse width high | 20 | — | ns |
| $t_{BTCPL}$ | TCK [BSCAN] clock pulse width low | 20 | — | ns |
| $t_{BTS}$ | TCK [BSCAN] setup time | 8 | — | ns |
| $t_{BTH}$ | TCK [BSCAN] hold time | 10 | — | ns |
| $t_{BTRF}$ | TCK [BSCAN] rise/fall time | 50 | — | mV/ns |
| $t_{BTCO}$ | TAP controller falling edge of clock to valid output | — | 10 | ns |
| $t_{BTCODIS}$ | TAP controller falling edge of clock to valid disable | — | 10 | ns |
| $t_{BTCOEN}$ | TAP controller falling edge of clock to valid enable | — | 10 | ns |
| $t_{BTCRS}$ | BSCAN test capture register setup time | 8 | — | ns |
| $t_{BTCRH}$ | BSCAN test capture register hold time | 25 | — | ns |
| $t_{BUTCO}$ | BSCAN test update register, falling edge of clock to valid output | — | 25 | ns |
| $t_{BTUODIS}$ | BSCAN test update register, falling edge of clock to valid disable | — | 25 | ns |
| $t_{BTUPOEN}$ | BSCAN test update register, falling edge of clock to valid enable | — | 25 | ns |

## Signal Descriptions (Cont.)

| Signal Name | I/O | Description |
|---|---|---|
| TDO | O | Output pin. Test Data Out pin used to shift data out of a device using 1149.1. |
| VCCJ | — | Power supply pin for JTAG Test Access Port. |
| **Configuration Pads** (Used during sysCONFIG) | | |
| CFG[1:0] | I | Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, an internal pull-up is enabled. |
| INITN[1] | I/O | Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. |
| PROGRAMN | I | Initiates configuration sequence when asserted low. This pin always has an active pull-up. |
| DONE | I/O | Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. |
| CCLK | I/O | Configuration Clock for configuring an FPGA in sysCONFIG mode. |
| SISPI[2] | I/O | Input data pin in slave SPI mode and Output data pin in Master SPI mode. |
| SOSPI[2] | I/O | Output data pin in slave SPI mode and Input data pin in Master SPI mode. |
| CSSPIN[2] | O | Chip select for external SPI Flash memory in Master SPI mode. This pin has a weak internal pull-up. |
| CSSPISN | I | Chip select in Slave SPI mode. This pin has a weak internal pull-up. |
| TOE | I | Test Output Enable tristates all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to $V_{CC}$ is recommended. |

1. If not actively driven, the internal pull-up may not be sufficient. An external pull-up resistor of 4.7k to 10kΩ is recommended.
2. When using the device in Master SPI mode, it must be mutually exclusive from JTAG operations (i.e. TCK tied to GND) or the JTAG TCK must be free-running when used in a system JTAG test environment. If Master SPI mode is used in conjunction with a JTAG download cable, the device power cycle is required after the cable is unplugged.

## Pin Information Summary (Cont.)

| | | XP2-5 | | | | XP2-8 | | | | XP2-17 | | | XP2-30 | | | XP2-40 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin Type | | 132 csBGA | 144 TQFP | 208 PQFP | 256 ftBGA | 132 csBGA | 144 TQFP | 208 PQFP | 256 ftBGA | 208 PQFP | 256 ftBGA | 484 fpBGA | 256 ftBGA | 484 fpBGA | 672 fpBGA | 484 fpBGA | 672 fpBGA |
| PCI capable I/Os Bonding Out per Bank | Bank0 | 18 | 20 | 20 | 26 | 18 | 20 | 20 | 28 | 20 | 28 | 52 | 28 | 52 | 70 | 52 | 70 |
| | Bank1 | 4 | 6 | 18 | 18 | 4 | 6 | 18 | 22 | 18 | 22 | 36 | 22 | 36 | 54 | 36 | 70 |
| | Bank2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank4 | 8 | 8 | 18 | 18 | 8 | 8 | 18 | 26 | 18 | 26 | 36 | 26 | 38 | 54 | 38 | 70 |
| | Bank5 | 14 | 18 | 20 | 24 | 14 | 18 | 20 | 24 | 20 | 24 | 52 | 24 | 53 | 70 | 53 | 70 |
| | Bank6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

# Logic Signal Connections

Package pinout information can be found under "Data Sheets" on the LatticeXP2 product page of the Lattice website a www.latticesemi.com/products/fpga/xp2 and in the Lattice Diamond design software.
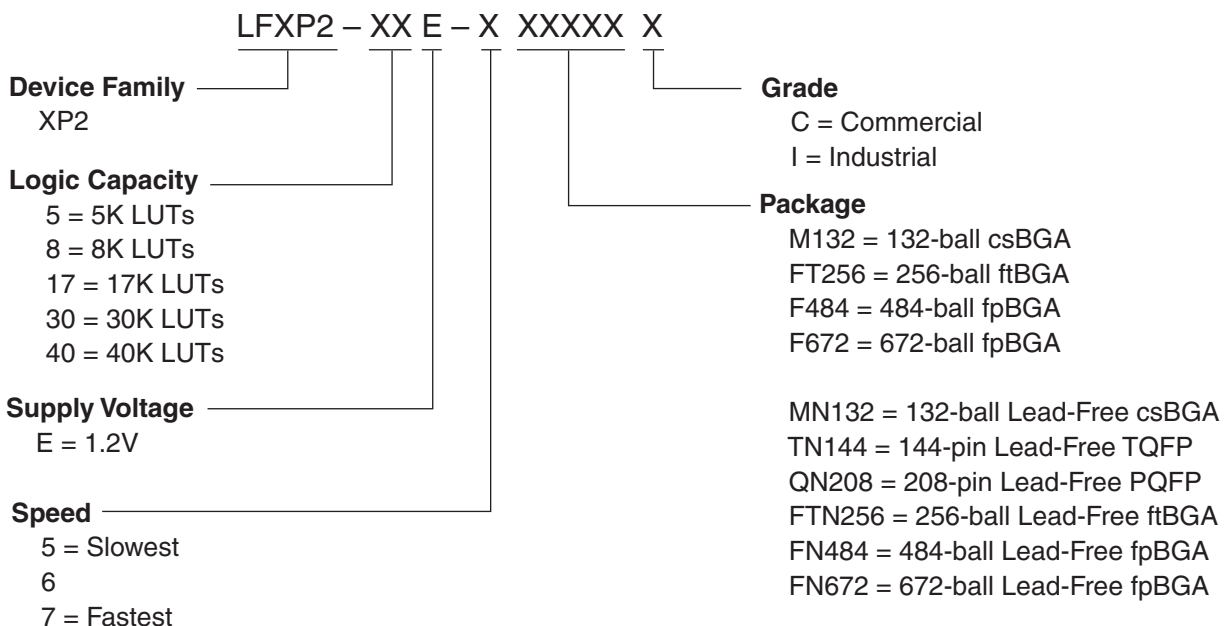
# Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Lattice Thermal Management document to find the device/package specific thermal values.
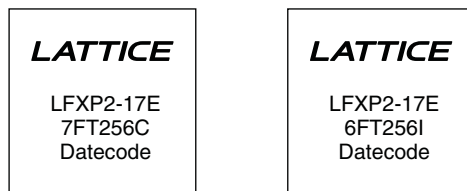
# For Further Information

• TN1139, Power Estimation and Management for LatticeXP2 Devices

• Power Calculator tool is included with the Lattice Diamond design tool or as a standalone download from www.latticesemi.com/products/designsoftware

## Part Number Description

LFXP2 – XX E – X XXXXX X

**Device Family**
XP2

**Logic Capacity**
5 = 5K LUTs
8 = 8K LUTs
17 = 17K LUTs
30 = 30K LUTs
40 = 40K LUTs

**Supply Voltage**
E = 1.2V

**Speed**
5 = Slowest
6
7 = Fastest

**Grade**
C = Commercial
I = Industrial

**Package**
M132 = 132-ball csBGA
FT256 = 256-ball ftBGA
F484 = 484-ball fpBGA
F672 = 672-ball fpBGA

MN132 = 132-ball Lead-Free csBGA
TN144 = 144-pin Lead-Free TQFP
QN208 = 208-pin Lead-Free PQFP
FTN256 = 256-ball Lead-Free ftBGA
FN484 = 484-ball Lead-Free fpBGA
FN672 = 672-ball Lead-Free fpBGA

## Ordering Information

The LatticeXP2 devices are marked with a single temperature grade, either Commercial or Industrial, as shown below.

LATTICE
LFXP2-17E
7FT256C
Datecode

LATTICE
LFXP2-17E
6FT256I
Datecode

## For Further Information

A variety of technical notes for the LatticeXP2 FPGA family are available on the Lattice Semiconductor web site at www.latticesemi.com.

- TN1136, LatticeXP2 sysIO Usage Guide
- TN1137, LatticeXP2 Memory Usage Guide
- TN1138, LatticeXP2 High Speed I/O Interface
- TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide
- TN1139, Power Estimation and Management for LatticeXP2 Devices
- TN1140, LatticeXP2 sysDSP Usage Guide
- TN1141, LatticeXP2 sysCONFIG Usage Guide
- TN1142, LatticeXP2 Configuration Encryption and Security Usage Guide
- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology
- TN1220, LatticeXP2 Dual Boot Feature
- TN1130, LatticeXP2 Soft Error Detection (SED) Usage Guide
- TN1143, LatticeXP2 Hardware Checklist

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com