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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	5000
Number of Logic Elements/Cells	40000
Total RAM Bits	906240
Number of I/O	363
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-40e-6f484i

Email: info@E-XFL.COM

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Introduction

LatticeXP2 devices combine a Look-up Table (LUT) based FPGA fabric with non-volatile Flash cells in an architecture referred to as flexiFLASH.

The flexiFLASH approach provides benefits including instant-on, infinite reconfigurability, on chip storage with FlashBAK embedded block memory and Serial TAG memory and design security. The parts also support Live Update technology with TransFR, 128-bit AES Encryption and Dual-boot technologies.

The LatticeXP2 FPGA fabric was optimized for the new technology from the outset with high performance and low cost in mind. LatticeXP2 devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support and enhanced sysDSP blocks.

Lattice Diamond[®] design software allows large and complex designs to be efficiently implemented using the LatticeXP2 family of FPGA devices. Synthesis library support for LatticeXP2 is available for popular logic synthesis tools. The Diamond software uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeXP2 device. The Diamond tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed Intellectual Property (IP) LatticeCORE[™] modules for the LatticeXP2 family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.







PFU Blocks

The core of the LatticeXP2 device is made up of logic blocks in two forms, PFUs and PFFs. PFUs can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. PFF blocks can be programmed to perform logic, arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered Slice 0 through Slice 3, as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.



Figure 2-4. General Purpose PLL (GPLL) Diagram



Table 2-4 provides a description of the signals in the GPLL blocks.

Signal	I/O	Description	
CLKI	I	Clock input from external pin or routing	
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)	
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers	
RSTK	I	"1" to reset K-divider	
DPHASE [3:0]	I	DPA Phase Adjust input	
DDDUTY [3:0]	I	DPA Duty Cycle Select input	
WRDEL	I	DPA Fine Delay Adjust input	
CLKOS	0	PLL output clock to clock tree (phase shifted/duty cycle changed)	
CLKOP	0	PLL output clock to clock tree (no phase shift)	
CLKOK	0	PLL output to clock tree through secondary clock divider	
CLKOK2	0	PLL output to clock tree (CLKOP divided by 3)	
LOCK	0	"1" indicates PLL LOCK to CLKI	

Clock Dividers

LatticeXP2 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from the CLKOP output from the GPLLs or from the Edge Clocks (ECLK). The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets the input and forces all outputs to low. The RELEASE signal releases outputs to the input clock. For further information on clock dividers, please see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide. Figure 2-5 shows the clock divider connections.



sysMEM Memory

LatticeXP2 devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of 18 Kbit RAM with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-5. FIFOs can be implemented in sysMEM EBR blocks by using support logic with PFUs. The EBR block supports an optional parity bit for each data byte to facilitate parity checking. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths.

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

FlashBAK EBR Content Storage

All the EBR memory in the LatticeXP2 is shadowed by Flash memory. Optionally, initialization values for the memory blocks can be defined using the Lattice Diamond design tools. The initialization values are loaded into the Flash memory during device programming and into the SRAM at power up or whenever the device is reconfigured. This feature is ideal for the storage of a variety of information such as look-up tables and microprocessor code. It is also possible to write the current contents of the EBR memory back to Flash memory. This capability is useful for the storage of data such as error codes and calibration information. For additional information on the FlashBAK capability see TN1137, LatticeXP2 Memory Usage Guide.



MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/ subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-23 shows the MULTADDSUBSUM sysDSP element.

Figure 2-23. MULTADDSUBSUM



Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable (CE) and Reset (RST) signals from routing are available to every DSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output



Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-27 shows the Tristate Register Block with the Output Block

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as Dtype or latch. In DDR mode, ONEG1 and OPOS1 are fed into registers on the positive edge of the clock. Then in the next clock the registered OPOS1 is latched. A multiplexer running off the same clock cycle selects the correct register for feeding to the output (D0).

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock signal is selected from general purpose routing, ECLK1, ECLK2 or a DQS signal (from the programmable DQS pin) and is provided to the input register block. The clock can optionally be inverted.

DDR Memory Support

PICs have additional circuitry to allow implementation of high speed source synchronous and DDR memory interfaces.

PICs have registered elements that support DDR memory interfaces. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the top and bottom are designed for memories that support 18 bits of data. One of every 16 PIOs on the left and right and one of every 18 PIOs on the top and bottom contain delay elements to facilitate the generation of DQS signals. The DQS signals feed the DQS buses which span the set of 16 or 18 PIOs. Figure 2-28 and Figure 2-29 show the DQS pin assignments in each set of PIOs.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. For additional information on using DDR memory support please see TN1138, <u>LatticeXP2 High Speed I/O Interface</u>.



Figure 2-28. DQS Input Routing (Left and Right)

	PIO A		PADA "T"
	PIO B		PADB "C"
	PIO A		PADA "T"
	PIO B	· · · · ·	PADB "C"
	PIO A		PADA "T"
	PIO B	↓+	PADB "C"
	PIO A		PADA "T"
	PIO B	┃┣	PADB "C"
DOG	PIO A	sysIO Buffer	
 ■ DQ5 		Delay	LVDS Pair
+ DQS	PIO B	Delay	LVDS Pair
↓ DQS	PIO B PIO A		PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair
	→ PIO B → PIO A → PIO B		PADA "1" LVDS Pair PADB "C" PADA "T" LVDS Pair LVDS Pair PADA "C"
	→ PIO B → PIO A → PIO B → PIO A		PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair
			PADA T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair LVDS Pair PADB "C"
			PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C"

Figure 2-29. DQS Input Routing (Top and Bottom)

	PIO A		PADA "T"
	PIO B	+	PADB "C"
	PIO A		PADA "T"
	PIO B	· · · · ·	PADB "C"
—	PIO A		PADA "T" LVDS Pair
	PIO B	→	PADB "C"
	PIO A		PADA "T"
<u> </u>	PIO B	→	PADB "C"
	PIO A	syslO Buffer	·
DQS		Palay	
•		Delay	LVDS Pair
	PIO B		LVDS Pair I I PADB "C" I
	PIO B PIO A		LVDS Pair I PADB "C"
	→ PIO B → PIO A → PIO B		LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C"
	→ PIO B → PIO A → PIO B → PIO A		LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair
	→ PIO B → PIO A → PIO B → PIO A → PIO B		LVDS Pair PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADA "C" PADA "C"
	→ PIO B → PIO A → PIO A → PIO A → PIO A → PIO B → PIO A		LVDS Pair PADA "T" LVDS Pair PADA "T" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADA "T" LVDS Pair
			LVDS Pair PADA "T" LVDS Pair PADA "T" PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair LVDS Pair PADB "C"
			LVDS Pair PADA "T" LVDS Pair PADB "C" PADB "C" PADB "C" PADB "C" PADB "C" PADB "C" PADB "C" PADA "T" LVDS Pair PADB "C" PADA "T" LVDS Pair PADA "T" LVDS Pair



DQSXFER

LatticeXP2 devices provide a DQSXFER signal to the output buffer to assist it in data transfer to DDR memories that require DQS strobe be shifted 90°. This shifted DQS strobe is generated by the DQSDEL block. The DQSXFER signal runs the span of the data bus.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

sysIO Buffer Banks

LatticeXP2 devices have eight sysIO buffer banks for user I/Os arranged two per side. Each bank is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank has voltage references, V_{REF1} and V_{REF2} , that allow it to be completely independent from the others. Figure 2-32 shows the eight banks and their associated supplies.

In LatticeXP2 devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO} . LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO} .

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2} , that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

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Figure 2-32. LatticeXP2 Banks



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Table 2-13. Supported Output Standards

Output Standard	Drive	V _{CCIO} (Nom.)			
Single-ended Interfaces					
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3			
LVCMOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3			
LVCMOS25	4mA, 8mA, 12mA, 16mA, 20mA	2.5			
LVCMOS18	4mA, 8mA, 12mA, 16mA	1.8			
LVCMOS15	4mA, 8mA	1.5			
LVCMOS12	2mA, 6mA	1.2			
LVCMOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—			
LVCMOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA				
LVCMOS18, Open Drain	4mA, 8mA, 12mA 16mA				
LVCMOS15, Open Drain	4mA, 8mA	_			
LVCMOS12, Open Drain	2mA, 6mA	_			
PCI33	N/A	3.3			
HSTL18 Class I, II	N/A	1.8			
HSTL15 Class I	N/A	1.5			
SSTL33 Class I, II	N/A	3.3			
SSTL25 Class I, II	N/A	2.5			
SSTL18 Class I, II	N/A	1.8			
Differential Interfaces					
Differential SSTL33, Class I, II	N/A	3.3			
Differential SSTL25, Class I, II	N/A	2.5			
Differential SSTL18, Class I, II	N/A	1.8			
Differential HSTL18, Class I, II	N/A	1.8			
Differential HSTL15, Class I	N/A	1.5			
LVDS ^{1, 2}	N/A	2.5			
MLVDS ¹	N/A	2.5			
BLVDS ¹	N/A	2.5			
LVPECL ¹	N/A	3.3			
RSDS ¹	N/A	2.5			
LVCMOS33D ¹	4mA, 8mA, 12mA, 16mA, 20mA	3.3			

1. Emulated with external resistors.

2. On the left and right edges, LVDS outputs are supported with a dedicated differential output driver on 50% of the I/Os. This solution does not require external resistors at the driver.

Hot Socketing

LatticeXP2 devices have been carefully designed to ensure predictable behavior during power-up and powerdown. Power supplies can be sequenced in any order. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the LatticeXP2 ideal for many multiple power supply and hot-swap applications.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeXP2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in



Hot Socketing Specifications^{1, 2, 3, 4}

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
I _{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX.)	_	_	+/-1	mA

1. Insensitive to sequence of V_{CC} , V_{CCAUX} and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} , V_{CCAUX} and V_{CCIO} .

2. $0 \le V_{CC} \le V_{CC}$ (MAX), $0 \le V_{CCIO} \le V_{CCIO}$ (MAX) or $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX).

3. I_{DK} is additive to I_{PU} , I_{PW} or I_{BH} .

4. LVCMOS and LVTTL only.

ESD Performance

Please refer to the <u>LatticeXP2 Product Family Qualification Summary</u> for complete qualification data, including ESD performance.

DC Electrical Characteristics

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
I _{IL} , I _{IH} 1	Input or I/O Low Leakage	$0 \le V_{IN} \le V_{CCIO}$	—		10	μΑ
		$V_{CCIO} \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	μΑ
I _{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7 \ V_{CCIO}$	-30	—	-150	μΑ
I _{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\leq V_{IN} \leq V_{CCIO}$	30		210	μΑ
I _{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	μΑ
I _{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCIO}$	-30	—	—	μΑ
I _{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—		210	μΑ
I _{BHHO}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	-150	μΑ
V _{BHT}	Bus Hold Trip Points		V_{IL} (MAX)	_	V _{IH} (MIN)	V
C1	I/O Capacitance ²	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} \text{ (MAX)}$	—	8	—	pf
C2	Dedicated Input Capacitance	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} \text{ (MAX)}$	—	6	—	pf

Over Recommended Operating Conditions

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. T_A 25°C, f = 1.0 MHz.



Initialization Supply Current^{1, 2, 3, 4, 5}

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical (25°C, Max. Supply) ⁶	Units
		XP2-5	20	mA
		XP2-8	21	mA
I _{CC}	Core Power Supply Current	XP2-17	44	mA
		XP2-30	58	mA
		XP2-40	62	mA
I _{CCAUX}		XP2-5	67	mA
	Auxiliary Power Supply Current ⁷	XP2-8	74	mA
		XP2-17	112	mA
		XP2-30	124	mA
		XP2-40	130	mA
I _{CCPLL}	PLL Power Supply Current (per PLL)		1.8	mA
I _{CCIO}	Bank Power Supply Current (per Bank)		6.4	mA
ICCJ	VCCJ Power Supply Current		1.2	mA

1. For further information on supply current, please see TN1139, Power Estimation and Management for LatticeXP2 Devices.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

3. Frequency 0 MHz.

4. Does not include additional current from bypass or decoupling capacitor across the supply.

5. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.

6. $T_J = 25^{\circ}C$, power supplies at nominal voltage.

In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual
auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the
auxiliary power supply.



BLVDS

The LatticeXP2 devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.





Table 3-2. BLVDS DC Conditions¹

		Typical		
Parameter	Description	Ζο = 45 Ω	Ζο = 90 Ω	Units
V _{CCIO}	Output Driver Supply (+/- 5%)	2.50	2.50	V
Z _{OUT}	Driver Impedance	10.00	10.00	Ω
R _S	Driver Series Resistor (+/- 1%)	90.00	90.00	Ω
R _{TL}	Driver Parallel Resistor (+/- 1%)	45.00	90.00	Ω
R _{TR}	Receiver Termination (+/- 1%)	45.00	90.00	Ω
V _{OH}	Output High Voltage (After R _{TL})	1.38	1.48	V
V _{OL}	Output Low Voltage (After R _{TL})	1.12	1.02	V
V _{OD}	Output Differential Voltage (After R _{TL})	0.25	0.46	V
V _{CM}	Output Common Mode Voltage	1.25	1.25	V
I _{DC}	DC Output Current	11.24	10.20	mA

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.



LatticeXP2 Family Timing Adders^{1, 2, 3, 4} (Continued)

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	0.32	0.69	1.06	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	0.32	0.69	1.06	ns
SSTL33_I	SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33_II	SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33D_II	Differential SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL18_I	SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
LVTTL33_4mA	LVTTL 4mA drive	-0.37	-0.05	0.26	ns
LVTTL33_8mA	LVTTL 8mA drive	-0.45	-0.18	0.10	ns
LVTTL33_12mA	LVTTL 12mA drive	-0.52	-0.24	0.04	ns
LVTTL33_16mA	LVTTL 16mA drive	-0.43	-0.14	0.14	ns
LVTTL33_20mA	LVTTL 20mA drive	-0.46	-0.18	0.09	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	-0.37	-0.05	0.26	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	-0.45	-0.18	0.10	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	-0.52	-0.24	0.04	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	-0.43	-0.14	0.14	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	-0.46	-0.18	0.09	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	-0.42	-0.15	0.13	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	-0.48	-0.21	0.05	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	-0.45	-0.18	0.08	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	-0.49	-0.22	0.04	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	-0.46	-0.18	0.10	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	-0.52	-0.25	0.02	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.56	-0.30	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	-0.50	-0.24	0.03	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate	-0.45	-0.17	0.11	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate	-0.53	-0.26	0.00	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate	-0.46	-0.19	0.08	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate	-0.55	-0.29	-0.02	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate	0.98	1.41	1.84	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate	0.74	1.16	1.58	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate	0.56	0.97	1.38	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate	0.77	1.19	1.61	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate	0.57	0.98	1.40	ns

Over Recommended Operating Conditions



sysCLOCK PLL Timing

Parameter	Description	Conditions	Min.	Тур.	Max.	Units
f _{IN}	Input Clock Frequency (CLKI, CLKFB)		10		435	MHz
fout	Output Clock Frequency (CLKOP, CLKOS)		10	—	435	MHz
f	K-Divider Output Frequency	CLKOK	0.078	_	217.5	MHz
'OUT2		CLKOK2	3.3		145	MHz
f _{VCO}	PLL VCO Frequency		435	_	870	MHz
f _{PFD}	Phase Detector Input Frequency		10	_	435	MHz
AC Characte	eristics					
t _{DT}	Output Clock Duty Cycle	Default duty cycle selected ³	45	50	55	%
t _{CPA}	Coarse Phase Adjust		-5	0	5	%
t _{PH} ⁴	Output Phase Accuracy		-5	0	5	%
		f _{OUT} > 400 MHz	—		±50	ps
t _{OPJIT} 1	Output Clock Period Jitter	100 MHz < f _{OUT} < 400 MHz	—	_	±125	ps
		f _{OUT} < 100 MHz	—	_	0.025	UIPP
t _{SK}	Input Clock to Output Clock Skew	N/M = integer	—		±240	ps
t _{OPW}	Output Clock Pulse Width	At 90% or 10%	1	_	—	ns
+ 2	PLL Look in Time	25 to 435 MHz	_		50	μs
LOCK		10 to 25 MHz	—	_	100	μs
t _{IPJIT}	Input Clock Period Jitter		_		±200	ps
t _{FBKDLY}	External Feedback Delay		_		10	ns
t _{HI}	Input Clock High Time	90% to 90%	0.5		_	ns
t _{LO}	Input Clock Low Time	10% to 10%	0.5		_	ns
t _{RSTKW}	Reset Signal Pulse Width (RSTK)		10	—	—	ns
t _{RSTW}	Reset Signal Pulse Width (RST)		500		—	ns

Over Recommended Operating Conditions

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. Relative to CLKOP.



On-Chip Oscillator and Configuration Master Clock Characteristics

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value -30%	Selected value +30%	MHz
Duty Cycle	40	60	%

Over Recommended Operating Conditions

Figure 3-9. Master SPI Configuration Waveforms





Flash Download Time (from On-Chip Flash to SRAM)

Over Recommended Operating Conditions

Symbol	Parar	neter	Min.	Тур.	Max.	Units
		XP2-5	—	1.8	2.1	ms
	PROGRAMN Low-to-	XP2-8	—	1.9	2.3	ms
	High. Transition to Done	XP2-17	—	1.7	2.0	ms
High.	High.	XP2-30	—	2.0	2.1	ms
t		XP2-40	—	2.0	2.3	ms
'REFRESH		XP2-5	—	1.8	2.1	ms
	Power-up refresh when	XP2-8	—	1.9	2.3	ms
	Up to Voc	XP2-17	—	1.7	2.0	ms
	$(V_{CC}=V_{CC} Min)$	XP2-30	—	2.0	2.1	ms
		XP2-40		2.0	2.3	ms

Flash Program Time

Over Recommended Operating Conditions

			Program Time	
Device	Flash Density		Тур.	Units
	1.0M	TAG	1.0	ms
XF2-5	1.2101	Main Array	1.1	S
	2.0M	TAG	1.0	ms
AF2-0	2.0101	Main Array	1.4	S
VP0 17	2.6M	TAG	1.0	ms
AF2-17	3.0101	Main Array	1.8	S
	6.014	TAG	2.0	ms
XF2-30	0.0101	Main Array	3.0	S
VP2 40	8 OM	TAG	2.0	ms
XP2-40	0.0101	Main Array	4.0	S

Flash Erase Time

Over Recommended Operating Conditions

	Flash Density		Erase Time	
Device			Тур.	Units
YP2_5	1.2M	TAG	1.0	s
XI 2-3	1.2101	Main Array	3.0	s
YP2_8	2.0M	TAG	1.0	S
AF2-0	2.0101	Main Array	4.0	s
VD2 17	2.6M	TAG	1.0	s
XI 2-17	3.0101	Main Array	5.0	S
XD2-30	6 OM	TAG	2.0	s
XI 2-30	0.0101	Main Array	7.0	S
XP2-40	8.0M	TAG	2.0	S
XP2-40	0.00	Main Array	9.0	S



Switching Test Conditions

Figure 3-11 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

Figure 3-11. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

 Table 3-6. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R ₁	R ₂	CL	Timing Ref.	V _T
				LVCMOS 3.3 = 1.5V	
LVTTL and other LVCMOS settings (L -> H, H -> L)				LVCMOS 2.5 = $V_{CCIO}/2$	
	∞	∞	0pF	LVCMOS 1.8 = V _{CCIO} /2	
				LVCMOS 1.5 = $V_{CCIO}/2$	_
				LVCMOS 1.2 = V _{CCIO} /2	_
LVCMOS 2.5 I/O (Z -> H)	x	1MΩ		V _{CCIO} /2	
LVCMOS 2.5 I/O (Z -> L)	1MΩ	∞		V _{CCIO} /2	V _{CCIO}
LVCMOS 2.5 I/O (H -> Z)	x	100		V _{OH} - 0.10	
LVCMOS 2.5 I/O (L -> Z)	100	∞		V _{OL} + 0.10	V _{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.



Signal Descriptions (Cont.)

Signal Name	I/O	Description
TDO	0	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ		Power supply pin for JTAG Test Access Port.
Configuration Pads (Used during sysC	ONFIG)	
CFG[1:0]	Ι	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, an internal pull-up is enabled.
INITN ¹	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
SISPI ²	I/O	Input data pin in slave SPI mode and Output data pin in Master SPI mode.
SOSPI ²	I/O	Output data pin in slave SPI mode and Input data pin in Master SPI mode.
CSSPIN ²	0	Chip select for external SPI Flash memory in Master SPI mode. This pin has a weak internal pull-up.
CSSPISN	I	Chip select in Slave SPI mode. This pin has a weak internal pull-up.
TOE	I	Test Output Enable tristates all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to $\rm V_{\rm CC}$ is recommended.

1. If not actively driven, the internal pull-up may not be sufficient. An external pull-up resistor of 4.7k to $10k\Omega$ is recommended.

2. When using the device in Master SPI mode, it must be mutually exclusive from JTAG operations (i.e. TCK tied to GND) or the JTAG TCK must be free-running when used in a system JTAG test environment. If Master SPI mode is used in conjunction with a JTAG download cable, the device power cycle is required after the cable is unplugged.



Lead-Free Packaging

Commercial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5MN132C	1.2V	-5	Lead-Free csBGA	132	COM	5
LFXP2-5E-6MN132C	1.2V	-6	Lead-Free csBGA	132	COM	5
LFXP2-5E-7MN132C	1.2V	-7	Lead-Free csBGA	132	COM	5
LFXP2-5E-5TN144C	1.2V	-5	Lead-Free TQFP	144	COM	5
LFXP2-5E-6TN144C	1.2V	-6	Lead-Free TQFP	144	COM	5
LFXP2-5E-7TN144C	1.2V	-7	Lead-Free TQFP	144	COM	5
LFXP2-5E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	5
LFXP2-5E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	5
LFXP2-5E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	5
LFXP2-5E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	5
LFXP2-5E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	5
LFXP2-5E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5MN132C	1.2V	-5	Lead-Free csBGA	132	COM	8
LFXP2-8E-6MN132C	1.2V	-6	Lead-Free csBGA	132	COM	8
LFXP2-8E-7MN132C	1.2V	-7	Lead-Free csBGA	132	COM	8
LFXP2-8E-5TN144C	1.2V	-5	Lead-Free TQFP	144	COM	8
LFXP2-8E-6TN144C	1.2V	-6	Lead-Free TQFP	144	COM	8
LFXP2-8E-7TN144C	1.2V	-7	Lead-Free TQFP	144	COM	8
LFXP2-8E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	8
LFXP2-8E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	8
LFXP2-8E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	8
LFXP2-8E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	8
LFXP2-8E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	8
LFXP2-8E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	17
LFXP2-17E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	17
LFXP2-17E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	17
LFXP2-17E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	17
LFXP2-17E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	17
LFXP2-17E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	17
LFXP2-17E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	17
LFXP2-17E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	17
LFXP2-17E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	17



Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5F484C	1.2V	-5	fpBGA	484	COM	40
LFXP2-40E-6F484C	1.2V	-6	fpBGA	484	COM	40
LFXP2-40E-7F484C	1.2V	-7	fpBGA	484	COM	40
LFXP2-40E-5F672C	1.2V	-5	fpBGA	672	COM	40
LFXP2-40E-6F672C	1.2V	-6	fpBGA	672	COM	40
LFXP2-40E-7F672C	1.2V	-7	fpBGA	672	COM	40

Industrial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5M132I	1.2V	-5	csBGA	132	IND	5
LFXP2-5E-6M132I	1.2V	-6	csBGA	132	IND	5
LFXP2-5E-6FT256I	1.2V	-6	ftBGA	256	IND	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5M132I	1.2V	-5	csBGA	132	IND	8
LFXP2-8E-6M132I	1.2V	-6	csBGA	132	IND	8
LFXP2-5E-5FT256I	1.2V	-5	ftBGA	256	IND	5
LFXP2-8E-5FT256I	1.2V	-5	ftBGA	256	IND	8
LFXP2-8E-6FT256I	1.2V	-6	ftBGA	256	IND	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5FT256I	1.2V	-5	ftBGA	256	IND	17
LFXP2-17E-6FT256I	1.2V	-6	ftBGA	256	IND	17
LFXP2-17E-5F484I	1.2V	-5	fpBGA	484	IND	17
LFXP2-17E-6F484I	1.2V	-6	fpBGA	484	IND	17

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-30E-5FT256I	1.2V	-5	ftBGA	256	IND	30
LFXP2-30E-6FT256I	1.2V	-6	ftBGA	256	IND	30
LFXP2-30E-5F484I	1.2V	-5	fpBGA	484	IND	30
LFXP2-30E-6F484I	1.2V	-6	fpBGA	484	IND	30
LFXP2-30E-5F672I	1.2V	-5	fpBGA	672	IND	30
LFXP2-30E-6F672I	1.2V	-6	fpBGA	672	IND	30