E.J. Lattice Semiconductor Corporation - <u>LFXP2-40E-6FN484C Datasheet</u>



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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	5000
Number of Logic Elements/Cells	40000
Total RAM Bits	906240
Number of I/O	363
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-40e-6fn484c

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PFU Blocks

The core of the LatticeXP2 device is made up of logic blocks in two forms, PFUs and PFFs. PFUs can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. PFF blocks can be programmed to perform logic, arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered Slice 0 through Slice 3, as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.



Figure 2-3. Slice Diagram



DI[3:2] for Slice 2 and DI[1:0] for Slice 0 data

WAD [A:D] is a 4bit address from slice 1 LUT input

Table 2-2. Slice Signal Descriptions

Function	Туре	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	MO	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-In ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.



LatticeXP2-30 and smaller devices have six secondary clock regions. All devices in the LatticeXP2 family have four secondary clocks (SC0 to SC3) which are distributed to every region.

The secondary clock muxes are located in the center of the device. Figure 2-12 shows the mux structure of the secondary clock routing. Secondary clocks SC0 to SC3 are used for clock and control and SC4 to SC7 are used for high fan-out signals.







Figure 2-14. Slice0 through Slice2 Control Selection



Edge Clock Routing

LatticeXP2 devices have eight high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. Each device has two edge clocks per edge. Figure 2-15 shows the selection muxes for these clocks.

Figure 2-15. Edge Clock Mux Connections





and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards. For more information, please see TN1141, LatticeXP2 sysCONFIG Usage Guide.

flexiFLASH Device Configuration

The LatticeXP2 devices combine Flash and SRAM on a single chip to provide users with flexibility in device programming and configuration. Figure 2-33 provides an overview of the arrangement of Flash and SRAM configuration cells within the device. The remainder of this section provides an overview of these capabilities. See TN1141, LatticeXP2 sysCONFIG Usage Guide for a more detailed description.



Figure 2-33. Overview of Flash and SRAM Configuration Cells Within LatticeXP2 Devices

At power-up, or on user command, data is transferred from the on-chip Flash memory to the SRAM configuration cells that control the operation of the device. This is done with massively parallel buses enabling the parts to operate within microseconds of the power supplies reaching valid levels; this capability is referred to as Instant-On.

The on-chip Flash enables a single-chip solution eliminating the need for external boot memory. This Flash can be programmed through either the JTAG or Slave SPI ports of the device. The SRAM configuration space can also be infinitely reconfigured through the JTAG and Master SPI ports. The JTAG port is IEEE 1149.1 and IEEE 1532 compliant.

As described in the EBR section of the data sheet, the FlashBAK capability of the parts enables the contents of the EBR blocks to be written back into the Flash storage area without erasing or reprogramming other aspects of the device configuration. Serial TAG memory is also available to allow the storage of small amounts of data such as calibration coefficients and error codes.

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM only FPGAs. This is further enhanced by device locking. The device can be in one of three modes:



Programming and Erase Flash Supply Current^{1, 2, 3, 4, 5}

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical (25°C, Max. Supply) ⁶	Units
		XP2-5	17	mA
I _{CC}		XP2-8	21	mA
	Core Power Supply Current	XP2-17	28	mA
		XP2-30	36	mA
		XP2-40	50	mA
I _{CCAUX}		XP2-5	64	mA
	Auxiliary Power Supply Current ⁷	XP2-8	66	mA
		XP2-17	83	mA
		XP2-30	87	mA
		XP2-40	88	mA
I _{CCPLL}	PLL Power Supply Current (per PLL)		0.1	mA
I _{CCIO}	Bank Power Supply Current (per Bank)		5	mA
I _{CCJ}	V _{CCJ} Power Supply Current ⁸		14	mA

1. For further information on supply current, please see TN1139, Power Estimation and Management for LatticeXP2 Devices.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

3. Frequency 0 MHz (excludes dynamic power from FPGA operation).

4. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.

5. Bypass or decoupling capacitor across the supply.

6. $T_J = 25^{\circ}C$, power supplies at nominal voltage.

 In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.

8. When programming via JTAG.



sysIO Differential Electrical Characteristics LVDS

Parameter	Description	Test Conditions	Min.	Тур.	Max.	Units
V _{INP} , V _{INM}	Input Voltage		0		2.4	V
V _{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
V _{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100		—	mV
I _{IN}	Input Current	Power On or Power Off		—	+/-10	μΑ
V _{OH}	Output High Voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	_	1.38	1.60	V
V _{OL}	Output Low Voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	0.9V	1.03	—	V
V _{OD}	Output Voltage Differential	(V _{OP} - V _{OM}), R _T = 100 Ohm	250	350	450	mV
ΔV _{OD}	Change in V _{OD} Between High and Low		_	_	50	mV
V _{OS}	Output Voltage Offset	(V _{OP} + V _{OM})/2, R _T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V _{OS} Between H and L				50	mV
I _{SA}	Output Short Circuit Current	V _{OD} = 0V Driver Outputs Shorted to Ground	_	_	24	mA
I _{SAB}	Output Short Circuit Current	V _{OD} = 0V Driver Outputs Shorted to Each Other	_	_	12	mA

Over Recommended Operating Conditions

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see details in additional technical notes listed at the end of this data sheet.

LVDS25E

The top and bottom sides of LatticeXP2 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.







Table 3-1. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/-1%)	158	Ω
R _P	Driver Parallel Resistor (+/-1%)	140	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage (after R _P)	1.43	V
V _{OL}	Output Low Voltage (after R _P)	1.07	V
V _{OD}	Output Differential Voltage (After R _P)	0.35	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	6.03	mA

LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3V VCCIO. The default drive current for LVCMOS33D output is 12mA with the option to change the device strength to 4mA, 8mA, 16mA or 20mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.



BLVDS

The LatticeXP2 devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.





Table 3-2. BLVDS DC Conditions¹

		Typical		
Parameter	Description	Ζο = 45 Ω	Ζο = 90 Ω	Units
V _{CCIO}	Output Driver Supply (+/- 5%)	2.50	2.50	V
Z _{OUT}	Driver Impedance	10.00	10.00	Ω
R _S	Driver Series Resistor (+/- 1%)	90.00	90.00	Ω
R _{TL}	Driver Parallel Resistor (+/- 1%)	45.00	90.00	Ω
R _{TR}	Receiver Termination (+/- 1%)	45.00	90.00	Ω
V _{OH}	Output High Voltage (After R _{TL})	1.38	1.48	V
V _{OL}	Output Low Voltage (After R _{TL})	1.12	1.02	V
V _{OD}	Output Differential Voltage (After R _{TL})	0.25	0.46	V
V _{CM}	Output Common Mode Voltage	1.25	1.25	V
I _{DC}	DC Output Current	11.24	10.20	mA

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.



Typical Building Block Function Performance¹

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	4.4	ns
32-bit Decoder	5.2	ns
64-bit Decoder	5.6	ns
4:1 MUX	3.7	ns
8:1 MUX	3.9	ns
16:1 MUX	4.3	ns
32:1 MUX	4.5	ns

Register-to-Register Performance

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	521	MHz
32-bit Decoder	537	MHz
64-bit Decoder	484	MHz
4:1 MUX	744	MHz
8:1 MUX	678	MHz
16:1 MUX	616	MHz
32:1 MUX	529	MHz
8-bit Adder	570	MHz
16-bit Adder	507	MHz
64-bit Adder	293	MHz
16-bit Counter	541	MHz
32-bit Counter	440	MHz
64-bit Counter	321	MHz
64-bit Accumulator	261	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	315	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	315	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	231	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (One PFU)	760	MHz
32x2 Pseudo-Dual Port RAM	455	MHz
64x1 Pseudo-Dual Port RAM	351	MHz
DSP Functions		
18x18 Multiplier (All Registers)	342	MHz
9x9 Multiplier (All Registers)	342	MHz
36x36 Multiply (All Registers)	330	MHz
18x18 Multiply/Accumulate (Input and Output Registers)	218	MHz
18x18 Multiply-Add/Sub-Sum (All Registers)	292	MHz



LatticeXP2 Internal Switching Characteristics¹ (Continued)

		-7 -6		-5				
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{RST_PIO}	Asynchronous reset time for PFU Logic	—	0.386	—	0.419	—	0.452	ns
t _{DEL}	Dynamic Delay Step Size	0.035	0.035	0.035	0.035	0.035	0.035	ns
EBR Timing	· · · · · ·							
t _{CO_EBR}	Clock (Read) to Output from Address or Data	_	2.774	_	3.142	_	3.510	ns
t _{COO_EBR}	Clock (Write) to Output from EBR Output Register	_	0.360	_	0.408	—	0.456	ns
^t SUDATA_EBR	Setup Data to EBR Memory (Write Clk)	-0.167	—	-0.198	_	-0.229	—	ns
t _{HDATA_EBR}	Hold Data to EBR Memory (Write Clk)	0.194	—	0.231	_	0.267	_	ns
t _{SUADDR_EBR}	Setup Address to EBR Memory (Write Clk)	-0.117	—	-0.137	_	-0.157	—	ns
t _{HADDR_EBR}	Hold Address to EBR Memory (Write Clk)	0.157	_	0.182	_	0.207	_	ns
t _{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory (Write/Read Clk)	-0.135	_	-0.159	_	-0.182	_	ns
t _{HWREN_EBR}	Hold Write/Read Enable to EBR Memory (Write/Read Clk)	0.158	—	0.186	_	0.214	_	ns
t _{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register (Read Clk)	0.144	—	0.160	_	0.176	_	ns
t _{HCE_EBR}	Clock Enable Hold Time to EBR Output Register (Read Clk)	-0.097	—	-0.113	_	-0.129	_	ns
t _{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register (Asynchro- nous)	_	1.156	_	1.341	_	1.526	ns
t _{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.117	—	-0.137	_	-0.157	_	ns
t _{HBE_EBR}	Byte Enable Hold Time to EBR Output Register Dynamic Delay on Each PIO	0.157	_	0.182	_	0.207	_	ns
t _{RSTREC_EBR}	Asynchronous reset recovery time for EBR	0.233	—	0.291		0.347	—	ns
t _{RST_EBR}	Asynchronous reset time for EBR	—	1.156	—	1.341	_	1.526	ns
PLL Paramete	ers							
t _{RSTKREC_PLL}	After RSTK De-assert, Recovery Time Before Next Clock Edge Can Toggle K-divider Counter	1.000	_	1.000	_	1.000	_	ns
t _{RSTREC_PLL}	After RST De-assert, Recovery Time Before Next Clock Edge Can Toggle M-divider Counter (Applies to M-Divider Portion of RST Only ²)	1.000	_	1.000		1.000	_	ns
DSP Block Tir	ning							
t _{SUI_DSP}	Input Register Setup Time	0.135		0.151		0.166		ns
t _{HI_DSP}	Input Register Hold Time	0.021	—	-0.006	—	-0.031		ns
t _{SUP_DSP}	Pipeline Register Setup Time	2.505	—	2.784	—	3.064	—	ns

Over Recommended Operating Conditions



LatticeXP2 Family Timing Adders^{1, 2, 3, 4}

Buffer Type	Description	-7	-6	-5	Units
Input Adjusters					
LVDS25	LVDS	-0.26	-0.11	0.04	ns
BLVDS25	BLVDS	-0.26	-0.11	0.04	ns
MLVDS	LVDS	-0.26	-0.11	0.04	ns
RSDS	RSDS	-0.26	-0.11	0.04	ns
LVPECL33	LVPECL	-0.26	-0.11	0.04	ns
HSTL18_I	HSTL_18 class I	-0.23	-0.08	0.07	ns
HSTL18_II	HSTL_18 class II	-0.23	-0.08	0.07	ns
HSTL18D_I	Differential HSTL 18 class I	-0.28	-0.13	0.02	ns
HSTL18D_II	Differential HSTL 18 class II	-0.28	-0.13	0.02	ns
HSTL15_I	HSTL_15 class I	-0.23	-0.09	0.06	ns
HSTL15D_I	Differential HSTL 15 class I	-0.28	-0.13	0.01	ns
SSTL33_I	SSTL_3 class I	-0.20	-0.04	0.12	ns
SSTL33_II	SSTL_3 class II	-0.20	-0.04	0.12	ns
SSTL33D_I	Differential SSTL_3 class I	-0.27	-0.11	0.04	ns
SSTL33D_II	Differential SSTL_3 class II	-0.27	-0.11	0.04	ns
SSTL25_I	SSTL_2 class I	-0.21	-0.06	0.10	ns
SSTL25_II	SSTL_2 class II	-0.21	-0.06	0.10	ns
SSTL25D_I	Differential SSTL_2 class I	-0.27	-0.12	0.03	ns
SSTL25D_II	Differential SSTL_2 class II	-0.27	-0.12	0.03	ns
SSTL18_I	SSTL_18 class I	-0.23	-0.08	0.07	ns
SSTL18_II	SSTL_18 class II	-0.23	-0.08	0.07	ns
SSTL18D_I	Differential SSTL_18 class I	-0.28	-0.13	0.02	ns
SSTL18D_II	Differential SSTL_18 class II	-0.28	-0.13	0.02	ns
LVTTL33	LVTTL	-0.09	0.05	0.18	ns
LVCMOS33	LVCMOS 3.3	-0.09	0.05	0.18	ns
LVCMOS25	LVCMOS 2.5	0.00	0.00	0.00	ns
LVCMOS18	LVCMOS 1.8	-0.23	-0.07	0.09	ns
LVCMOS15	LVCMOS 1.5	-0.20	-0.02	0.16	ns
LVCMOS12	LVCMOS 1.2	-0.35	-0.20	-0.04	ns
PCI33	3.3V PCI	-0.09	0.05	0.18	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E ⁵	-0.25	0.02	0.30	ns
LVDS25	LVDS 2.5	-0.25	0.02	0.30	ns
BLVDS25	BLVDS 2.5	-0.28	0.00	0.28	ns
MLVDS	MLVDS 2.5 ⁵	-0.28	0.00	0.28	ns
RSDS	RSDS 2.5⁵	-0.25	0.02	0.30	ns
LVPECL33	LVPECL 3.3 ⁵	-0.37	-0.10	0.18	ns
HSTL18_I	HSTL_18 class I 8mA drive	-0.17	0.13	0.43	ns
HSTL18_II	HSTL_18 class II	-0.29	0.00	0.29	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	-0.17	0.13	0.43	ns
HSTL18D_II	Differential HSTL 18 class II	-0.29	0.00	0.29	ns

Over Recommended Operating Conditions



LatticeXP2 sysCONFIG Port Timing Specifications

Parameter	Description	Min	Max	Units
sysCONFIG PO	R, Initialization and Wake Up			
t _{ICFG}	Minimum Vcc to INITN High	_	50	ms
t _{VMC}	Time from t _{ICFG} to valid Master CCLK	_	2	μs
t _{PRGMRJ}	PROGRAMN Pin Pulse Rejection	_	12	ns
t _{PRGM}	PROGRAMN Low Time to Start Configuration	50	—	ns
t _{DINIT} 1	PROGRAMN High to INITN High Delay	_	1	ms
t _{DPPINIT}	Delay Time from PROGRAMN Low to INITN Low	_	50	ns
t _{DPPDONE}	Delay Time from PROGRAMN Low to DONE Low	_	50	ns
t _{IODISS}	User I/O Disable from PROGRAMN Low	_	35	ns
t _{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	_	25	ns
t _{MWC}	Additional Wake Master Clock Signals after DONE Pin High	0	—	Cycles
sysCONFIG SP	I Port (Master)			
t _{CFGX}	INITN High to CCLK Low	_	1	μs
t _{CSSPI}	INITN High to CSSPIN Low	_	2	μs
t _{CSCCLK}	CCLK Low before CSSPIN Low	0	—	ns
t _{SOCDO}	CCLK Low to Output Valid	_	15	ns
t _{CSPID}	CSSPIN[0:1] Low to First CCLK Edge Setup Time	2cyc	600+6cyc	ns
f _{MAXSPI}	Max CCLK Frequency	—	20	MHz
t _{SUSPI}	SOSPI Data Setup Time Before CCLK	7	—	ns
t _{HSPI}	SOSPI Data Hold Time After CCLK	10	—	ns
sysCONFIG SP	I Port (Slave)			
f _{MAXSPIS}	Slave CCLK Frequency	—	25	MHz
t _{RF}	Rise and Fall Time	50	—	mV/ns
t _{STCO}	Falling Edge of CCLK to SOSPI Active	—	20	ns
t _{STOZ}	Falling Edge of CCLK to SOSPI Disable	—	20	ns
t _{STSU}	Data Setup Time (SISPI)	8	—	ns
t _{STH}	Data Hold Time (SISPI)	10	—	ns
t _{sтскн}	CCLK Clock Pulse Width, High	0.02	200	μs
t _{STCKL}	CCLK Clock Pulse Width, Low	0.02	200	μs
t _{STVO}	Falling Edge of CCLK to Valid SOSPI Output		20	ns
t _{SCS}	CSSPISN High Time	25	—	ns
t _{SCSS}	CSSPISN Setup Time	25	—	ns
t _{SCSH}	CSSPISN Hold Time	25	—	ns

Over Recommended Operating Conditions

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of PROGRAMN.



On-Chip Oscillator and Configuration Master Clock Characteristics

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value -30%	Selected value +30%	MHz
Duty Cycle	40	60	%

Over Recommended Operating Conditions

Figure 3-9. Master SPI Configuration Waveforms











Signal Descriptions (Cont.)

Signal Name	I/O	Description
TDO	0	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ		Power supply pin for JTAG Test Access Port.
Configuration Pads (Used during sysC	ONFIG)	
CFG[1:0]	Ι	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, an internal pull-up is enabled.
INITN ¹	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
SISPI ²	I/O	Input data pin in slave SPI mode and Output data pin in Master SPI mode.
SOSPI ²	I/O	Output data pin in slave SPI mode and Input data pin in Master SPI mode.
CSSPIN ²	0	Chip select for external SPI Flash memory in Master SPI mode. This pin has a weak internal pull-up.
CSSPISN	I	Chip select in Slave SPI mode. This pin has a weak internal pull-up.
TOE	I	Test Output Enable tristates all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to $\rm V_{\rm CC}$ is recommended.

1. If not actively driven, the internal pull-up may not be sufficient. An external pull-up resistor of 4.7k to $10k\Omega$ is recommended.

2. When using the device in Master SPI mode, it must be mutually exclusive from JTAG operations (i.e. TCK tied to GND) or the JTAG TCK must be free-running when used in a system JTAG test environment. If Master SPI mode is used in conjunction with a JTAG download cable, the device power cycle is required after the cable is unplugged.



PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins						
For Left and Right Edges of the Device								
D[Edgo] [n 4]	А	DQ						
r[Euge] [11-4]	В	DQ						
D[Edga] [n 2]	А	DQ						
r[Euge] [II-3]	В	DQ						
D[Edgo] [n 2]	А	DQ						
	В	DQ						
P[Edge] [n-1]	А	DQ						
	В	DQ						
P[Edge] [n]	А	[Edge]DQSn						
	В	DQ						
P[Edge] [n+1]	А	DQ						
	В	DQ						
P[Edge] [n+2]	А	DQ						
	В	DQ						
P[Edge] [n+3]	А	DQ						
	В	DQ						
For Top and Bottom Edge	es of the Device							
P[Edge] [n-4]	А	DQ						
	В	DQ						
P[Edge] [n-3]	A	DQ						
	В	DQ						
P[Edge] [n-2]	A	DQ						
. [=090] [=]	В	DQ						
P[Edge] [n-1]	A	DQ						
. [=090][]	В	DQ						
P[Edge] [n]	A	[Edge]DQSn						
. [====================================	В	DQ						
P[Edge] [n+1]	A	DQ						
. [=a90][]	В	DQ						
P[Edge] [n+2]	A	DQ						
. [=390] [5]	В	DQ						
P[Edge] [n+3]	A	DQ						
	В	DQ						
P[Edge] [n+4]	A	DQ						
. [=390][]	В	DQ						

Notes:

1. "n" is a row PIC number.

^{2.} The DDR interface is designed for memories that support one DQS strobe up to 16 bits of data for the left and right edges and up to 18 bits of data for the top and bottom edges. In some packages, all the potential DDR data (DQ) pins may not be available. PIC numbering definitions are provided in the "Signal Names" column of the Signal Descriptions table.



Pin Information Summary (Cont.)

XP2-5				XP2-8			XP2-17		XP2-30		XP2-40						
Pin Type		132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
	Bank0	18	20	20	26	18	20	20	28	20	28	52	28	52	70	52	70
	Bank1	4	6	18	18	4	6	18	22	18	22	36	22	36	54	36	70
	Bank2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI capable I/Os	Bank3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bank	Bank4	8	8	18	18	8	8	18	26	18	26	36	26	38	54	38	70
	Bank5	14	18	20	24	14	18	20	24	20	24	52	24	53	70	53	70
	Bank6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

Logic Signal Connections

Package pinout information can be found under "Data Sheets" on the LatticeXP2 product page of the Lattice website a www.latticesemi.com/products/fpga/xp2 and in the Lattice Diamond design software.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Lattice <u>Thermal Management</u> document to find the device/ package specific thermal values.

For Further Information

- TN1139, Power Estimation and Management for LatticeXP2 Devices
- Power Calculator tool is included with the Lattice Diamond design tool or as a standalone download from www.latticesemi.com/products/designsoftware



Lead-Free Packaging

Commercial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5MN132C	1.2V	-5	Lead-Free csBGA	132	COM	5
LFXP2-5E-6MN132C	1.2V	-6	Lead-Free csBGA	132	COM	5
LFXP2-5E-7MN132C	1.2V	-7	Lead-Free csBGA	132	COM	5
LFXP2-5E-5TN144C	1.2V	-5	Lead-Free TQFP	144	COM	5
LFXP2-5E-6TN144C	1.2V	-6	Lead-Free TQFP	144	COM	5
LFXP2-5E-7TN144C	1.2V	-7	Lead-Free TQFP	144	COM	5
LFXP2-5E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	5
LFXP2-5E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	5
LFXP2-5E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	5
LFXP2-5E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	5
LFXP2-5E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	5
LFXP2-5E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5MN132C	1.2V	-5	Lead-Free csBGA	132	COM	8
LFXP2-8E-6MN132C	1.2V	-6	Lead-Free csBGA	132	COM	8
LFXP2-8E-7MN132C	1.2V	-7	Lead-Free csBGA	132	COM	8
LFXP2-8E-5TN144C	1.2V	-5	Lead-Free TQFP	144	COM	8
LFXP2-8E-6TN144C	1.2V	-6	Lead-Free TQFP	144	COM	8
LFXP2-8E-7TN144C	1.2V	-7	Lead-Free TQFP	144	COM	8
LFXP2-8E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	8
LFXP2-8E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	8
LFXP2-8E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	8
LFXP2-8E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	8
LFXP2-8E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	8
LFXP2-8E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5QN208C	1.2V	-5	Lead-Free PQFP	208	COM	17
LFXP2-17E-6QN208C	1.2V	-6	Lead-Free PQFP	208	COM	17
LFXP2-17E-7QN208C	1.2V	-7	Lead-Free PQFP	208	COM	17
LFXP2-17E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	17
LFXP2-17E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	17
LFXP2-17E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	17
LFXP2-17E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	17
LFXP2-17E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	17
LFXP2-17E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	17



LatticeXP2 Family Data Sheet Revision History

September 2014

Data Sheet DS1009

Revision History

Date	Version	Section	Change Summary
May 2007	01.1	_	Initial release.
September 2007	01.2	DC and Switching Characteristics	Added JTAG Port Timing Waveforms diagram.
			Updated sysCLOCK PLL Timing table.
		Pinout Information	Added Thermal Management text section.
February 2008	01.3	Architecture	Added LVCMOS33D to Supported Output Standards table.
			Clarified: "This Flash can be programmed through either the JTAG or Slave SPI ports of the device. The SRAM configuration space can also be infinitely reconfigured through the JTAG and Master SPI ports."
			Added External Slave SPI Port to Serial TAG Memory section. Updated Serial TAG Memory diagram.
		DC and Switching Characteristics	Updated Flash Programming Specifications table.
			Added "8W" specification to Hot Socketing Specifications table.
			Updated Timing Tables
			Clarifications for IIH in DC Electrical Characteristics table.
			Added LVCMOS33D section
			Updated DOA and DOA (Regs) to EBR Timing diagrams.
			Removed Master Clock Frequency and Duty Cycle sections from the LatticeXP2 sysCONFIG Port Timing Specifications table. These are listed on the On-chip Oscillator and Configuration Master Clock Characteristics table.
			Changed CSSPIN to CSSPISN in description of $t_{SCS}, t_{SCSS},$ and t_{SCSH} parameters. Removed t_{SOE} parameter.
			Clarified On-chip Oscillator documentation
			Added Switching Test Conditions
		Pinout Information	Added "True LVDS Pairs Bonding Out per Bank," "DDR Banks Bonding Out per I/O Bank," and "PCI capable I/Os Bonding Out per Bank" to Pin Information Summary in place of previous blank table "PCI and DDR Capabilities of the Device-Package Combinations"
			Removed pinout listing. This information is available on the LatticeXP2 product web pages
		Ordering Information	Added XP2-17 "8W" and all other family OPNs.
April 2008	01.4	DC and Switching	Updated Absolute Maximum Ratings footnotes.
		Characteristics	Updated Recommended Operating Conditions Table footnotes.
		Updated Supply Current (Standby) Table	
			Updated Initialization Supply Current Table
			Updated Programming and Erase Flash Supply Current Table
			Updated Register to Register Performance Table
			Updated LatticeXP2 External Switching Characteristics Table
			Updated LatticeXP2 Internal Switching Characteristics Table
			Updated sysCLOCK PLL Timing Table

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