E.J. Lattice Semiconductor Corporation - <u>LFXP2-40E-6FN672C Datasheet</u>



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	5000
Number of Logic Elements/Cells	40000
Total RAM Bits	906240
Number of I/O	540
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-40e-6fn672c

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Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as LUT4s. A LUT4 has 16 possible input combinations. Fourinput logic functions are generated by programming the LUT4. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger LUTs such as LUT6, LUT7 and LUT8, can be constructed by concatenating two or more slices. Note that a LUT8 requires more than four slices.

Ripple Mode

Ripple mode allows efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with async clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Two carry signals, FCI and FCO, are generated per slice in this mode, allowing fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed Single Port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit Pseudo Dual Port RAM (PDPR) memory is created by using one slice as the read-write port and the other companion slice as the read-only port.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information on using RAM in LatticeXP2 devices, please see TN1137, <u>LatticeXP2 Memory Usage Guide</u>.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

Number of slices	3 3	

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in the ROM mode. Preloading is accomplished through the programming interface during PFU configuration.



Figure 2-4. General Purpose PLL (GPLL) Diagram



Table 2-4 provides a description of the signals in the GPLL blocks.

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
DPHASE [3:0]	I	DPA Phase Adjust input
DDDUTY [3:0]	I	DPA Duty Cycle Select input
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	0	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	0	PLL output clock to clock tree (no phase shift)
CLKOK	0	PLL output to clock tree through secondary clock divider
CLKOK2	0	PLL output to clock tree (CLKOP divided by 3)
LOCK	0	"1" indicates PLL LOCK to CLKI

Clock Dividers

LatticeXP2 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from the CLKOP output from the GPLLs or from the Edge Clocks (ECLK). The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets the input and forces all outputs to low. The RELEASE signal releases outputs to the input clock. For further information on clock dividers, please see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide. Figure 2-5 shows the clock divider connections.



Figure 2-12. Secondary Clock Selection



Slice Clock Selection

Figure 2-13 shows the clock selections and Figure 2-14 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals, via routing, can be used as clock inputs to the slices. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control, then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-13. Slice0 through Slice2 Clock Selection





sysMEM Memory

LatticeXP2 devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of 18 Kbit RAM with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-5. FIFOs can be implemented in sysMEM EBR blocks by using support logic with PFUs. The EBR block supports an optional parity bit for each data byte to facilitate parity checking. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths.

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

FlashBAK EBR Content Storage

All the EBR memory in the LatticeXP2 is shadowed by Flash memory. Optionally, initialization values for the memory blocks can be defined using the Lattice Diamond design tools. The initialization values are loaded into the Flash memory during device programming and into the SRAM at power up or whenever the device is reconfigured. This feature is ideal for the storage of a variety of information such as look-up tables and microprocessor code. It is also possible to write the current contents of the EBR memory back to Flash memory. This capability is useful for the storage of data such as error codes and calibration information. For additional information on the FlashBAK capability see TN1137, LatticeXP2 Memory Usage Guide.



- In the 'Signed/Unsigned' options the operands can be switched between signed and unsigned on every cycle.
- In the 'Add/Sub' option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-20 shows the MULT sysDSP element.

Figure 2-20. MULT sysDSP Element





MULTADDSUB sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. The user can enable the input, output and pipeline registers. Figure 2-22 shows the MULTADDSUB sysDSP element.

Figure 2-22. MULTADDSUB





Table 2-11. PIO Signal List

Name	Туре	Description
CE	Control from the core	Clock enables for input and output block flip-flops
CLK	Control from the core	System clocks for input and output blocks
ECLK1, ECLK2	Control from the core	Fast edge clocks
LSR	Control from the core	Local Set/Reset
GSRN	Control from routing	Global Set/Reset (active low)
INCK ²	Input to the core	Input to Primary Clock Network or PLL reference inputs
DQS	Input to PIO	DQS signal from logic (routing) to PIO
INDD	Input to the core	Unregistered data input to core
INFF	Input to the core	Registered input on positive edge of the clock (CLK0)
IPOS0, IPOS1	Input to the core	Double data rate registered inputs to the core
QPOS0 ¹ , QPOS1 ¹	Input to the core	Gearbox pipelined inputs to the core
QNEG0 ¹ , QNEG1 ¹	Input to the core	Gearbox pipelined inputs to the core
OPOS0, ONEG0, OPOS2, ONEG2	Output data from the core	Output signals from the core for SDR and DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation
DEL[3:0]	Control from the core	Dynamic input delay control bits
TD	Tristate control from the core	Tristate signal from the core used in SDR operation
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block
DQSXFER	Control from core	Controls signal to the Output block

1. Signals available on left/right/bottom only.

2. Selected I/O.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with necessary clock and selection logic.

Input Register Block

The input register blocks for PIOs contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-26 shows the diagram of the input register block.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the Single Data Rate (SDR) mode, the data is registered, by one of the registers in the SDR Sync register block, with the system clock. In DDR mode two registers are used to sample the data on the positive and negative edges of the DQS signal which creates two data streams, D0 and D2. D0 and D2 are synchronized with the system clock before entering the core. Further information on this topic can be found in the DDR Memory Support section of this data sheet.

By combining input blocks of the complementary PIOs and sharing registers from output blocks, a gearbox function can be implemented, that takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-26 shows the diagram using this gearbox function. For more information on this topic, please see TN1138, LatticeXP2 High Speed I/O Interface.



Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-27 shows the Tristate Register Block with the Output Block

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as Dtype or latch. In DDR mode, ONEG1 and OPOS1 are fed into registers on the positive edge of the clock. Then in the next clock the registered OPOS1 is latched. A multiplexer running off the same clock cycle selects the correct register for feeding to the output (D0).

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock signal is selected from general purpose routing, ECLK1, ECLK2 or a DQS signal (from the programmable DQS pin) and is provided to the input register block. The clock can optionally be inverted.

DDR Memory Support

PICs have additional circuitry to allow implementation of high speed source synchronous and DDR memory interfaces.

PICs have registered elements that support DDR memory interfaces. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the top and bottom are designed for memories that support 18 bits of data. One of every 16 PIOs on the left and right and one of every 18 PIOs on the top and bottom contain delay elements to facilitate the generation of DQS signals. The DQS signals feed the DQS buses which span the set of 16 or 18 PIOs. Figure 2-28 and Figure 2-29 show the DQS pin assignments in each set of PIOs.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. For additional information on using DDR memory support please see TN1138, <u>LatticeXP2 High Speed I/O Interface</u>.



Figure 2-31. DQS Local Bus



*DQSXFERDEL shifts ECLK1 by 90% and is not associated with a particular PIO.

Polarity Control Logic

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeXP2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block and requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.



and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards. For more information, please see TN1141, LatticeXP2 sysCONFIG Usage Guide.

flexiFLASH Device Configuration

The LatticeXP2 devices combine Flash and SRAM on a single chip to provide users with flexibility in device programming and configuration. Figure 2-33 provides an overview of the arrangement of Flash and SRAM configuration cells within the device. The remainder of this section provides an overview of these capabilities. See TN1141, LatticeXP2 sysCONFIG Usage Guide for a more detailed description.



Figure 2-33. Overview of Flash and SRAM Configuration Cells Within LatticeXP2 Devices

At power-up, or on user command, data is transferred from the on-chip Flash memory to the SRAM configuration cells that control the operation of the device. This is done with massively parallel buses enabling the parts to operate within microseconds of the power supplies reaching valid levels; this capability is referred to as Instant-On.

The on-chip Flash enables a single-chip solution eliminating the need for external boot memory. This Flash can be programmed through either the JTAG or Slave SPI ports of the device. The SRAM configuration space can also be infinitely reconfigured through the JTAG and Master SPI ports. The JTAG port is IEEE 1149.1 and IEEE 1532 compliant.

As described in the EBR section of the data sheet, the FlashBAK capability of the parts enables the contents of the EBR blocks to be written back into the Flash storage area without erasing or reprogramming other aspects of the device configuration. Serial TAG memory is also available to allow the storage of small amounts of data such as calibration coefficients and error codes.

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM only FPGAs. This is further enhanced by device locking. The device can be in one of three modes:



Density Shifting

The LatticeXP2 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.



Supply Current (Standby)^{1, 2, 3, 4}

Symbol	Parameter	Device	Typical⁵	Units
		XP2-5	14	mA
Icc		XP2-8	18	mA
	Core Power Supply Current	XP2-17	24	mA
		XP2-30	35	mA
		XP2-40	45	mA
Iccaux		XP2-5	15	mA
		XP2-8	15	mA
	Auxiliary Power Supply Current ⁶	XP2-17	15	mA
		XP2-30	16	mA
		XP2-40	16	mA
I _{CCPLL}	PLL Power Supply Current (per PLL)		0.1	mA
I _{CCIO}	Bank Power Supply Current (per bank)		2	mA
ICCJ	V _{CCJ} Power Supply Current		0.25	mA

Over Recommended Operating Conditions

1. For further information on supply current, please see TN1139, Power Estimation and Management for LatticeXP2 Devices.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

3. Frequency 0 MHz.

4. Pattern represents a "blank" configuration data file.

5. $T_J = 25^{\circ}C$, power supplies at nominal voltage.

6. In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.



sysIO Differential Electrical Characteristics LVDS

Parameter	Description	Test Conditions	Min.	Тур.	Max.	Units
V _{INP} , V _{INM}	Input Voltage		0		2.4	V
V _{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	_	2.35	V
V _{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	_	—	mV
I _{IN}	Input Current	Power On or Power Off			+/-10	μA
V _{OH}	Output High Voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	_	1.38	1.60	V
V _{OL}	Output Low Voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	0.9V	1.03	—	V
V _{OD}	Output Voltage Differential	(V _{OP} - V _{OM}), R _T = 100 Ohm	250	350	450	mV
ΔV _{OD}	Change in V _{OD} Between High and Low		_	_	50	mV
V _{OS}	Output Voltage Offset	(V _{OP} + V _{OM})/2, R _T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V _{OS} Between H and L			_	50	mV
I _{SA}	Output Short Circuit Current	V _{OD} = 0V Driver Outputs Shorted to Ground	_	_	24	mA
I _{SAB}	Output Short Circuit Current	V _{OD} = 0V Driver Outputs Shorted to Each Other	_	_	12	mA

Over Recommended Operating Conditions

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see details in additional technical notes listed at the end of this data sheet.

LVDS25E

The top and bottom sides of LatticeXP2 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.







Table 3-1. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/-1%)	158	Ω
R _P	Driver Parallel Resistor (+/-1%)	140	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage (after R _P)	1.43	V
V _{OL}	Output Low Voltage (after R _P)	1.07	V
V _{OD}	Output Differential Voltage (After R _P)	0.35	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	6.03	mA

LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3V VCCIO. The default drive current for LVCMOS33D output is 12mA with the option to change the device strength to 4mA, 8mA, 16mA or 20mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.



LatticeXP2 External Switching Characteristics (Continued)

			-7		-6		-5		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
		XP2-5	1.00		1.30	_	1.60		ns
		XP2-8	1.00	_	1.30	_	1.60	_	ns
t _{HE}	Clock to Data Hold - PIO Input Register	XP2-17	1.00		1.30	_	1.60		ns
		XP2-30	1.20		1.60	_	1.90		ns
		XP2-40	1.20		1.60		1.90		ns
		XP2-5	1.00		1.30	_	1.60		ns
		XP2-8	1.00		1.30	_	1.60		ns
t _{SU_DELE}	Clock to Data Setup - PIO Input Begister with Data Input Delay	XP2-17	1.00		1.30	_	1.60		ns
		XP2-30	1.20		1.60		1.90		ns
		XP2-40	1.20		1.60		1.90		ns
		XP2-5	0.00		0.00		0.00		ns
		XP2-8	0.00	—	0.00	—	0.00	—	ns
t _{H_DELE}	Clock to Data Hold - PIO Input Begister with Input Data Delay	XP2-17	0.00	—	0.00	—	0.00	—	ns
		XP2-30	0.00		0.00		0.00		ns
		XP2-40	0.00		0.00		0.00		ns
f _{MAX_IOE}	Clock Frequency of I/O and PFU Register	XP2	_	420	_	357	_	311	MHz
General I/O Pir	Parameters (using Primary Clo	ck with PLL)1	1	1	1	1	1	
		XP2-5	—	3.00	—	3.30	—	3.70	ns
		XP2-8		3.00		3.30		3.70	ns
t _{COPLL}	Clock to Output - PIO Output Register	XP2-17		3.00		3.30		3.70	ns
		XP2-30	_	3.00		3.30		3.70	ns
		XP2-40		3.00		3.30		3.70	ns
		XP2-5	1.00		1.20		1.40		ns
		XP2-8	1.00		1.20		1.40		ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	XP2-17	1.00		1.20		1.40		ns
		XP2-30	1.00		1.20		1.40		ns
		XP2-40	1.00		1.20	_	1.40		ns
		XP2-5	0.90		1.10		1.30		ns
		XP2-8	0.90		1.10		1.30		ns
t _{HPLL}	Clock to Data Hold - PIO Input	XP2-17	0.90		1.10		1.30		ns
		XP2-30	1.00	—	1.20	—	1.40	—	ns
		XP2-40	1.00	—	1.20	—	1.40	—	ns
		XP2-5	1.90	—	2.10	—	2.30	—	ns
		XP2-8	1.90		2.10	—	2.30	_	ns
t _{SU_DELPLL}	Clock to Data Setup - PIO Input Begister with Data Input Delay	XP2-17	1.90	—	2.10	—	2.30	—	ns
	lingibion with Data input Delay	XP2-30	2.00	—	2.20	—	2.40	—	ns
		XP2-40	2.00	—	2.20	—	2.40	—	ns

Over Recommended Operating Conditions



Flash Download Time (from On-Chip Flash to SRAM)

Over Recommended Operating Conditions

Symbol	Parar	neter	Min.	Тур.	Max.	Units
	PROGRAMN Low-to-	XP2-5	—	1.8	2.1	ms
		XP2-8	—	1.9	2.3	ms
	High. Transition to Done	XP2-17	—	1.7	2.0	ms
•	High.	XP2-30	—	2.0	2.1	ms
		XP2-40	—	2.0	2.3	ms
'REFRESH	Power-up refresh when PROGRAMN is pulled	XP2-5	—	1.8	2.1	ms
		XP2-8	—	1.9	2.3	ms
		XP2-17	—	1.7	2.0	ms
	$(V_{CC}=V_{CC} Min)$	XP2-30	—	2.0	2.1	ms
		XP2-40		2.0	2.3	ms

Flash Program Time

Over Recommended Operating Conditions

	Flash Density		Program Time	
Device			Тур.	Units
	1.0M	TAG	1.0	ms
XF2-5	1.2101	Main Array	1.1	S
	2.0M	TAG	1.0	ms
AF 2-0	2.0101	Main Array	1.4	S
XP2-17	3.6M	TAG	1.0	ms
		Main Array	1.8	S
	6.014	TAG	2.0	ms
XP2-30	6.UIVI	Main Array	3.0	S
VP2 40	8 OM	TAG	2.0	ms
ΛΓ 2 -40	8.0101	Main Array	4.0	S

Flash Erase Time

Over Recommended Operating Conditions

			Erase Time		
Device	Flash I	Density	Тур.	Units	
	1.2M	TAG	1.0	s	
XI 2-3	1.2101	Main Array	3.0	s	
XP2-8	2.0M	TAG	1.0	S	
	2.0101	Main Array	4.0	s	
XP2-17	2.6M	TAG	1.0	s	
	3.01	Main Array	5.0	S	
XP2-30	6 OM	TAG	2.0	s	
	0.0101	Main Array	7.0	s	
XP2-40	8.0M	TAG	2.0	S	
	0.0101	Main Array	9.0	S	



Signal Descriptions (Cont.)

Signal Name	I/O	Description
TDO	0	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ		Power supply pin for JTAG Test Access Port.
Configuration Pads (Used during sysC	ONFIG)	
CFG[1:0]	Ι	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, an internal pull-up is enabled.
INITN ¹	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
SISPI ²	I/O	Input data pin in slave SPI mode and Output data pin in Master SPI mode.
SOSPI ²	I/O	Output data pin in slave SPI mode and Input data pin in Master SPI mode.
CSSPIN ²	0	Chip select for external SPI Flash memory in Master SPI mode. This pin has a weak internal pull-up.
CSSPISN	I	Chip select in Slave SPI mode. This pin has a weak internal pull-up.
TOE	I	Test Output Enable tristates all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to $\rm V_{\rm CC}$ is recommended.

1. If not actively driven, the internal pull-up may not be sufficient. An external pull-up resistor of 4.7k to $10k\Omega$ is recommended.

2. When using the device in Master SPI mode, it must be mutually exclusive from JTAG operations (i.e. TCK tied to GND) or the JTAG TCK must be free-running when used in a system JTAG test environment. If Master SPI mode is used in conjunction with a JTAG download cable, the device power cycle is required after the cable is unplugged.



Pin Information Summary

		XP2-5			XP2-8			XP2-17		XP2-30		XP2-40					
Pin Ty	ре	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
Single Ended Us	er I/O	86	100	146	172	86	100	146	201	146	201	358	201	363	472	363	540
Differential Pair	Normal	35	39	57	66	35	39	57	77	57	77	135	77	137	180	137	204
User I/O	Highspeed	8	11	16	20	8	11	16	23	16	23	44	23	44	56	44	66
	TAP	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
Configuration	Muxed	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9
	Dedicated	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Non Configura-	Muxed	5	5	7	7	7	7	9	9	11	11	21	7	11	13	11	13
tion	Dedicated	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Vcc		6	4	9	6	6	4	9	6	9	6	16	6	16	20	16	20
Vccaux		4	4	4	4	4	4	4	4	4	4	8	4	8	8	8	8
VCCPLL		2	2	2	-	2	2	2	-	4	-	-	-	-	-	-	-
	Bank0	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
	Bank1	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank2	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
VCCIO	Bank3	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
10010	Bank4	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank5	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
	Bank6	1	1	2	2	1	1	2	2	2	2	4	2	4	4	4	4
	Bank7	2	2	2	2	2	2	2	2	2	2	4	2	4	4	4	4
GND, GND0-GNI	77	15	15	20	20	15	15	22	20	22	20	56	20	56	64	56	64
NC		-	-	4	31	-	-	2	2	-	2	7	2	2	69	2	1
	Bank0	18/9	20/10	20/10	26/13	18/9	20/10	20/10	28/14	20/10	28/14	52/26	28/14	52/26	70/35	52/26	70/35
Single Ended/	Bank1	4/2	6/3	18/9	18/9	4/2	6/3	18/9	22/11	18/9	22/11	36/18	22/11	36/18	54/27	36/18	70/35
	Bank2	16/8	18/9	18/9	22/11	16/8	18/9	18/9	26/13	18/9	26/13	46/23	26/13	46/23	56/28	46/23	64/32
	Bank3	4/2	4/2	16/8	20/10	4/2	4/2	16/8	24/12	16/8	24/12	44/22	24/12	46/23	56/28	46/23	66/33
per Bank	Bank4	8/4	8/4	18/9	18/9	8/4	8/4	18/9	26/13	18/9	26/13	36/18	26/13	38/19	54/27	38/19	70/35
	Bank5	14/7	18/9	20/10	24/12	14/7	18/9	20/10	24/12	20/10	24/12	52/26	24/12	53/26	70/35	53/26	70/35
	Bank6	6/3	8/4	18/9	22/11	6/3	8/4	18/9	27/13	18/9	27/13	46/23	27/13	46/23	56/28	46/23	66/33
	Bank7	16/8	18/9	18/9	22/11	16/8	18/9	18/9	24/12	18/9	24/12	46/23	24/12	46/23	56/28	46/23	64/32
	Bank0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank2	3	4	4	5	3	4	4	6	4	6	11	6	11	14	11	16
True LVDS Pairs	Bank3	1	1	4	5	1	1	4	6	4	6	11	6	11	14	11	17
Bank	Bank4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank6	1	2	4	5	1	2	4	6	4	6	11	6	11	14	11	17
	Bank7	3	4	4	5	3	4	4	5	4	5	11	5	11	14	11	16
	Bank0	1	1	1	1	1	1	1	1	1	1	3	1	2	4	2	4
	Bank1	0	0	1	1	0	0	1	1	1	1	2	1	2	3	2	4
	Bank2	1	1	1	1	1	1	1	1	1	1	2	1	3	3	3	4
DDR Banks	Bank3	0	0	1	1	0	0	1	1	1	1	2	1	3	3	3	4
I/O Bank ¹	Bank4	0	0	1	1	0	0	1	1	1	1	2	1	2	3	2	4
	Bank5	1	1	1	1	1	1	1	1	1	1	3	1	2	4	2	4
	Bank6	0	0	1	1	0	0	1	1	1	1	2	1	3	3	3	4
	Bank7	1	1	1	1	1	1	1	1	1	1	2	1	3	3	3	4



Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5QN208I	1.2V	-5	Lead-Free PQFP	208	IND	17
LFXP2-17E-6QN208I	1.2V	-6	Lead-Free PQFP	208	IND	17
LFXP2-17E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	17
LFXP2-17E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	17
LFXP2-17E-5FN484I	1.2V	-5	Lead-Free fpBGA	484	IND	17
LFXP2-17E-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	17

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-30E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	30
LFXP2-30E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	30
LFXP2-30E-5FN484I	1.2V	-5	Lead-Free fpBGA	484	IND	30
LFXP2-30E-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	30
LFXP2-30E-5FN672I	1.2V	-5	Lead-Free fpBGA	672	IND	30
LFXP2-30E-6FN672I	1.2V	-6	Lead-Free fpBGA	672	IND	30

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5FN484I	1.2V	-5	Lead-Free fpBGA	484	IND	40
LFXP2-40E-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	40
LFXP2-40E-5FN672I	1.2V	-5	Lead-Free fpBGA	672	IND	40
LFXP2-40E-6FN672I	1.2V	-6	Lead-Free fpBGA	672	IND	40



Date	Version	Section	Change Summary				
April 2008	01.4	DC and Switching	Updated Flash Download Time (From On-Chip Flash to SRAM) Table				
(cont.)	(cont.)	Characteristics (cont.)	Updated Flash Program Time Table				
			Updated Flash Erase Time Table				
			Updated FlashBAK (from EBR to Flash) Table				
			Updated Hot Socketing Specifications Table footnotes				
		Pinout Information	Updated Signal Descriptions Table				
June 2008	01.5	Architecture	Removed Read-Before-Write sysMEM EBR mode.				
			Clarification of the operation of the secondary clock regions.				
		DC and Switching Characteristics	Removed Read-Before-Write sysMEM EBR mode.				
		Pinout Information	Updated DDR Banks Bonding Out per I/O Bank section of Pin Informa- tion Summary Table.				
August 2008	01.6	—	Data sheet status changed from preliminary to final.				
		Architecture	Clarification of the operation of the secondary clock regions.				
		DC and Switching Characteristics	Removed "8W" specification from Hot Socketing Specifications table.				
			Removed "8W" footnote from DC Electrical Characteristics table.				
			Updated Register-to-Register Performance table.				
		Ordering Information	Removed "8W" option from Part Number Description.				
			Removed XP2-17 "8W" OPNs.				
April 2011	01.7	DC and Switching Characteristics	Recommended Operating Conditions table, added footnote 5.				
			On-Chip Flash Memory Specifications table, added footnote 1.				
			BLVDS DC Conditions, corrected column title to be Z0 = 90 ohms.				
			sysCONFIG Port Timing Specifications table, added footnote 1 for t _{DINIT} .				
January 2012	01.8	Multiple	Added support for Lattice Diamond design software.				
		Architecture	Corrected information regarding SED support.				
		DC and Switching Characteristics	Added reference to ESD Performance Qualification Summary informa- tion.				
May 2013	01.9	All	Updated document with new corporate logo.				
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.				
			Added information regarding SED support.				
		DC and Switching Characteristics	Removed Input Clock Rise/Fall Time 1ns max from the sysCLOCK PLL Timing table.				
		Ordering Information	Updated topside mark in Ordering Information diagram.				
March 2014	02.0	Architecture	Updated Typical sysIO I/O Behavior During Power-up section. Added information on POR signal deactivation.				
August 2014	02.1	Architecture	Updated Typical sysIO I/O Behavior During Power-up section. Described user I/Os during power up and before FPGA core logic is active.				
September 2014	2.2	DC and Switching Characteristics	Updated Switching Test Conditions section. Re-linked missing figure.				