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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	625
Number of Logic Elements/Cells	5000
Total RAM Bits	169984
Number of I/O	172
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-5e-5ft256c

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# LatticeXP2 Family Data Sheet Introduction

#### February 2012

## Features

- flexiFLASH<sup>™</sup> Architecture
  - Instant-on
  - Infinitely reconfigurable
  - Single chip
  - FlashBAK<sup>™</sup> technology
  - Serial TAG memory
  - Design security

#### Live Update Technology

- TransFR<sup>™</sup> technology
- Secure updates with 128 bit AES encryption
- Dual-boot with external SPI

#### ■ sysDSP<sup>™</sup> Block

- Three to eight blocks for high performance Multiply and Accumulate
- 12 to 32 18x18 multipliers
- Each block supports one 36x36 multiplier or four 18x18 or eight 9x9 multipliers

#### Embedded and Distributed Memory

- Up to 885 Kbits sysMEM<sup>™</sup> EBR
- Up to 83 Kbits Distributed RAM

#### ■ sysCLOCK<sup>™</sup> PLLs

- Up to four analog PLLs per device
- Clock multiply, divide and phase shifting

## Flexible I/O Buffer

- sysIO<sup>™</sup> buffer supports:
  - LVCMOS 33/25/18/15/12; LVTTL
  - SSTL 33/25/18 class I, II
  - HSTL15 class I; HSTL18 class I, II
  - PCI
  - LVDS, Bus-LVDS, MLVDS, LVPECL, RSDS
- Pre-engineered Source Synchronous Interfaces
  - DDR / DDR2 interfaces up to 200 MHz
  - 7:1 LVDS interfaces support display applications
  - XGMII
- Density And Package Options
  - 5k to 40k LUT4s, 86 to 540 I/Os
  - csBGA, TQFP, PQFP, ftBGA and fpBGA packages
  - Density migration supported
- Flexible Device Configuration
  - SPI (master and slave) Boot Flash Interface
  - Dual Boot Image supported
  - Soft Error Detect (SED) macro embedded

## System Level Support

- IEEE 1149.1 and IEEE 1532 Compliant
- · On-chip oscillator for initialization & general use
- Devices operate with 1.2V power supply

Device	XP2-5	XP2-8	XP2-17	XP2-30	XP2-40
LUTs (K)	5	8	17	29	40
Distributed RAM (KBits)	10	18	35	56	83
EBR SRAM (KBits)	166	221	276	387	885
EBR SRAM Blocks	9	12	15	21	48
sysDSP Blocks	3	4	5	7	8
18 x 18 Multipliers	12	16	20	28	32
V <sub>CC</sub> Voltage	1.2	1.2	1.2	1.2	1.2
GPLL	2	2	4	4	4
Max Available I/O	172	201	358	472	540
Packages and I/O Combinations					•
132-Ball csBGA (8 x 8 mm)	86	86			
144-Pin TQFP (20 x 20 mm)	100	100			
208-Pin PQFP (28 x 28 mm)	146	146	146		
256-Ball ftBGA (17 x17 mm)	172	201	201	201	
484-Ball fpBGA (23 x 23 mm)			358	363	363
672-Ball fpBGA (27 x 27 mm)				472	540

## Table 1-1. LatticeXP2 Family Selection Guide

#### Data Sheet DS1009

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## Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

#### Logic Mode

In this mode, the LUTs in each slice are configured as LUT4s. A LUT4 has 16 possible input combinations. Fourinput logic functions are generated by programming the LUT4. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger LUTs such as LUT6, LUT7 and LUT8, can be constructed by concatenating two or more slices. Note that a LUT8 requires more than four slices.

#### **Ripple Mode**

Ripple mode allows efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with async clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two carry signals, FCI and FCO, are generated per slice in this mode, allowing fast arithmetic functions to be constructed by concatenating slices.

#### RAM Mode

In this mode, a 16x4-bit distributed Single Port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit Pseudo Dual Port RAM (PDPR) memory is created by using one slice as the read-write port and the other companion slice as the read-only port.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information on using RAM in LatticeXP2 devices, please see TN1137, <u>LatticeXP2 Memory Usage Guide</u>.

#### Table 2-3. Number of Slices Required For Implementing Distributed RAM

Number of slices	3 3	

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

#### **ROM Mode**

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in the ROM mode. Preloading is accomplished through the programming interface during PFU configuration.



# Routing

There are many resources provided in the LatticeXP2 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) or x6 (spans seven PFU) connections. The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered to allow both short and long connections routing between PFUs.

The LatticeXP2 family has an enhanced routing architecture to produce a compact design. The Diamond design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

# sysCLOCK Phase Locked Loops (PLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The LatticeXP2 family supports between two and four full featured General Purpose PLLs (GPLL). The architecture of the GPLL is shown in Figure 2-4.

CLKI, the PLL reference frequency, is provided either from the pin or from routing; it feeds into the Input Clock Divider block. CLKFB, the feedback signal, is generated from CLKOP (the primary clock output) or from a user clock pin/logic. CLKFB feeds into the Feedback Divider and is used to multiply the reference frequency.

Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. The phase and frequency of the VCO are determined from the input path and feedback signals. A LOCK signal is generated by the VCO to indicate that the VCO is locked with the input clock signal.

The output of the VCO feeds into the CLKOP Divider, a post-scalar divider. The duty cycle of the CLKOP Divider output can be fine tuned using the Duty Trim block, which creates the CLKOP signal. By allowing the VCO to operate at higher frequencies than CLKOP, the frequency range of the GPLL is expanded. The output of the CLKOP Divider is passed through the CLKOK Divider, a secondary clock divider, to generate lower frequencies for the CLKOK output. For applications that require even lower frequencies, the CLKOP signal is passed through a divide-by-three divider to produce the CLKOK2 output. The CLKOK2 output is provided for applications that use source synchronous logic. The Phase/Duty Cycle/Duty Trim block is used to adjust the phase and duty cycle of the CLKOP Divider output to generate the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The clock outputs from the GPLL; CLKOP, CLKOK, CLKOK2 and CLKOS, are fed to the clock distribution network.

For further information on the GPLL please see TN1126, LatticeXP2 sysCLOCK PLL Design and Usage Guide.



## Primary Clock Routing

The clock routing structure in LatticeXP2 devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-9 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally.





## **Dynamic Clock Select (DCS)**

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved irrespective of when the select signal is toggled. There are two DCS blocks per quadrant; in total, eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-9).

Figure 2-10 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, please see TN1126, <u>LatticeXP2 sysCLOCK PLL Design and</u> <u>Usage Guide</u>.

#### Figure 2-10. DCS Waveforms



## Secondary Clock/Control Routing

Secondary clocks in the LatticeXP2 devices are region-based resources. The benefit of region-based resources is the relatively low injection delay and skew within the region, as compared to primary clocks. EBR rows, DSP rows and a special vertical routing channel bound the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP block in the DSP row or the center of the DSP row. Figure 2-11 shows this special vertical routing channel and the eight secondary clock regions for the LatticeXP2-40.



## Figure 2-12. Secondary Clock Selection



## Slice Clock Selection

Figure 2-13 shows the clock selections and Figure 2-14 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals, via routing, can be used as clock inputs to the slices. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control, then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

## Figure 2-13. Slice0 through Slice2 Clock Selection





- In the 'Signed/Unsigned' options the operands can be switched between signed and unsigned on every cycle.
- In the 'Add/Sub' option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

## **MULT sysDSP Element**

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-20 shows the MULT sysDSP element.

#### Figure 2-20. MULT sysDSP Element





#### Table 2-11. PIO Signal List

Name	Туре	Description
CE	Control from the core	Clock enables for input and output block flip-flops
CLK	Control from the core	System clocks for input and output blocks
ECLK1, ECLK2	Control from the core	Fast edge clocks
LSR	Control from the core	Local Set/Reset
GSRN	Control from routing	Global Set/Reset (active low)
INCK <sup>2</sup>	Input to the core	Input to Primary Clock Network or PLL reference inputs
DQS	Input to PIO	DQS signal from logic (routing) to PIO
INDD	Input to the core	Unregistered data input to core
INFF	Input to the core	Registered input on positive edge of the clock (CLK0)
IPOS0, IPOS1	Input to the core	Double data rate registered inputs to the core
QPOS0 <sup>1</sup> , QPOS1 <sup>1</sup>	Input to the core	Gearbox pipelined inputs to the core
QNEG0 <sup>1</sup> , QNEG1 <sup>1</sup>	Input to the core	Gearbox pipelined inputs to the core
OPOS0, ONEG0, OPOS2, ONEG2	Output data from the core	Output signals from the core for SDR and DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation
DEL[3:0]	Control from the core	Dynamic input delay control bits
TD	Tristate control from the core	Tristate signal from the core used in SDR operation
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block
DQSXFER	Control from core	Controls signal to the Output block

1. Signals available on left/right/bottom only.

2. Selected I/O.

# PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with necessary clock and selection logic.

## Input Register Block

The input register blocks for PIOs contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-26 shows the diagram of the input register block.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the Single Data Rate (SDR) mode, the data is registered, by one of the registers in the SDR Sync register block, with the system clock. In DDR mode two registers are used to sample the data on the positive and negative edges of the DQS signal which creates two data streams, D0 and D2. D0 and D2 are synchronized with the system clock before entering the core. Further information on this topic can be found in the DDR Memory Support section of this data sheet.

By combining input blocks of the complementary PIOs and sharing registers from output blocks, a gearbox function can be implemented, that takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-26 shows the diagram using this gearbox function. For more information on this topic, please see TN1138, LatticeXP2 High Speed I/O Interface.



original backup configuration and try again. This all can be done without power cycling the system. For more information please see TN1220, <u>LatticeXP2 Dual Boot Feature</u>.

For more information on device configuration, please see TN1141, LatticeXP2 sysCONFIG Usage Guide.

## Soft Error Detect (SED) Support

LatticeXP2 devices have dedicated logic to perform Cyclic Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, LatticeXP2 devices can be programmed for checking soft errors in SRAM. SED can be run on a programmed device when the user logic is not active. In the event a soft error occurs, the device can be programmed to either reload from a known good boot image (from internal Flash or external SPI memory) or generate an error signal.

For further information on SED support, please see TN1130, LatticeXP2 Soft Error Detection (SED) Usage Guide.

## **On-Chip Oscillator**

Every LatticeXP2 device has an internal CMOS oscillator that is used to derive a Master Clock (CCLK) for configuration. The oscillator and CCLK run continuously and are available to user logic after configuration is complete. The available CCLK frequencies are listed in Table 2-14. When a different CCLK frequency is selected during the design process, the following sequence takes place:

- 1. Device powers up with the default CCLK frequency.
- 2. During configuration, users select a different CCLK frequency.
- 3. CCLK frequency changes to the selected frequency after clock configuration bits are received.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1141, <u>LatticeXP2 sysCON-FIG Usage Guide</u>.

Table 2-14. Selectable	CCLKs and Oscillato	r Freauencies Durina	Configuration and	User Mode

CCLK/Oscillator (MHz)
2.5 <sup>1</sup>
3.1 <sup>2</sup>
4.3
5.4
6.9
8.1
9.2
10
13
15
20
26
32
40
54
80 <sup>3</sup>
163 <sup>3</sup>
1 Software default oscillator frequency

1. Software default oscillator frequency.

2. Software default CCLK frequency.

3. Frequency not valid for CCLK.



# **Density Shifting**

The LatticeXP2 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.



#### Table 3-1. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V <sub>CCIO</sub>	Output Driver Supply (+/-5%)	2.50	V
Z <sub>OUT</sub>	Driver Impedance	20	Ω
R <sub>S</sub>	Driver Series Resistor (+/-1%)	158	Ω
R <sub>P</sub>	Driver Parallel Resistor (+/-1%)	140	Ω
R <sub>T</sub>	Receiver Termination (+/-1%)	100	Ω
V <sub>OH</sub>	Output High Voltage (after R <sub>P</sub> )	1.43	V
V <sub>OL</sub>	Output Low Voltage (after R <sub>P</sub> )	1.07	V
V <sub>OD</sub>	Output Differential Voltage (After R <sub>P</sub> )	0.35	V
V <sub>CM</sub>	Output Common Mode Voltage	1.25	V
Z <sub>BACK</sub>	Back Impedance	100.5	Ω
I <sub>DC</sub>	DC Output Current	6.03	mA

## LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3V VCCIO. The default drive current for LVCMOS33D output is 12mA with the option to change the device strength to 4mA, 8mA, 16mA or 20mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.



# LatticeXP2 External Switching Characteristics (Continued)

			-	7	-6		-5		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
		XP2-5	1.00		1.30	_	1.60		ns
	Clock to Data Hold - PIO Input	XP2-8	1.00	_	1.30	_	1.60	_	ns
t <sub>HE</sub>		XP2-17	1.00		1.30	_	1.60		ns
		XP2-30	1.20		1.60	_	1.90		ns
		XP2-40	1.20		1.60		1.90		ns
		XP2-5	1.00		1.30	_	1.60		ns
		XP2-8	1.00		1.30	_	1.60		ns
t <sub>SU_DELE</sub>	Clock to Data Setup - PIO Input Begister with Data Input Delay	XP2-17	1.00		1.30	_	1.60		ns
		XP2-30	1.20		1.60		1.90		ns
		XP2-40	1.20		1.60		1.90		ns
		XP2-5	0.00		0.00		0.00		ns
		XP2-8	0.00	—	0.00	—	0.00	—	ns
t <sub>H_DELE</sub>	Clock to Data Hold - PIO Input Begister with Input Data Delay	XP2-17	0.00	—	0.00	—	0.00	—	ns
		XP2-30	0.00		0.00		0.00		ns
		XP2-40	0.00		0.00		0.00		ns
f <sub>MAX_IOE</sub>	Clock Frequency of I/O and PFU Register	XP2	_	420	_	357	_	311	MHz
General I/O Pir	Parameters (using Primary Clo	ck with PLL	)1	1	1	1	1	1	
		XP2-5	—	3.00	—	3.30	—	3.70	ns
		XP2-8		3.00		3.30		3.70	ns
t <sub>COPLL</sub>	Clock to Output - PIO Output	XP2-17		3.00		3.30		3.70	ns
		XP2-30	_	3.00		3.30		3.70	ns
		XP2-40		3.00		3.30		3.70	ns
		XP2-5	1.00		1.20		1.40		ns
		XP2-8	1.00		1.20		1.40		ns
t <sub>SUPLL</sub>	Clock to Data Setup - PIO Input Register	XP2-17	1.00		1.20		1.40		ns
		XP2-30	1.00		1.20		1.40		ns
		XP2-40	1.00		1.20	_	1.40		ns
		XP2-5	0.90		1.10		1.30		ns
		XP2-8	0.90		1.10		1.30		ns
t <sub>HPLL</sub>	Clock to Data Hold - PIO Input	XP2-17	0.90		1.10		1.30		ns
		XP2-30	1.00	—	1.20	—	1.40	—	ns
		XP2-40	1.00	—	1.20	—	1.40	—	ns
		XP2-5	1.90	—	2.10	—	2.30	—	ns
		XP2-8	1.90		2.10	—	2.30	_	ns
t <sub>SU_DELPLL</sub>	Clock to Data Setup - PIO Input Begister with Data Input Delay	XP2-17	1.90	—	2.10	—	2.30	—	ns
	lingibion with Data input Delay	XP2-30	2.00	—	2.20	—	2.40	—	ns
		XP2-40	2.00	—	2.20	—	2.40	—	ns



# LatticeXP2 Internal Switching Characteristics<sup>1</sup> (Continued)

		-	7	-6		-5		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
t <sub>RST_PIO</sub>	Asynchronous reset time for PFU Logic	—	0.386	—	0.419	—	0.452	ns
t <sub>DEL</sub>	Dynamic Delay Step Size	0.035	0.035	0.035	0.035	0.035	0.035	ns
EBR Timing	· · · · · ·							
t <sub>CO_EBR</sub>	Clock (Read) to Output from Address or Data	_	2.774	_	3.142	_	3.510	ns
t <sub>COO_EBR</sub>	Clock (Write) to Output from EBR Output Register	_	0.360	_	0.408	—	0.456	ns
<sup>t</sup> SUDATA_EBR	Setup Data to EBR Memory (Write Clk)	-0.167	—	-0.198	_	-0.229	—	ns
t <sub>HDATA_EBR</sub>	Hold Data to EBR Memory (Write Clk)	0.194	—	0.231	_	0.267	_	ns
t <sub>SUADDR_EBR</sub>	Setup Address to EBR Memory (Write Clk)	-0.117	—	-0.137	_	-0.157	—	ns
t <sub>HADDR_EBR</sub>	Hold Address to EBR Memory (Write Clk)	0.157	_	0.182	_	0.207	_	ns
t <sub>SUWREN_EBR</sub>	Setup Write/Read Enable to EBR Memory (Write/Read Clk)	-0.135	_	-0.159	_	-0.182	_	ns
t <sub>HWREN_EBR</sub>	Hold Write/Read Enable to EBR Memory (Write/Read Clk)	0.158	_	0.186	_	0.214	_	ns
t <sub>SUCE_EBR</sub>	Clock Enable Setup Time to EBR Output Register (Read Clk)	0.144	—	0.160	_	0.176	_	ns
t <sub>HCE_EBR</sub>	Clock Enable Hold Time to EBR Output Register (Read Clk)	-0.097	—	-0.113	_	-0.129	_	ns
t <sub>RSTO_EBR</sub>	Reset To Output Delay Time from EBR Output Register (Asynchro- nous)	_	1.156	_	1.341	_	1.526	ns
t <sub>SUBE_EBR</sub>	Byte Enable Set-Up Time to EBR Output Register	-0.117	—	-0.137	_	-0.157	_	ns
t <sub>HBE_EBR</sub>	Byte Enable Hold Time to EBR Output Register Dynamic Delay on Each PIO	0.157	_	0.182	_	0.207	_	ns
t <sub>RSTREC_EBR</sub>	Asynchronous reset recovery time for EBR	0.233	—	0.291		0.347	—	ns
t <sub>RST_EBR</sub>	Asynchronous reset time for EBR	—	1.156	—	1.341	_	1.526	ns
PLL Paramete	ers							
t <sub>RSTKREC_PLL</sub>	After RSTK De-assert, Recovery Time Before Next Clock Edge Can Toggle K-divider Counter	1.000	_	1.000	_	1.000	_	ns
t <sub>RSTREC_PLL</sub>	After RST De-assert, Recovery Time Before Next Clock Edge Can Toggle M-divider Counter (Applies to M-Divider Portion of RST Only <sup>2</sup> )	1.000	_	1.000		1.000	_	ns
DSP Block Tir	ning							
t <sub>SUI_DSP</sub>	Input Register Setup Time	0.135		0.151		0.166		ns
t <sub>HI_DSP</sub>	Input Register Hold Time	0.021	—	-0.006	—	-0.031		ns
t <sub>SUP_DSP</sub>	Pipeline Register Setup Time	2.505	—	2.784	—	3.064	—	ns







Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.



# LatticeXP2 Family Timing Adders<sup>1, 2, 3, 4</sup>

Buffer Type	Description	-7	-6	-5	Units
Input Adjusters					
LVDS25	LVDS	-0.26	-0.11	0.04	ns
BLVDS25	BLVDS	-0.26	-0.11	0.04	ns
MLVDS	LVDS	-0.26	-0.11	0.04	ns
RSDS	RSDS	-0.26	-0.11	0.04	ns
LVPECL33	LVPECL	-0.26	-0.11	0.04	ns
HSTL18_I	HSTL_18 class I	-0.23	-0.08	0.07	ns
HSTL18_II	HSTL_18 class II	-0.23	-0.08	0.07	ns
HSTL18D_I	Differential HSTL 18 class I	-0.28	-0.13	0.02	ns
HSTL18D_II	Differential HSTL 18 class II	-0.28	-0.13	0.02	ns
HSTL15_I	HSTL_15 class I	-0.23	-0.09	0.06	ns
HSTL15D_I	Differential HSTL 15 class I	-0.28	-0.13	0.01	ns
SSTL33_I	SSTL_3 class I	-0.20	-0.04	0.12	ns
SSTL33_II	SSTL_3 class II	-0.20	-0.04	0.12	ns
SSTL33D_I	Differential SSTL_3 class I	-0.27	-0.11	0.04	ns
SSTL33D_II	Differential SSTL_3 class II	-0.27	-0.11	0.04	ns
SSTL25_I	SSTL_2 class I	-0.21	-0.06	0.10	ns
SSTL25_II	SSTL_2 class II	-0.21	-0.06	0.10	ns
SSTL25D_I	Differential SSTL_2 class I	-0.27	-0.12	0.03	ns
SSTL25D_II	Differential SSTL_2 class II	-0.27	-0.12	0.03	ns
SSTL18_I	SSTL_18 class I	-0.23	-0.08	0.07	ns
SSTL18_II	SSTL_18 class II	-0.23	-0.08	0.07	ns
SSTL18D_I	Differential SSTL_18 class I	-0.28	-0.13	0.02	ns
SSTL18D_II	Differential SSTL_18 class II	-0.28	-0.13	0.02	ns
LVTTL33	LVTTL	-0.09	0.05	0.18	ns
LVCMOS33	LVCMOS 3.3	-0.09	0.05	0.18	ns
LVCMOS25	LVCMOS 2.5	0.00	0.00	0.00	ns
LVCMOS18	LVCMOS 1.8	-0.23	-0.07	0.09	ns
LVCMOS15	LVCMOS 1.5	-0.20	-0.02	0.16	ns
LVCMOS12	LVCMOS 1.2	-0.35	-0.20	-0.04	ns
PCI33	3.3V PCI	-0.09	0.05	0.18	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E <sup>5</sup>	-0.25	0.02	0.30	ns
LVDS25	LVDS 2.5	-0.25	0.02	0.30	ns
BLVDS25	BLVDS 2.5	-0.28	0.00	0.28	ns
MLVDS	MLVDS 2.5 <sup>5</sup>	-0.28	0.00	0.28	ns
RSDS	RSDS 2.5⁵	-0.25	0.02	0.30	ns
LVPECL33	LVPECL 3.3 <sup>5</sup>	-0.37	-0.10	0.18	ns
HSTL18_I	HSTL_18 class I 8mA drive	-0.17	0.13	0.43	ns
HSTL18_II	HSTL_18 class II	-0.29	0.00	0.29	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	-0.17	0.13	0.43	ns
HSTL18D_II	Differential HSTL 18 class II	-0.29	0.00	0.29	ns



# LatticeXP2 Family Timing Adders<sup>1, 2, 3, 4</sup> (Continued)

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	0.32	0.69	1.06	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	0.32	0.69	1.06	ns
SSTL33_I	SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33_II	SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33D_II	Differential SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL18_I	SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
LVTTL33_4mA	LVTTL 4mA drive	-0.37	-0.05	0.26	ns
LVTTL33_8mA	LVTTL 8mA drive	-0.45	-0.18	0.10	ns
LVTTL33_12mA	LVTTL 12mA drive	-0.52	-0.24	0.04	ns
LVTTL33_16mA	LVTTL 16mA drive	-0.43	-0.14	0.14	ns
LVTTL33_20mA	LVTTL 20mA drive	-0.46	-0.18	0.09	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	-0.37	-0.05	0.26	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	-0.45	-0.18	0.10	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	-0.52	-0.24	0.04	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	-0.43	-0.14	0.14	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	-0.46	-0.18	0.09	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	-0.42	-0.15	0.13	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	-0.48	-0.21	0.05	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	-0.45	-0.18	0.08	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	-0.49	-0.22	0.04	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	-0.46	-0.18	0.10	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	-0.52	-0.25	0.02	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.56	-0.30	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	-0.50	-0.24	0.03	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate	-0.45	-0.17	0.11	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate	-0.53	-0.26	0.00	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate	-0.46	-0.19	0.08	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate	-0.55	-0.29	-0.02	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate	0.98	1.41	1.84	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate	0.74	1.16	1.58	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate	0.56	0.97	1.38	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate	0.77	1.19	1.61	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate	0.57	0.98	1.40	ns



# LatticeXP2 sysCONFIG Port Timing Specifications

Parameter	Description	Min	Max	Units
sysCONFIG PO	R, Initialization and Wake Up			
t <sub>ICFG</sub>	Minimum Vcc to INITN High	_	50	ms
t <sub>VMC</sub>	Time from t <sub>ICFG</sub> to valid Master CCLK	_	2	μs
t <sub>PRGMRJ</sub>	PROGRAMN Pin Pulse Rejection	_	12	ns
t <sub>PRGM</sub>	PROGRAMN Low Time to Start Configuration	50	—	ns
t <sub>DINIT</sub> 1	PROGRAMN High to INITN High Delay	_	1	ms
t <sub>DPPINIT</sub>	Delay Time from PROGRAMN Low to INITN Low	_	50	ns
t <sub>DPPDONE</sub>	Delay Time from PROGRAMN Low to DONE Low	_	50	ns
t <sub>IODISS</sub>	User I/O Disable from PROGRAMN Low	_	35	ns
t <sub>IOENSS</sub>	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	_	25	ns
t <sub>MWC</sub>	Additional Wake Master Clock Signals after DONE Pin High	0	—	Cycles
sysCONFIG SP	I Port (Master)			
t <sub>CFGX</sub>	INITN High to CCLK Low	_	1	μs
t <sub>CSSPI</sub>	INITN High to CSSPIN Low	_	2	μs
t <sub>CSCCLK</sub>	CCLK Low before CSSPIN Low	0	—	ns
t <sub>SOCDO</sub>	CCLK Low to Output Valid	_	15	ns
t <sub>CSPID</sub>	CSSPIN[0:1] Low to First CCLK Edge Setup Time	2cyc	600+6cyc	ns
f <sub>MAXSPI</sub>	Max CCLK Frequency	—	20	MHz
t <sub>SUSPI</sub>	SOSPI Data Setup Time Before CCLK	7	—	ns
t <sub>HSPI</sub>	SOSPI Data Hold Time After CCLK	10	—	ns
sysCONFIG SP	I Port (Slave)			
f <sub>MAXSPIS</sub>	Slave CCLK Frequency	—	25	MHz
t <sub>RF</sub>	Rise and Fall Time	50	—	mV/ns
t <sub>STCO</sub>	Falling Edge of CCLK to SOSPI Active	—	20	ns
t <sub>STOZ</sub>	Falling Edge of CCLK to SOSPI Disable	—	20	ns
t <sub>STSU</sub>	Data Setup Time (SISPI)	8	—	ns
t <sub>STH</sub>	Data Hold Time (SISPI)	10	—	ns
t <sub>sтскн</sub>	CCLK Clock Pulse Width, High	0.02	200	μs
t <sub>STCKL</sub>	CCLK Clock Pulse Width, Low	0.02	200	μs
t <sub>STVO</sub>	Falling Edge of CCLK to Valid SOSPI Output		20	ns
t <sub>SCS</sub>	CSSPISN High Time	25	—	ns
t <sub>SCSS</sub>	CSSPISN Setup Time	25	—	ns
t <sub>SCSH</sub>	CSSPISN Hold Time	25	—	ns

#### **Over Recommended Operating Conditions**

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of PROGRAMN.



# FlashBAK Time (from EBR to Flash)

## **Over Recommended Operating Conditions**

Device	EBR Density (Bits)	Time (Typ.)	Units
XP2-5	166K	1.5	S
XP2-8	221K	1.5	S
XP2-17	276K	1.5	S
XP2-30	387K	2.0	S
XP2-40	885K	3.0	S

# JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f <sub>MAX</sub>	TCK Clock Frequency	—	25	MHz
t <sub>BTCP</sub>	TCK [BSCAN] clock pulse width	40	—	ns
t <sub>BTCPH</sub>	TCK [BSCAN] clock pulse width high	20	—	ns
t <sub>BTCPL</sub>	TCK [BSCAN] clock pulse width low	20	—	ns
t <sub>BTS</sub>	TCK [BSCAN] setup time	8	—	ns
t <sub>BTH</sub>	TCK [BSCAN] hold time	10	—	ns
t <sub>BTRF</sub>	TCK [BSCAN] rise/fall time	50	—	mV/ns
t <sub>BTCO</sub>	TAP controller falling edge of clock to valid output	—	10	ns
t <sub>BTCODIS</sub>	TAP controller falling edge of clock to valid disable	—	10	ns
t <sub>BTCOEN</sub>	TAP controller falling edge of clock to valid enable	—	10	ns
t <sub>BTCRS</sub>	BSCAN test capture register setup time	8	—	ns
t <sub>BTCRH</sub>	BSCAN test capture register hold time	25	—	ns
t <sub>BUTCO</sub>	BSCAN test update register, falling edge of clock to valid output	—	25	ns
t <sub>BTUODIS</sub>	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
t <sub>BTUPOEN</sub>	BSCAN test update register, falling edge of clock to valid enable	_	25	ns



## **Switching Test Conditions**

Figure 3-11 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

## Figure 3-11. Output Test Load, LVTTL and LVCMOS Standards



\*CL Includes Test Fixture and Probe Capacitance

 Table 3-6. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R <sub>1</sub>	R <sub>2</sub>	CL	Timing Ref.	V <sub>T</sub>
				LVCMOS 3.3 = 1.5V	
		8	0pF	LVCMOS 2.5 = $V_{CCIO}/2$	
LVTTL and other LVCMOS settings (L -> H, H -> L)	$\infty$			LVCMOS 1.8 = V <sub>CCIO</sub> /2	
				LVCMOS 1.5 = $V_{CCIO}/2$	_
				LVCMOS 1.2 = V <sub>CCIO</sub> /2	_
LVCMOS 2.5 I/O (Z -> H)	8	1MΩ		V <sub>CCIO</sub> /2	
LVCMOS 2.5 I/O (Z -> L)	1MΩ	$\infty$		V <sub>CCIO</sub> /2	V <sub>CCIO</sub>
LVCMOS 2.5 I/O (H -> Z)	8	100		V <sub>OH</sub> - 0.10	
LVCMOS 2.5 I/O (L -> Z)	100	$\infty$		V <sub>OL</sub> + 0.10	V <sub>CCIO</sub>

Note: Output test conditions for all other interfaces are determined by the respective standards.



Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-30E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	30
LFXP2-30E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	30
LFXP2-30E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	30
LFXP2-30E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	30
LFXP2-30E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	30
LFXP2-30E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	30
LFXP2-30E-5FN672C	1.2V	-5	Lead-Free fpBGA	672	COM	30
LFXP2-30E-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	30
LFXP2-30E-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	30

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	40
LFXP2-40E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	40
LFXP2-40E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	40
LFXP2-40E-5FN672C	1.2V	-5	Lead-Free fpBGA	672	COM	40
LFXP2-40E-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	40
LFXP2-40E-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	40

## Industrial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5MN132I	1.2V	-5	Lead-Free csBGA	132	IND	5
LFXP2-5E-6MN132I	1.2V	-6	Lead-Free csBGA	132	IND	5
LFXP2-5E-5TN144I	1.2V	-5	Lead-Free TQFP	144	IND	5
LFXP2-5E-6TN144I	1.2V	-6	Lead-Free TQFP	144	IND	5
LFXP2-5E-5QN208I	1.2V	-5	Lead-Free PQFP	208	IND	5
LFXP2-5E-6QN208I	1.2V	-6	Lead-Free PQFP	208	IND	5
LFXP2-5E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	5
LFXP2-5E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5MN132I	1.2V	-5	Lead-Free csBGA	132	IND	8
LFXP2-8E-6MN132I	1.2V	-6	Lead-Free csBGA	132	IND	8
LFXP2-8E-5TN144I	1.2V	-5	Lead-Free TQFP	144	IND	8
LFXP2-8E-6TN144I	1.2V	-6	Lead-Free TQFP	144	IND	8
LFXP2-8E-5QN208I	1.2V	-5	Lead-Free PQFP	208	IND	8
LFXP2-8E-6QN208I	1.2V	-6	Lead-Free PQFP	208	IND	8
LFXP2-8E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	8
LFXP2-8E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	8



Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5F484I	1.2V	-5	fpBGA	484	IND	40
LFXP2-40E-6F484I	1.2V	-6	fpBGA	484	IND	40
LFXP2-40E-5F672I	1.2V	-5	fpBGA	672	IND	40
LFXP2-40E-6F672I	1.2V	-6	fpBGA	672	IND	40