



Welcome to [E-XFL.COM](https://www.e-xfl.com)

## Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

### Details

Product Status	Active
Number of LABs/CLBs	625
Number of Logic Elements/Cells	5000
Total RAM Bits	169984
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-5e-5tn144i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-5e-5tn144i</a>

## **Introduction**

LatticeXP2 devices combine a Look-up Table (LUT) based FPGA fabric with non-volatile Flash cells in an architecture referred to as flexiFLASH.

The flexiFLASH approach provides benefits including instant-on, infinite reconfigurability, on chip storage with FlashBAK embedded block memory and Serial TAG memory and design security. The parts also support Live Update technology with TransFR, 128-bit AES Encryption and Dual-boot technologies.

The LatticeXP2 FPGA fabric was optimized for the new technology from the outset with high performance and low cost in mind. LatticeXP2 devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support and enhanced sysDSP blocks.

Lattice Diamond<sup>®</sup> design software allows large and complex designs to be efficiently implemented using the LatticeXP2 family of FPGA devices. Synthesis library support for LatticeXP2 is available for popular logic synthesis tools. The Diamond software uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeXP2 device. The Diamond tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed Intellectual Property (IP) LatticeCORE™ modules for the LatticeXP2 family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

## Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

### Logic Mode

In this mode, the LUTs in each slice are configured as LUT4s. A LUT4 has 16 possible input combinations. Four-input logic functions are generated by programming the LUT4. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger LUTs such as LUT6, LUT7 and LUT8, can be constructed by concatenating two or more slices. Note that a LUT8 requires more than four slices.

### Ripple Mode

Ripple mode allows efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with async clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two carry signals, FCI and FCO, are generated per slice in this mode, allowing fast arithmetic functions to be constructed by concatenating slices.

### RAM Mode

In this mode, a 16x4-bit distributed Single Port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit Pseudo Dual Port RAM (PDPR) memory is created by using one slice as the read-write port and the other companion slice as the read-only port.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information on using RAM in LatticeXP2 devices, please see TN1137, [LatticeXP2 Memory Usage Guide](#).

**Table 2-3. Number of Slices Required For Implementing Distributed RAM**

	<b>SPR 16X4</b>	<b>PDPR 16X4</b>
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

### ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in the ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

**Figure 2-4. General Purpose PLL (GPLL) Diagram**

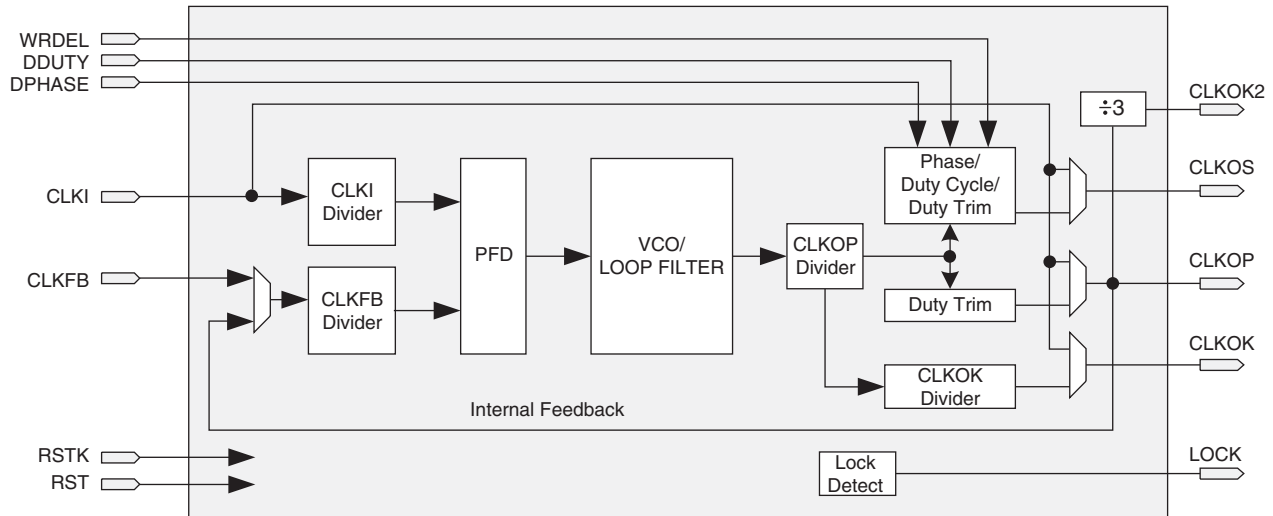


Table 2-4 provides a description of the signals in the GPLL blocks.

**Table 2-4. GPLL Block Signal Descriptions**

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
DPHASE [3:0]	I	DPA Phase Adjust input
DDUTY [3:0]	I	DPA Duty Cycle Select input
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
CLKOK2	O	PLL output to clock tree (CLKOP divided by 3)
LOCK	O	"1" indicates PLL LOCK to CLKI

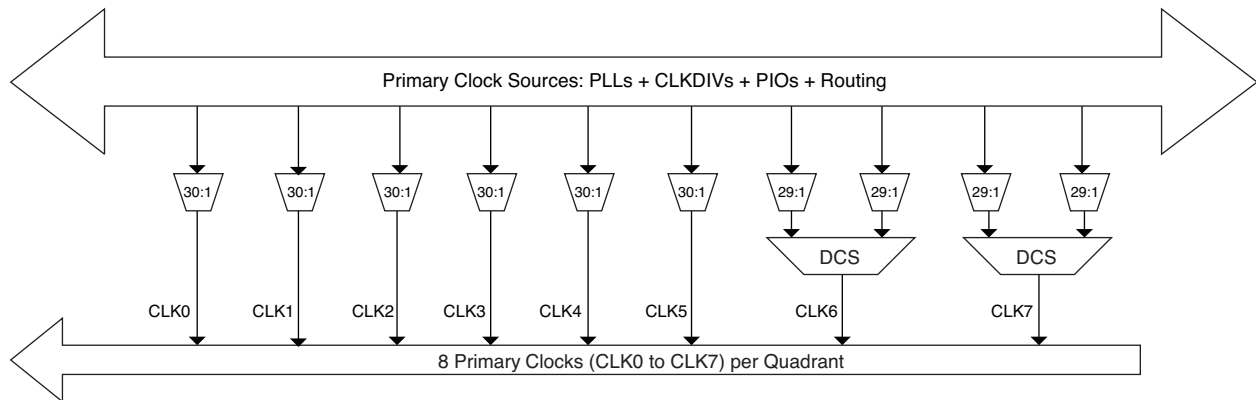
## Clock Dividers

LatticeXP2 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a  $\div 2$ ,  $\div 4$  or  $\div 8$  mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from the CLKOP output from the GPLLs or from the Edge Clocks (ECLK). The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets the input and forces all outputs to low. The RELEASE signal releases outputs to the input clock. For further information on clock dividers, please see TN1126, [LatticeXP2 sysCLOCK PLL Design and Usage Guide](#). Figure 2-5 shows the clock divider connections.

## Primary Clock Routing

The clock routing structure in LatticeXP2 devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-9 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally.

**Figure 2-9. Per Quadrant Primary Clock Selection**

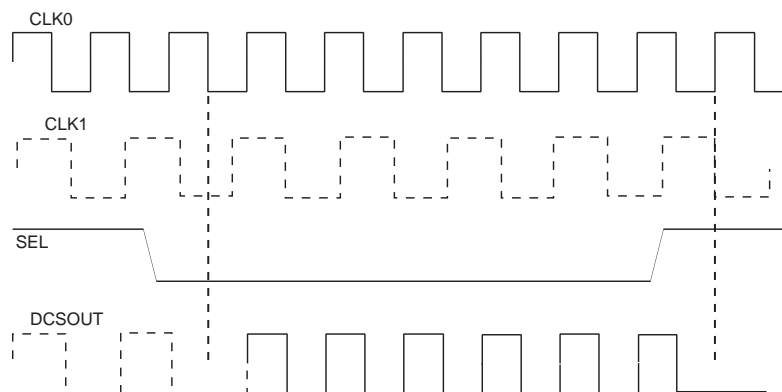


## Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved irrespective of when the select signal is toggled. There are two DCS blocks per quadrant; in total, eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-9).

Figure 2-10 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, please see TN1126, [LatticeXP2 sysCLOCK PLL Design and Usage Guide](#).

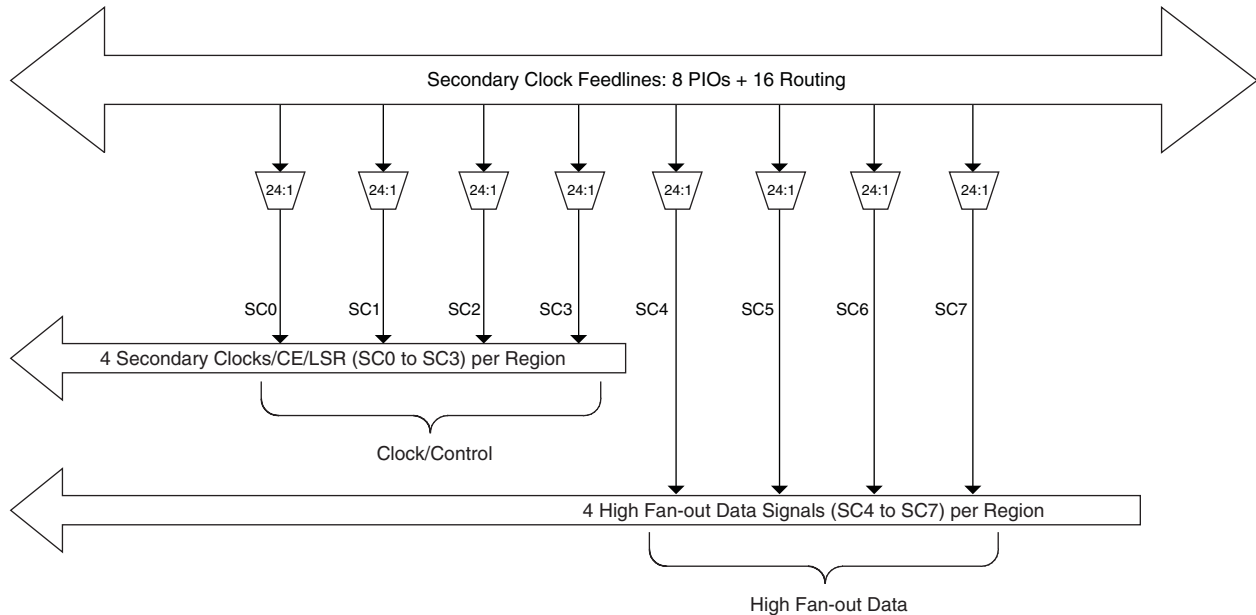
**Figure 2-10. DCS Waveforms**



## Secondary Clock/Control Routing

Secondary clocks in the LatticeXP2 devices are region-based resources. The benefit of region-based resources is the relatively low injection delay and skew within the region, as compared to primary clocks. EBR rows, DSP rows and a special vertical routing channel bound the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP block in the DSP row or the center of the DSP row. Figure 2-11 shows this special vertical routing channel and the eight secondary clock regions for the LatticeXP2-40.

**Figure 2-12. Secondary Clock Selection**

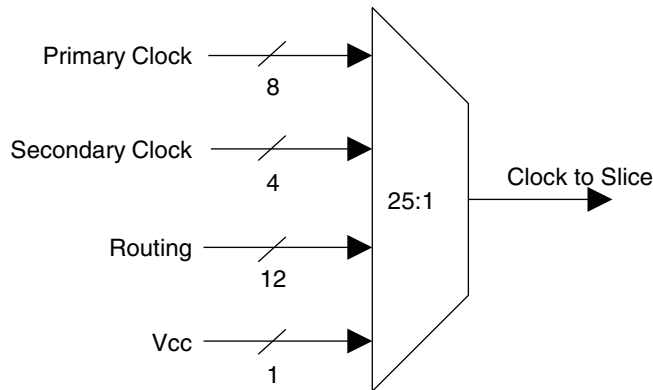


**Slice Clock Selection**

Figure 2-13 shows the clock selections and Figure 2-14 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals, via routing, can be used as clock inputs to the slices. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control, then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

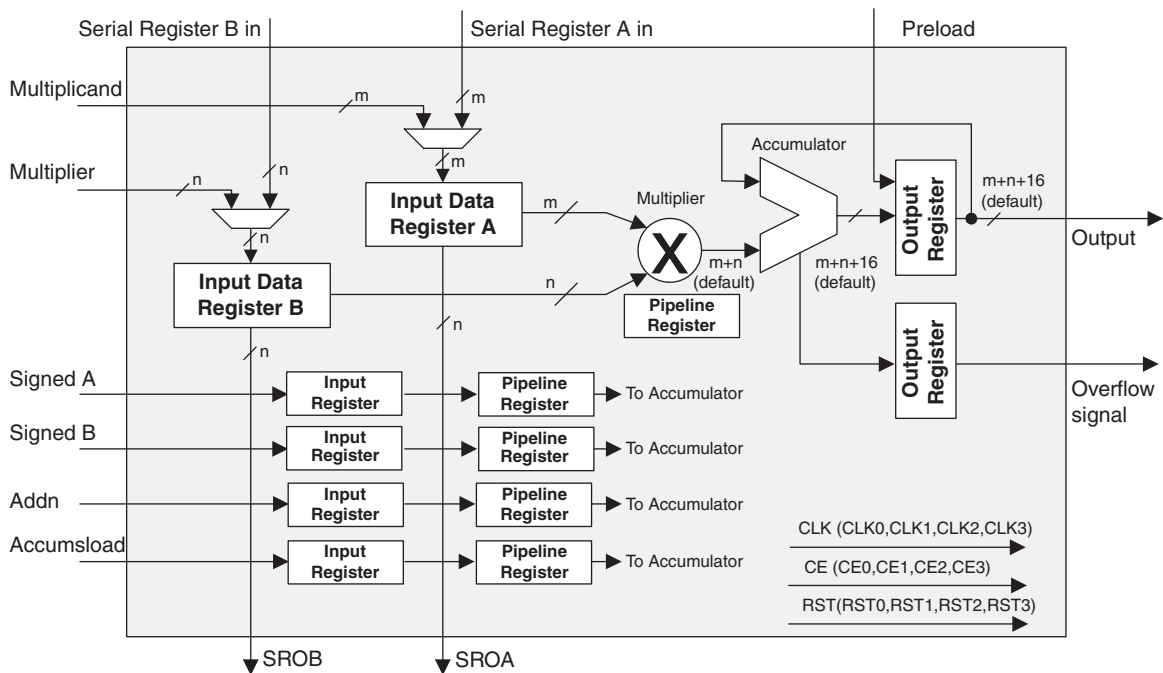
**Figure 2-13. Slice0 through Slice2 Clock Selection**



### MAC sysDSP Element

In this case, the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers but the output register is always enabled. The output register is used to store the accumulated value. The Accumulators in the DSP blocks in LatticeXP2 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-21 shows the MAC sysDSP element.

**Figure 2-21. MAC sysDSP**



**Table 2-11. PIO Signal List**

Name	Type	Description
CE	Control from the core	Clock enables for input and output block flip-flops
CLK	Control from the core	System clocks for input and output blocks
ECLK1, ECLK2	Control from the core	Fast edge clocks
LSR	Control from the core	Local Set/Reset
GSRN	Control from routing	Global Set/Reset (active low)
INCK <sup>2</sup>	Input to the core	Input to Primary Clock Network or PLL reference inputs
DQS	Input to PIO	DQS signal from logic (routing) to PIO
INDD	Input to the core	Unregistered data input to core
INFF	Input to the core	Registered input on positive edge of the clock (CLK0)
IPOS0, IPOS1	Input to the core	Double data rate registered inputs to the core
QPOS0 <sup>1</sup> , QPOS1 <sup>1</sup>	Input to the core	Gearbox pipelined inputs to the core
QNEG0 <sup>1</sup> , QNEG1 <sup>1</sup>	Input to the core	Gearbox pipelined inputs to the core
OPOS0, ONEG0, OPOS2, ONEG2	Output data from the core	Output signals from the core for SDR and DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation
DEL[3:0]	Control from the core	Dynamic input delay control bits
TD	Tristate control from the core	Tristate signal from the core used in SDR operation
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block
DQSXFER	Control from core	Controls signal to the Output block

1. Signals available on left/right/bottom only.

2. Selected I/O.

## PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with necessary clock and selection logic.

### Input Register Block

The input register blocks for PIOs contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-26 shows the diagram of the input register block.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the Single Data Rate (SDR) mode, the data is registered, by one of the registers in the SDR Sync register block, with the system clock. In DDR mode two registers are used to sample the data on the positive and negative edges of the DQS signal which creates two data streams, D0 and D2. D0 and D2 are synchronized with the system clock before entering the core. Further information on this topic can be found in the DDR Memory Support section of this data sheet.

By combining input blocks of the complementary PIOs and sharing registers from output blocks, a gearbox function can be implemented, that takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-26 shows the diagram using this gearbox function. For more information on this topic, please see TN1138, [LatticeXP2 High Speed I/O Interface](#).



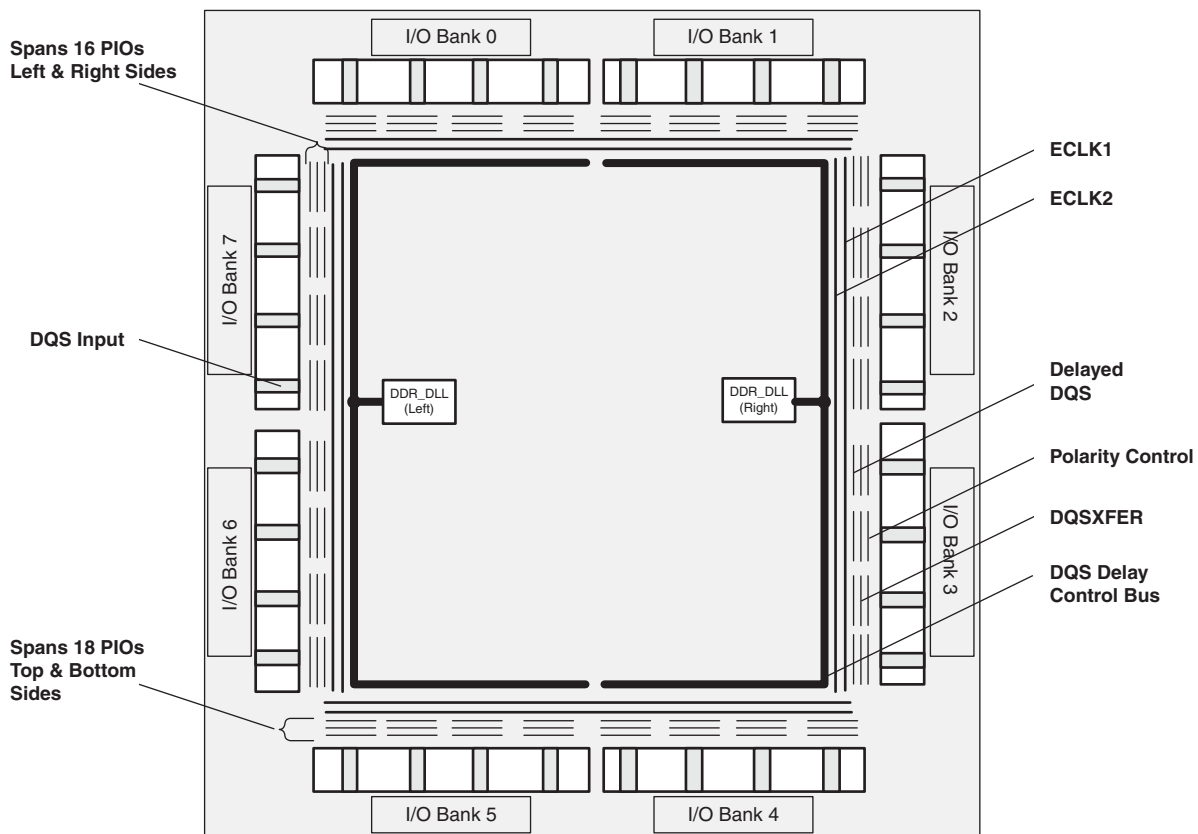
### DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock, referred to as DQS, is not free-running, and this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only, as shown in Figure 2-30) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figure 2-30 and Figure 2-31 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of 6-bit bus calibration signals from two dedicated DLLs (DDR\_DLL) on opposite sides of the device. Each DLL compensates DQS delays in its half of the device as shown in Figure 2-30. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

**Figure 2-30. Edge Clock, DLL Calibration and DQS Local Bus Distribution**



## DQSXFER

LatticeXP2 devices provide a DQSXFER signal to the output buffer to assist it in data transfer to DDR memories that require DQS strobe be shifted 90°. This shifted DQS strobe is generated by the DQSDEL block. The DQSXFER signal runs the span of the data bus.

## sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

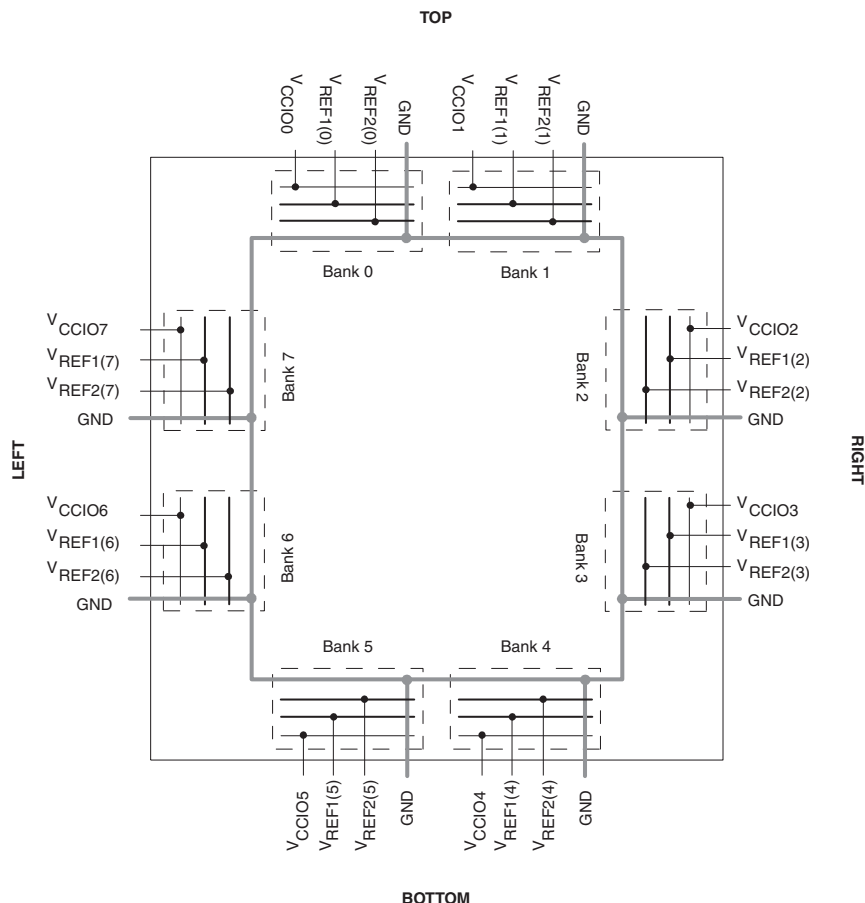
## sysIO Buffer Banks

LatticeXP2 devices have eight sysIO buffer banks for user I/Os arranged two per side. Each bank is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage ( $V_{CCIO}$ ). In addition, each bank has voltage references,  $V_{REF1}$  and  $V_{REF2}$ , that allow it to be completely independent from the others. Figure 2-32 shows the eight banks and their associated supplies.

In LatticeXP2 devices, single-ended output buffers and ratioed input buffers (LVTTTL, LVCMOS and PCI) are powered using  $V_{CCIO}$ . LVTTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of  $V_{CCIO}$ .

Each bank can support up to two separate  $V_{REF}$  voltages,  $V_{REF1}$  and  $V_{REF2}$ , that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

**Figure 2-32. LatticeXP2 Banks**



## sysIO Single-Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}^1$ (mA)	$I_{OH}^1$ (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)	Max. (V)	Min. (V)		
LVCMOS33	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVTTTL33	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS25	-0.3	0.7	1.7	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS18	-0.3	$0.35 V_{CCIO}$	$0.65 V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	16, 12, 8, 4	-16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS15	-0.3	$0.35 V_{CCIO}$	$0.65 V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	8, 4	-8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS12	-0.3	$0.35 V_{CC}$	$0.65 V_{CC}$	3.6	0.4	$V_{CCIO} - 0.4$	6, 2	-6, -2
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
PCI33	-0.3	$0.3 V_{CCIO}$	$0.5 V_{CCIO}$	3.6	$0.1 V_{CCIO}$	$0.9 V_{CCIO}$	1.5	-0.5
SSTL33_I	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.7	$V_{CCIO} - 1.1$	8	-8
SSTL33_II	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCIO} - 0.9$	16	-16
SSTL25_I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCIO} - 0.62$	7.6	-7.6
							12	-12
SSTL25_II	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.35	$V_{CCIO} - 0.43$	15.2	-15.2
							20	-20
SSTL18_I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	0.4	$V_{CCIO} - 0.4$	6.7	-6.7
SSTL18_II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	0.28	$V_{CCIO} - 0.28$	8	-8
							11	-11
HSTL15_I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
							8	-8
HSTL18_I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	8	-8
							12	-12
HSTL18_II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	16	-16

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed  $n * 8\text{mA}$ , where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

### BLVDS

The LatticeXP2 devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

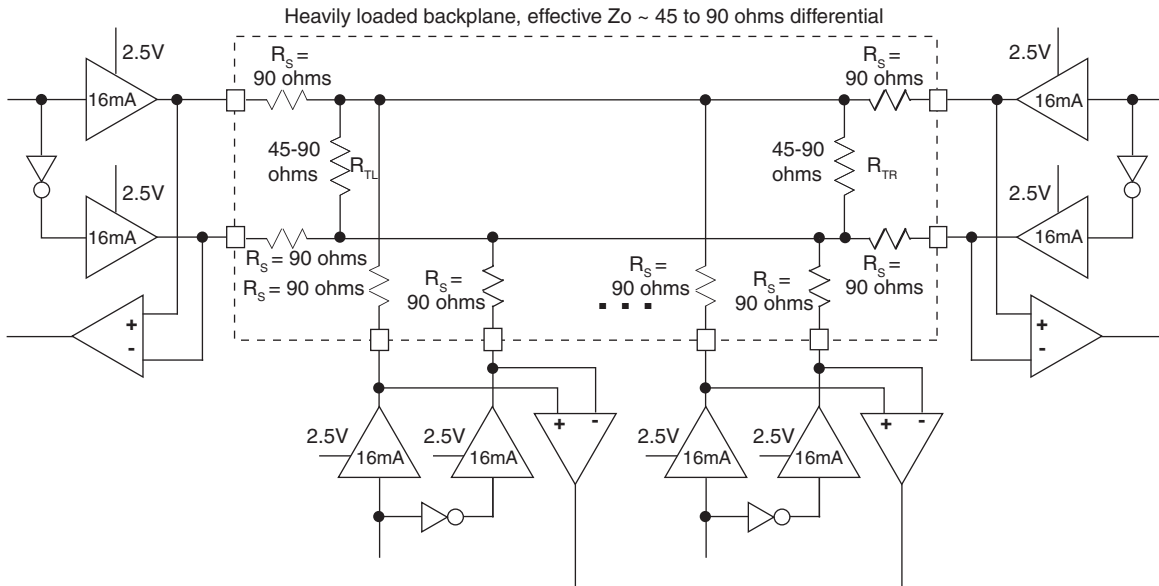


Table 3-2. BLVDS DC Conditions<sup>1</sup>

#### Over Recommended Operating Conditions

Parameter	Description	Typical		Units
		Zo = 45Ω	Zo = 90Ω	
V <sub>CCIO</sub>	Output Driver Supply (+/- 5%)	2.50	2.50	V
Z <sub>OUT</sub>	Driver Impedance	10.00	10.00	Ω
R <sub>S</sub>	Driver Series Resistor (+/- 1%)	90.00	90.00	Ω
R <sub>TL</sub>	Driver Parallel Resistor (+/- 1%)	45.00	90.00	Ω
R <sub>TR</sub>	Receiver Termination (+/- 1%)	45.00	90.00	Ω
V <sub>OH</sub>	Output High Voltage (After R <sub>TL</sub> )	1.38	1.48	V
V <sub>OL</sub>	Output Low Voltage (After R <sub>TL</sub> )	1.12	1.02	V
V <sub>OD</sub>	Output Differential Voltage (After R <sub>TL</sub> )	0.25	0.46	V
V <sub>CM</sub>	Output Common Mode Voltage	1.25	1.25	V
I <sub>DC</sub>	DC Output Current	11.24	10.20	mA

1. For input buffer, see LVDS table.

### LVPECL

The LatticeXP2 devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

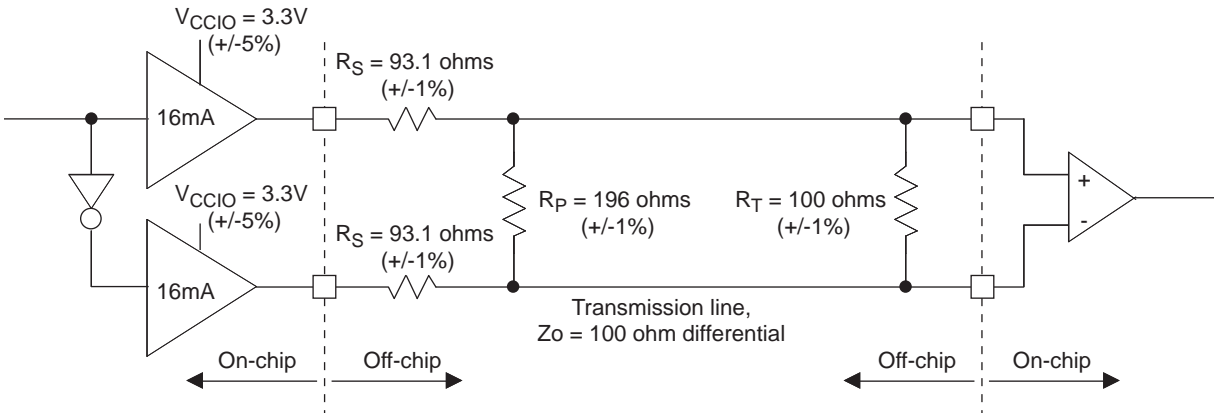


Table 3-3. LVPECL DC Conditions<sup>1</sup>

#### Over Recommended Operating Conditions

Parameter	Description	Typical	Units
$V_{CCIO}$	Output Driver Supply (+/-5%)	3.30	V
$Z_{OUT}$	Driver Impedance	10	$\Omega$
$R_S$	Driver Series Resistor (+/-1%)	93	$\Omega$
$R_P$	Driver Parallel Resistor (+/-1%)	196	$\Omega$
$R_T$	Receiver Termination (+/-1%)	100	$\Omega$
$V_{OH}$	Output High Voltage (After $R_P$ )	2.05	V
$V_{OL}$	Output Low Voltage (After $R_P$ )	1.25	V
$V_{OD}$	Output Differential Voltage (After $R_P$ )	0.80	V
$V_{CM}$	Output Common Mode Voltage	1.65	V
$Z_{BACK}$	Back Impedance	100.5	$\Omega$
$I_{DC}$	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

## RSDS

The LatticeXP2 devices support differential RSDS standard. This standard is emulated using complementary LVC-MOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

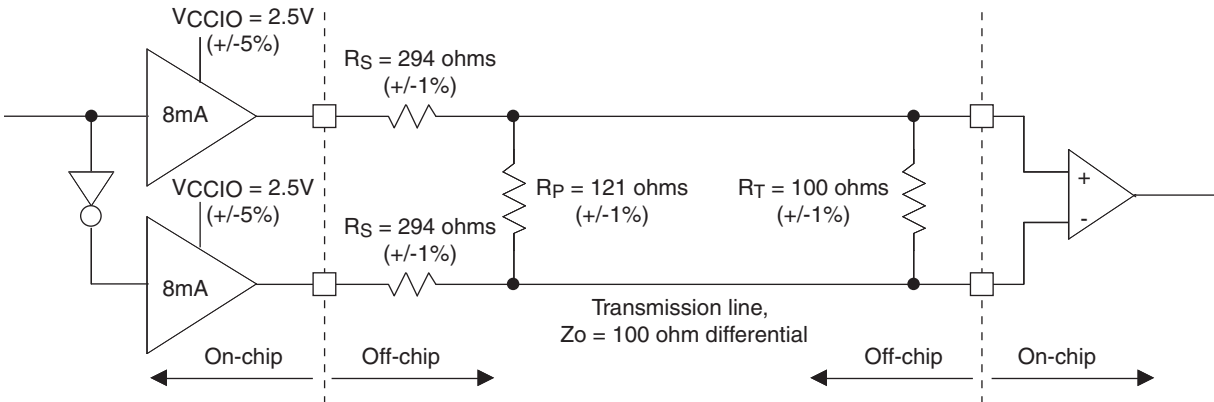


Table 3-4. RSDS DC Conditions<sup>1</sup>

### Over Recommended Operating Conditions

Parameter	Description	Typical	Units
$V_{CCIO}$	Output Driver Supply ( $\pm 5\%$ )	2.50	V
$Z_{OUT}$	Driver Impedance	20	$\Omega$
$R_S$	Driver Series Resistor ( $\pm 1\%$ )	294	$\Omega$
$R_P$	Driver Parallel Resistor ( $\pm 1\%$ )	121	$\Omega$
$R_T$	Receiver Termination ( $\pm 1\%$ )	100	$\Omega$
$V_{OH}$	Output High Voltage (After $R_P$ )	1.35	V
$V_{OL}$	Output Low Voltage (After $R_P$ )	1.15	V
$V_{OD}$	Output Differential Voltage (After $R_P$ )	0.20	V
$V_{CM}$	Output Common Mode Voltage	1.25	V
$Z_{BACK}$	Back Impedance	101.5	$\Omega$
$I_{DC}$	DC Output Current	3.66	mA

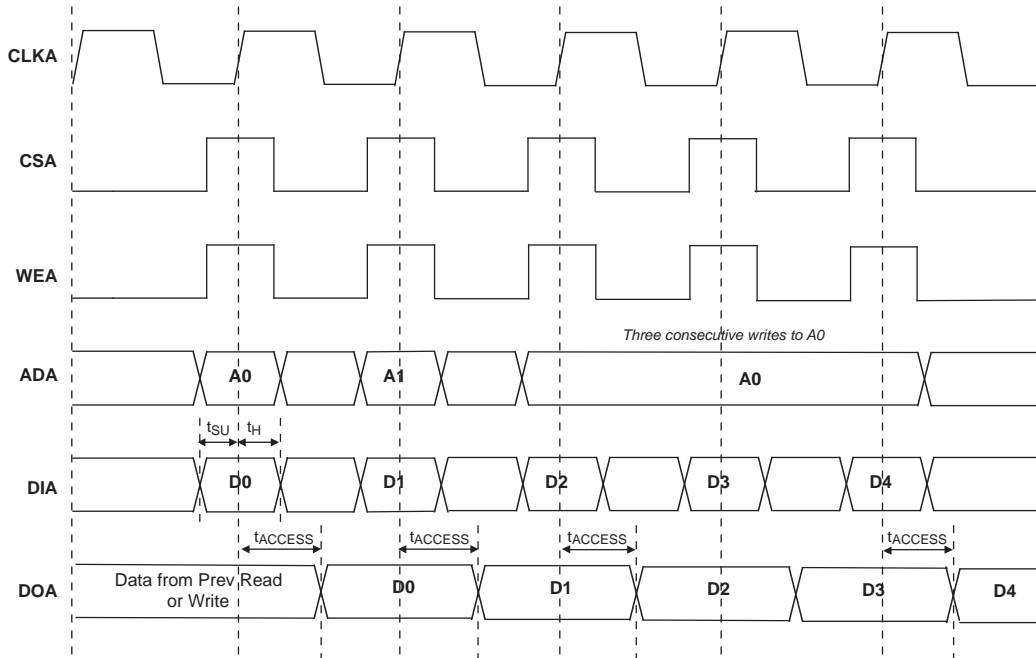
1. For input buffer, see LVDS table.

## LatticeXP2 Internal Switching Characteristics<sup>1</sup>

Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>PFU/PFF Logic Mode Timing</b>								
t <sub>LUT4_PFU</sub>	LUT4 delay (A to D inputs to F output)	—	0.216	—	0.238	—	0.260	ns
t <sub>LUT6_PFU</sub>	LUT6 delay (A to D inputs to OFX output)	—	0.304	—	0.399	—	0.494	ns
t <sub>LSR_PFU</sub>	Set/Reset to output of PFU (Asynchronous)	—	0.720	—	0.769	—	0.818	ns
t <sub>SUM_PFU</sub>	Clock to Mux (M0,M1) Input Setup Time	0.154	—	0.151	—	0.148	—	ns
t <sub>HM_PFU</sub>	Clock to Mux (M0,M1) Input Hold Time	-0.061	—	-0.057	—	-0.053	—	ns
t <sub>SUD_PFU</sub>	Clock to D input setup time	0.061	—	0.077	—	0.093	—	ns
t <sub>HD_PFU</sub>	Clock to D input hold time	0.002	—	0.003	—	0.003	—	ns
t <sub>CK2Q_PFU</sub>	Clock to Q delay, (D-type Register Configuration)	—	0.342	—	0.363	—	0.383	ns
t <sub>RSTREC_PFU</sub>	Asynchronous reset recovery time for PFU Logic	—	0.520	—	0.634	—	0.748	ns
t <sub>RST_PFU</sub>	Asynchronous reset time for PFU Logic	—	0.720	—	0.769	—	0.818	ns
<b>PFU Dual Port Memory Mode Timing</b>								
t <sub>CORAM_PFU</sub>	Clock to Output (F Port)	—	1.082	—	1.267	—	1.452	ns
t <sub>SUDATA_PFU</sub>	Data Setup Time	-0.206	—	-0.240	—	-0.274	—	ns
t <sub>HDATA_PFU</sub>	Data Hold Time	0.239	—	0.275	—	0.312	—	ns
t <sub>SUADDR_PFU</sub>	Address Setup Time	-0.294	—	-0.333	—	-0.371	—	ns
t <sub>HADDR_PFU</sub>	Address Hold Time	0.295	—	0.333	—	0.371	—	ns
t <sub>SUWREN_PFU</sub>	Write/Read Enable Setup Time	-0.146	—	-0.169	—	-0.193	—	ns
t <sub>HWREN_PFU</sub>	Write/Read Enable Hold Time	0.158	—	0.182	—	0.207	—	ns
<b>PIO Input/Output Buffer Timing</b>								
t <sub>IN_PIO</sub>	Input Buffer Delay (LVCMOS25)	—	0.858	—	0.766	—	0.674	ns
t <sub>OUT_PIO</sub>	Output Buffer Delay (LVCMOS25)	—	1.561	—	1.403	—	1.246	ns
<b>IOLOGIC Input/Output Timing</b>								
t <sub>SUI_PIO</sub>	Input Register Setup Time (Data Before Clock)	0.583	—	0.893	—	1.201	—	ns
t <sub>HI_PIO</sub>	Input Register Hold Time (Data after Clock)	0.062	—	0.322	—	0.482	—	ns
t <sub>COO_PIO</sub>	Output Register Clock to Output Delay	—	0.608	—	0.661	—	0.715	ns
t <sub>SUCE_PIO</sub>	Input Register Clock Enable Setup Time	0.032	—	0.037	—	0.041	—	ns
t <sub>HCE_PIO</sub>	Input Register Clock Enable Hold Time	-0.022	—	-0.025	—	-0.028	—	ns
t <sub>SULSR_PIO</sub>	Set/Reset Setup Time	0.184	—	0.201	—	0.217	—	ns
t <sub>HLSR_PIO</sub>	Set/Reset Hold Time	-0.080	—	-0.086	—	-0.093	—	ns
t <sub>RSTREC_PIO</sub>	Asynchronous reset recovery time for IO Logic	0.228	—	0.247	—	0.266	—	ns

Figure 3-8. Write Through (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.



**LatticeXP2 Family Timing Adders<sup>1, 2, 3, 4</sup> (Continued)**

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	0.32	0.69	1.06	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	0.32	0.69	1.06	ns
SSTL33_I	SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33_II	SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33D_II	Differential SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL18_I	SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
LVTTTL33_4mA	LVTTTL 4mA drive	-0.37	-0.05	0.26	ns
LVTTTL33_8mA	LVTTTL 8mA drive	-0.45	-0.18	0.10	ns
LVTTTL33_12mA	LVTTTL 12mA drive	-0.52	-0.24	0.04	ns
LVTTTL33_16mA	LVTTTL 16mA drive	-0.43	-0.14	0.14	ns
LVTTTL33_20mA	LVTTTL 20mA drive	-0.46	-0.18	0.09	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	-0.37	-0.05	0.26	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	-0.45	-0.18	0.10	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	-0.52	-0.24	0.04	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	-0.43	-0.14	0.14	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	-0.46	-0.18	0.09	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	-0.42	-0.15	0.13	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	-0.48	-0.21	0.05	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	-0.45	-0.18	0.08	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	-0.49	-0.22	0.04	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	-0.46	-0.18	0.10	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	-0.52	-0.25	0.02	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.56	-0.30	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	-0.50	-0.24	0.03	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate	-0.45	-0.17	0.11	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate	-0.53	-0.26	0.00	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate	-0.46	-0.19	0.08	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate	-0.55	-0.29	-0.02	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate	0.98	1.41	1.84	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate	0.74	1.16	1.58	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate	0.56	0.97	1.38	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate	0.77	1.19	1.61	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate	0.57	0.98	1.40	ns

**LatticeXP2 Family Timing Adders<sup>1, 2, 3, 4</sup> (Continued)**
**Over Recommended Operating Conditions**

Buffer Type	Description	-7	-6	-5	Units
LVC MOS25_4mA	LVC MOS 2.5 4mA drive, slow slew rate	1.05	1.43	1.81	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive, slow slew rate	0.78	1.15	1.52	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive, slow slew rate	0.59	0.96	1.33	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive, slow slew rate	0.81	1.18	1.55	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive, slow slew rate	0.61	0.98	1.35	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive, slow slew rate	1.01	1.38	1.75	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive, slow slew rate	0.72	1.08	1.45	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive, slow slew rate	0.53	0.90	1.26	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive, slow slew rate	0.74	1.11	1.48	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive, slow slew rate	0.96	1.33	1.71	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive, slow slew rate	-0.53	-0.26	0.00	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive, slow slew rate	0.90	1.27	1.65	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive, slow slew rate	-0.55	-0.29	-0.02	ns
PCI33	3.3V PCI	-0.29	-0.01	0.26	ns

1. Timing Adders are characterized but not tested on every device.
2. LVC MOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. The base parameters used with these timing adders to calculate timing are listed in the LatticeXP2 Internal Switching Characteristics table under PIO Input/Output Timing.
5. These timing adders are measured with the recommended resistor values.

### Signal Descriptions

Signal Name	I/O	Description
<b>General Purpose</b>		
P[Edge] [Row/Column Number*]_[A/B]	I/O	<p>[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).</p> <p>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.</p> <p>[A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.</p>
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
GND	—	Ground. Dedicated pins.
V <sub>CC</sub>	—	Power supply pins for core logic. Dedicated pins.
V <sub>CCAUX</sub>	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers.
V <sub>CCPLL</sub>	—	PLL supply pins. csBGA, PQFP and TQFP packages only.
V <sub>CCIOx</sub>	—	Dedicated power supply pins for I/O bank x.
V <sub>REF1_x</sub> , V <sub>REF2_x</sub>	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V <sub>REF</sub> inputs. When not used, they may be used as I/O pins.
<b>PLL and Clock Functions</b> (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_V <sub>CCPLL</sub>	—	Power supply pin for PLL: LLC, LRC, URC, ULC, num = row from center.
[LOC][num]_GPLL[T, C]_IN_A	I	General Purpose PLL (GPLL) input pads: LLC, LRC, URC, ULC, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_GPLL[T, C]_FB_A	I	Optional feedback GPLL input pads: LLC, LRC, URC, ULC, num = row from center, T = true and C = complement, index A,B,C...at each side.
PCLK[T, C]_[n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank.
[LOC]DQS[num]	I	DQS input pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = ball function number. Any pad can be configured to be output.
<b>Test and Programming (Dedicated Pins)</b>		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.

## Signal Descriptions (Cont.)

Signal Name	I/O	Description
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
<b>Configuration Pads (Used during sysCONFIG)</b>		
CFG[1:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, an internal pull-up is enabled.
INITN <sup>1</sup>	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
SISPI <sup>2</sup>	I/O	Input data pin in slave SPI mode and Output data pin in Master SPI mode.
SOSPI <sup>2</sup>	I/O	Output data pin in slave SPI mode and Input data pin in Master SPI mode.
CSSPIN <sup>2</sup>	O	Chip select for external SPI Flash memory in Master SPI mode. This pin has a weak internal pull-up.
CSSPISN	I	Chip select in Slave SPI mode. This pin has a weak internal pull-up.
TOE	I	Test Output Enable tristates all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to V <sub>CC</sub> is recommended.

1. If not actively driven, the internal pull-up may not be sufficient. An external pull-up resistor of 4.7k to 10k $\Omega$  is recommended.
2. When using the device in Master SPI mode, it must be mutually exclusive from JTAG operations (i.e. TCK tied to GND) or the JTAG TCK must be free-running when used in a system JTAG test environment. If Master SPI mode is used in conjunction with a JTAG download cable, the device power cycle is required after the cable is unplugged.

**Conventional Packaging**
**Commercial**

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5M132C	1.2V	-5	csBGA	132	COM	5
LFXP2-5E-6M132C	1.2V	-6	csBGA	132	COM	5
LFXP2-5E-7M132C	1.2V	-7	csBGA	132	COM	5
LFXP2-5E-5FT256C	1.2V	-5	ftBGA	256	COM	5
LFXP2-5E-6FT256C	1.2V	-6	ftBGA	256	COM	5
LFXP2-5E-7FT256C	1.2V	-7	ftBGA	256	COM	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5M132C	1.2V	-5	csBGA	132	COM	8
LFXP2-8E-6M132C	1.2V	-6	csBGA	132	COM	8
LFXP2-8E-7M132C	1.2V	-7	csBGA	132	COM	8
LFXP2-8E-5FT256C	1.2V	-5	ftBGA	256	COM	8
LFXP2-8E-6FT256C	1.2V	-6	ftBGA	256	COM	8
LFXP2-8E-7FT256C	1.2V	-7	ftBGA	256	COM	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5FT256C	1.2V	-5	ftBGA	256	COM	17
LFXP2-17E-6FT256C	1.2V	-6	ftBGA	256	COM	17
LFXP2-17E-7FT256C	1.2V	-7	ftBGA	256	COM	17
LFXP2-17E-5F484C	1.2V	-5	fpBGA	484	COM	17
LFXP2-17E-6F484C	1.2V	-6	fpBGA	484	COM	17
LFXP2-17E-7F484C	1.2V	-7	fpBGA	484	COM	17

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-30E-5FT256C	1.2V	-5	ftBGA	256	COM	30
LFXP2-30E-6FT256C	1.2V	-6	ftBGA	256	COM	30
LFXP2-30E-7FT256C	1.2V	-7	ftBGA	256	COM	30
LFXP2-30E-5F484C	1.2V	-5	fpBGA	484	COM	30
LFXP2-30E-6F484C	1.2V	-6	fpBGA	484	COM	30
LFXP2-30E-7F484C	1.2V	-7	fpBGA	484	COM	30
LFXP2-30E-5F672C	1.2V	-5	fpBGA	672	COM	30
LFXP2-30E-6F672C	1.2V	-6	fpBGA	672	COM	30
LFXP2-30E-7F672C	1.2V	-7	fpBGA	672	COM	30