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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	625
Number of Logic Elements/Cells	5000
Total RAM Bits	169984
Number of I/O	86
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	132-LFBGA, CSPBGA
Supplier Device Package	132-CSBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfxp2-5e-6mn132c

Routing

There are many resources provided in the LatticeXP2 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) or x6 (spans seven PFU) connections. The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered to allow both short and long connections routing between PFUs.

The LatticeXP2 family has an enhanced routing architecture to produce a compact design. The Diamond design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Phase Locked Loops (PLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The LatticeXP2 family supports between two and four full featured General Purpose PLLs (GPLL). The architecture of the GPLL is shown in Figure 2-4.

CLKI, the PLL reference frequency, is provided either from the pin or from routing; it feeds into the Input Clock Divider block. CLKFB, the feedback signal, is generated from CLKOP (the primary clock output) or from a user clock pin/logic. CLKFB feeds into the Feedback Divider and is used to multiply the reference frequency.

Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. The phase and frequency of the VCO are determined from the input path and feedback signals. A LOCK signal is generated by the VCO to indicate that the VCO is locked with the input clock signal.

The output of the VCO feeds into the CLKOP Divider, a post-scalar divider. The duty cycle of the CLKOP Divider output can be fine tuned using the Duty Trim block, which creates the CLKOP signal. By allowing the VCO to operate at higher frequencies than CLKOP, the frequency range of the GPLL is expanded. The output of the CLKOP Divider is passed through the CLKOK Divider, a secondary clock divider, to generate lower frequencies for the CLKOK output. For applications that require even lower frequencies, the CLKOP signal is passed through a divide-by-three divider to produce the CLKOK2 output. The CLKOK2 output is provided for applications that use source synchronous logic. The Phase/Duty Cycle/Duty Trim block is used to adjust the phase and duty cycle of the CLKOP Divider output to generate the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The clock outputs from the GPLL; CLKOP, CLKOK, CLKOK2 and CLKOS, are fed to the clock distribution network.

For further information on the GPLL please see TN1126, [LatticeXP2 sysCLOCK PLL Design and Usage Guide](#).

Secondary Clock/Control Sources

LatticeXP2 devices derive secondary clocks (SC0 through SC7) from eight dedicated clock input pads and the rest from routing. Figure 2-7 shows the secondary clock sources.

Figure 2-7. Secondary Clock Sources

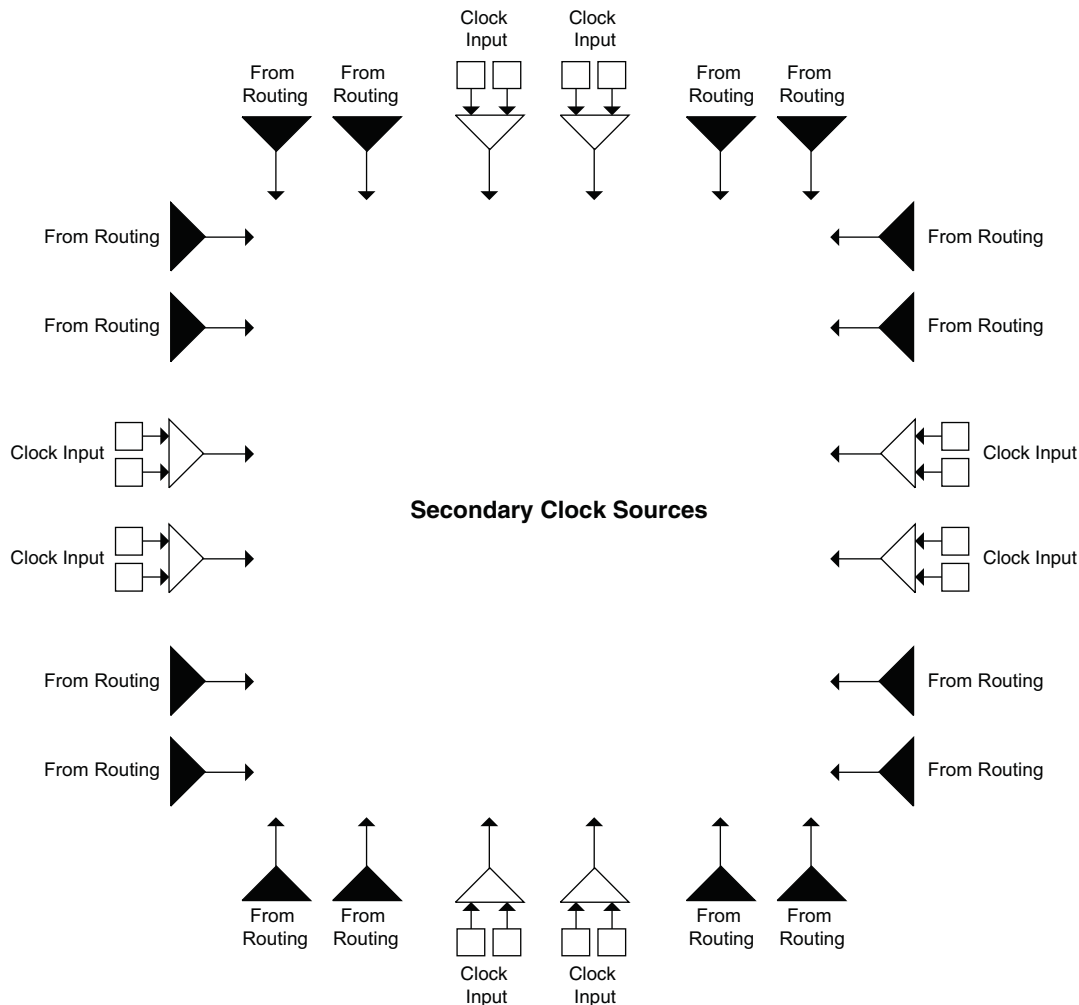
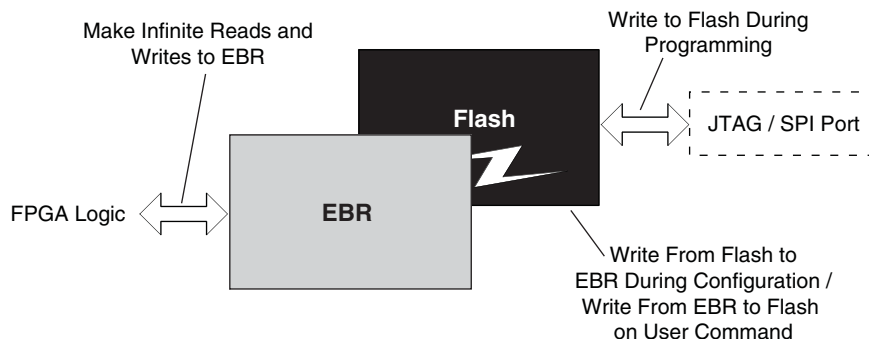


Figure 2-16. FlashBAK Technology



Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

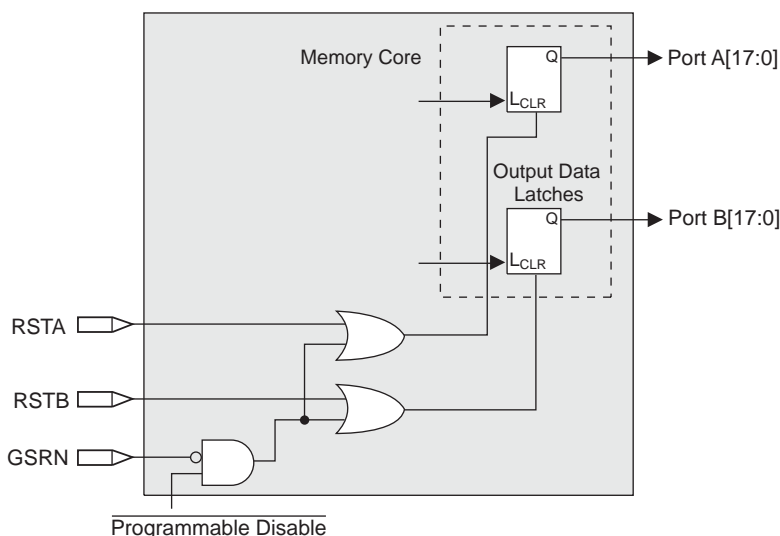
EBR memory supports two forms of write behavior for single port or dual port operation:

1. Normal – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. Write Through – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. GSRN, the global reset signal, resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-17.

Figure 2-17. Memory Core Reset



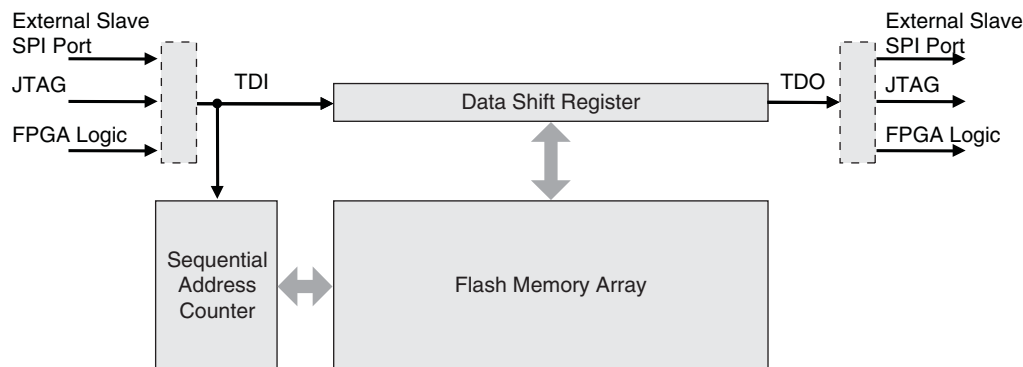
1. Unlocked
2. Key Locked – Presenting the key through the programming interface allows the device to be unlocked.
3. Permanently Locked – The device is permanently locked.

To further complement the security of the device a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash portion of the device.

Serial TAG Memory

LatticeXP2 devices offer 0.6 to 3.3kbits of Flash memory in the form of Serial TAG memory. The TAG memory is an area of the on-chip Flash that can be used for non-volatile storage including electronic ID codes, version codes, date stamps, asset IDs and calibration settings. A block diagram of the TAG memory is shown in Figure 2-34. The TAG memory is accessed in the same way as external SPI Flash and it can be read or programmed either through JTAG, an external Slave SPI Port, or directly from FPGA logic. To read the TAG memory, a start address is specified and the entire TAG memory contents are read sequentially in a first-in-first-out manner. The TAG memory is independent of the Flash used for device configuration and given its use for general-purpose storage functions is always accessible regardless of the device security settings. For more information, see TN1137, [LatticeXP2 Memory Usage Guide](#) and TN1141, [LatticeXP2 sysCONFIG Usage Guide](#).

Figure 2-34. Serial TAG Memory Diagram



Live Update Technology

Many applications require field updates of the FPGA. LatticeXP2 devices provide three features that enable this configuration to be done in a secure and failsafe manner while minimizing impact on system operation.

1. **Decryption Support**
LatticeXP2 devices provide on-chip, non-volatile key storage to support decryption of a 128-bit AES encrypted bitstream, securing designs and deterring design piracy.
2. **TransFR (Transparent Field Reconfiguration)**
TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. For more information please see TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#).
3. **Dual Boot Image Support**
Dual boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeXP2 can be re-booted from this new configuration file. If there is a problem such as corrupt data during download or incorrect version number with this new boot image, the LatticeXP2 device can revert back to the

original backup configuration and try again. This all can be done without power cycling the system. For more information please see TN1220, [LatticeXP2 Dual Boot Feature](#).

For more information on device configuration, please see TN1141, [LatticeXP2 sysCONFIG Usage Guide](#).

Soft Error Detect (SED) Support

LatticeXP2 devices have dedicated logic to perform Cyclic Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, LatticeXP2 devices can be programmed for checking soft errors in SRAM. SED can be run on a programmed device when the user logic is not active. In the event a soft error occurs, the device can be programmed to either reload from a known good boot image (from internal Flash or external SPI memory) or generate an error signal.

For further information on SED support, please see TN1130, [LatticeXP2 Soft Error Detection \(SED\) Usage Guide](#).

On-Chip Oscillator

Every LatticeXP2 device has an internal CMOS oscillator that is used to derive a Master Clock (CCLK) for configuration. The oscillator and CCLK run continuously and are available to user logic after configuration is complete. The available CCLK frequencies are listed in Table 2-14. When a different CCLK frequency is selected during the design process, the following sequence takes place:

1. Device powers up with the default CCLK frequency.
2. During configuration, users select a different CCLK frequency.
3. CCLK frequency changes to the selected frequency after clock configuration bits are received.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1141, [LatticeXP2 sysCONFIG Usage Guide](#).

Table 2-14. Selectable CCLKs and Oscillator Frequencies During Configuration and User Mode

CCLK/Oscillator (MHz)
2.5 ¹
3.1 ²
4.3
5.4
6.9
8.1
9.2
10
13
15
20
26
32
40
54
80 ³
163 ³

1. Software default oscillator frequency.
2. Software default CCLK frequency.
3. Frequency not valid for CCLK.

Density Shifting

The LatticeXP2 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Hot Socketing Specifications^{1, 2, 3, 4}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq V_{IH} \text{ (MAX.)}$	—	—	+/-1	mA

1. Insensitive to sequence of V_{CC} , V_{CCAUX} and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} , V_{CCAUX} and V_{CCIO} .
2. $0 \leq V_{CC} \leq V_{CC} \text{ (MAX)}$, $0 \leq V_{CCIO} \leq V_{CCIO} \text{ (MAX)}$ or $0 \leq V_{CCAUX} \leq V_{CCAUX} \text{ (MAX)}$.
3. I_{DK} is additive to I_{PU} , I_{PW} or I_{BH} .
4. LVCMOS and LVTTL only.

ESD Performance

Please refer to the [LatticeXP2 Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL} , I_{IH} ¹	Input or I/O Low Leakage	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	10	μA
		$V_{CCIO} \leq V_{IN} \leq V_{IH} \text{ (MAX)}$	—	—	150	μA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCIO}$	-30	—	-150	μA
I_{PD}	I/O Active Pull-down Current	$V_{IL} \text{ (MAX)} \leq V_{IN} \leq V_{CCIO}$	30	—	210	μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} \text{ (MAX)}$	30	—	—	μA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCIO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	210	μA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	-150	μA
V_{BHT}	Bus Hold Trip Points		$V_{IL} \text{ (MAX)}$	—	$V_{IH} \text{ (MIN)}$	V
C1	I/O Capacitance ²	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V$, $V_{CC} = 1.2V$, $V_{IO} = 0$ to $V_{IH} \text{ (MAX)}$	—	8	—	pf
C2	Dedicated Input Capacitance	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V$, $V_{CC} = 1.2V$, $V_{IO} = 0$ to $V_{IH} \text{ (MAX)}$	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, $f = 1.0$ MHz.

Initialization Supply Current^{1, 2, 3, 4, 5}

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical (25°C, Max. Supply) ⁶	Units
I_{CC}	Core Power Supply Current	XP2-5	20	mA
		XP2-8	21	mA
		XP2-17	44	mA
		XP2-30	58	mA
		XP2-40	62	mA
I_{CCAUX}	Auxiliary Power Supply Current ⁷	XP2-5	67	mA
		XP2-8	74	mA
		XP2-17	112	mA
		XP2-30	124	mA
		XP2-40	130	mA
I_{CCPLL}	PLL Power Supply Current (per PLL)		1.8	mA
I_{CCIO}	Bank Power Supply Current (per Bank)		6.4	mA
I_{CCJ}	VCCJ Power Supply Current		1.2	mA

1. For further information on supply current, please see TN1139, [Power Estimation and Management for LatticeXP2 Devices](#).

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

3. Frequency 0 MHz.

4. Does not include additional current from bypass or decoupling capacitor across the supply.

5. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.

6. $T_J = 25^\circ\text{C}$, power supplies at nominal voltage.

7. In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL} . For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.

sysIO Recommended Operating Conditions

Over Recommended Operating Conditions

Standard	V _{CCIO}			V _{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS33 ²	3.135	3.3	3.465	—	—	—
LVC MOS25 ²	2.375	2.5	2.625	—	—	—
LVC MOS18	1.71	1.8	1.89	—	—	—
LVC MOS15	1.425	1.5	1.575	—	—	—
LVC MOS12 ²	1.14	1.2	1.26	—	—	—
LV TTL33 ²	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
SSTL18_I ² , SSTL18_II ²	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I ² , SSTL25_II ²	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I ² , SSTL33_II ²	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I ²	1.425	1.5	1.575	0.68	0.75	0.9
HSTL18_I ² , HSTL18_II ²	1.71	1.8	1.89	0.816	0.9	1.08
LVDS25 ²	2.375	2.5	2.625	—	—	—
MLVDS25 ¹	2.375	2.5	2.625	—	—	—
LVPECL33 ^{1, 2}	3.135	3.3	3.465	—	—	—
BLVDS25 ^{1, 2}	2.375	2.5	2.625	—	—	—
RSDS ^{1, 2}	2.375	2.5	2.625	—	—	—
SSTL18D_I ² , SSTL18D_II ²	1.71	1.8	1.89	—	—	—
SSTL25D_I ² , SSTL25D_II ²	2.375	2.5	2.625	—	—	—
SSTL33D_I ² , SSTL33D_II ²	3.135	3.3	3.465	—	—	—
HSTL15D_I ²	1.425	1.5	1.575	—	—	—
HSTL18D_I ² , HSTL18D_II ²	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.

2. Input on this standard does not depend on the value of V_{CCIO}.

sysIO Single-Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}^1 (mA)	I_{OH}^1 (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)	Max. (V)	Min. (V)		
LVCMOS33	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVTTTL33	-0.3	0.8	2.0	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS25	-0.3	0.7	1.7	3.6	0.4	$V_{CCIO} - 0.4$	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS18	-0.3	$0.35 V_{CCIO}$	$0.65 V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	16, 12, 8, 4	-16, -12, -8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS15	-0.3	$0.35 V_{CCIO}$	$0.65 V_{CCIO}$	3.6	0.4	$V_{CCIO} - 0.4$	8, 4	-8, -4
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVCMOS12	-0.3	$0.35 V_{CC}$	$0.65 V_{CC}$	3.6	0.4	$V_{CCIO} - 0.4$	6, 2	-6, -2
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
PCI33	-0.3	$0.3 V_{CCIO}$	$0.5 V_{CCIO}$	3.6	$0.1 V_{CCIO}$	$0.9 V_{CCIO}$	1.5	-0.5
SSTL33_I	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.7	$V_{CCIO} - 1.1$	8	-8
SSTL33_II	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCIO} - 0.9$	16	-16
SSTL25_I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCIO} - 0.62$	7.6	-7.6
							12	-12
SSTL25_II	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.35	$V_{CCIO} - 0.43$	15.2	-15.2
							20	-20
SSTL18_I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	0.4	$V_{CCIO} - 0.4$	6.7	-6.7
SSTL18_II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	3.6	0.28	$V_{CCIO} - 0.28$	8	-8
							11	-11
HSTL15_I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	4	-4
							8	-8
HSTL18_I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	8	-8
							12	-12
HSTL18_II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCIO} - 0.4$	16	-16

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed $n * 8\text{mA}$, where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

MLVDS

The LatticeXP2 devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.

Figure 3-5. MLVDS (Reduced Swing Differential Standard)

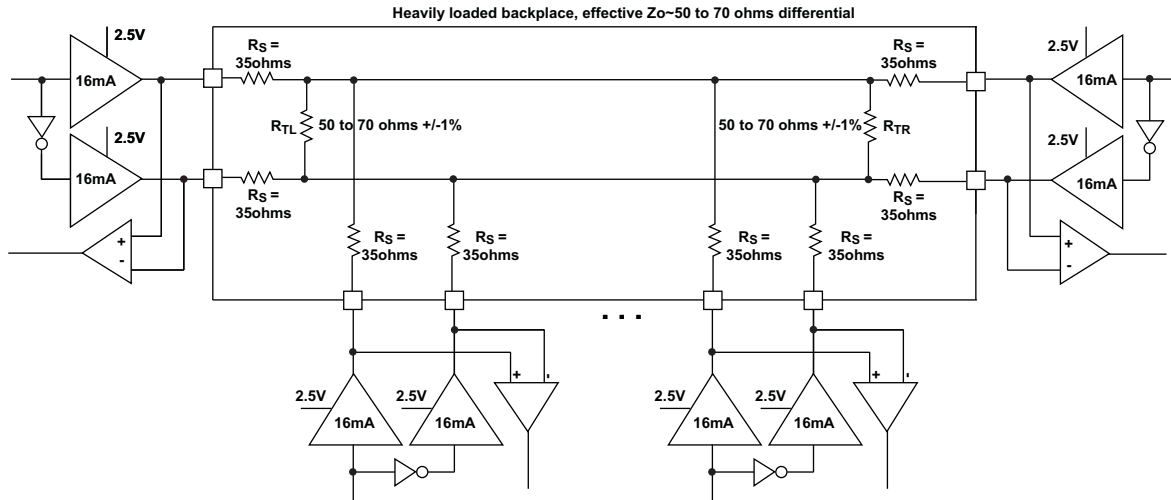


Table 3-5. MLVDS DC Conditions¹

Parameter	Description	Typical		Units
		$Z_o=50\Omega$	$Z_o=70\Omega$	
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (+/-1%)	35.00	35.00	Ω
R_{TL}	Driver Parallel Resistor (+/-1%)	50.00	70.00	Ω
R_{TR}	Receiver Termination (+/-1%)	50.00	70.00	Ω
V_{OH}	Output High Voltage (After R_{TL})	1.52	1.60	V
V_{OL}	Output Low Voltage (After R_{TL})	0.98	0.90	V
V_{OD}	Output Differential Voltage (After R_{TL})	0.54	0.70	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see details of additional technical information at the end of this data sheet.

LatticeXP2 Family Timing Adders^{1, 2, 3, 4}

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
Input Adjusters					
LVDS25	LVDS	-0.26	-0.11	0.04	ns
BLVDS25	BLVDS	-0.26	-0.11	0.04	ns
MLVDS	LVDS	-0.26	-0.11	0.04	ns
RSDS	RSDS	-0.26	-0.11	0.04	ns
LVPECL33	LVPECL	-0.26	-0.11	0.04	ns
HSTL18_I	HSTL_18 class I	-0.23	-0.08	0.07	ns
HSTL18_II	HSTL_18 class II	-0.23	-0.08	0.07	ns
HSTL18D_I	Differential HSTL 18 class I	-0.28	-0.13	0.02	ns
HSTL18D_II	Differential HSTL 18 class II	-0.28	-0.13	0.02	ns
HSTL15_I	HSTL_15 class I	-0.23	-0.09	0.06	ns
HSTL15D_I	Differential HSTL 15 class I	-0.28	-0.13	0.01	ns
SSTL33_I	SSTL_3 class I	-0.20	-0.04	0.12	ns
SSTL33_II	SSTL_3 class II	-0.20	-0.04	0.12	ns
SSTL33D_I	Differential SSTL_3 class I	-0.27	-0.11	0.04	ns
SSTL33D_II	Differential SSTL_3 class II	-0.27	-0.11	0.04	ns
SSTL25_I	SSTL_2 class I	-0.21	-0.06	0.10	ns
SSTL25_II	SSTL_2 class II	-0.21	-0.06	0.10	ns
SSTL25D_I	Differential SSTL_2 class I	-0.27	-0.12	0.03	ns
SSTL25D_II	Differential SSTL_2 class II	-0.27	-0.12	0.03	ns
SSTL18_I	SSTL_18 class I	-0.23	-0.08	0.07	ns
SSTL18_II	SSTL_18 class II	-0.23	-0.08	0.07	ns
SSTL18D_I	Differential SSTL_18 class I	-0.28	-0.13	0.02	ns
SSTL18D_II	Differential SSTL_18 class II	-0.28	-0.13	0.02	ns
LVTTTL33	LVTTTL	-0.09	0.05	0.18	ns
LVCMOS33	LVCMOS 3.3	-0.09	0.05	0.18	ns
LVCMOS25	LVCMOS 2.5	0.00	0.00	0.00	ns
LVCMOS18	LVCMOS 1.8	-0.23	-0.07	0.09	ns
LVCMOS15	LVCMOS 1.5	-0.20	-0.02	0.16	ns
LVCMOS12	LVCMOS 1.2	-0.35	-0.20	-0.04	ns
PCI33	3.3V PCI	-0.09	0.05	0.18	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E ⁵	-0.25	0.02	0.30	ns
LVDS25	LVDS 2.5	-0.25	0.02	0.30	ns
BLVDS25	BLVDS 2.5	-0.28	0.00	0.28	ns
MLVDS	MLVDS 2.5 ⁵	-0.28	0.00	0.28	ns
RSDS	RSDS 2.5 ⁵	-0.25	0.02	0.30	ns
LVPECL33	LVPECL 3.3 ⁵	-0.37	-0.10	0.18	ns
HSTL18_I	HSTL_18 class I 8mA drive	-0.17	0.13	0.43	ns
HSTL18_II	HSTL_18 class II	-0.29	0.00	0.29	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	-0.17	0.13	0.43	ns
HSTL18D_II	Differential HSTL 18 class II	-0.29	0.00	0.29	ns

LatticeXP2 Family Timing Adders^{1, 2, 3, 4} (Continued)
Over Recommended Operating Conditions

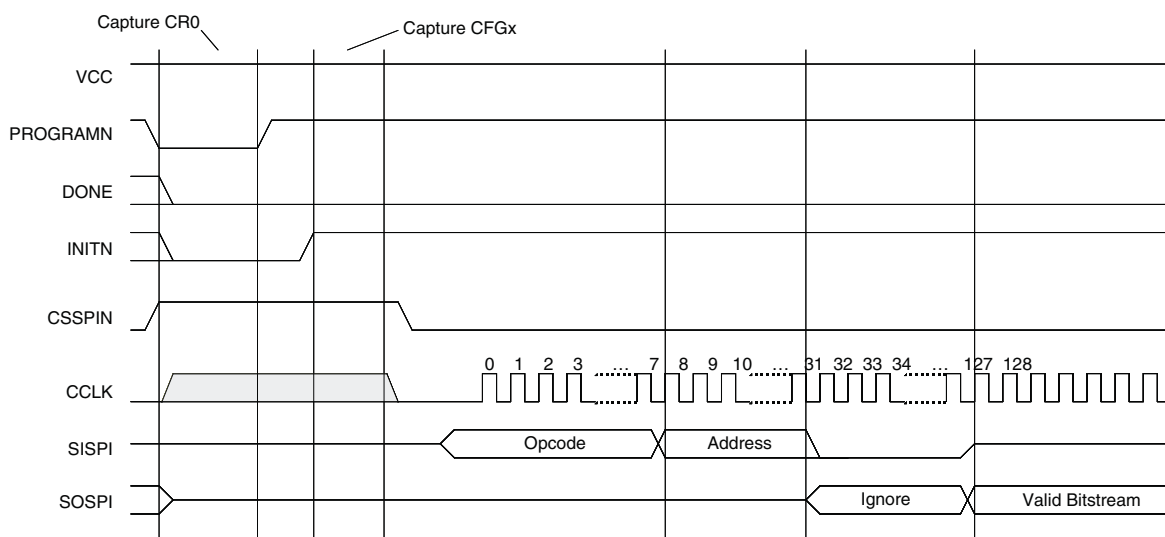
Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	0.32	0.69	1.06	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	0.32	0.69	1.06	ns
SSTL33_I	SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33_II	SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.25	0.05	0.35	ns
SSTL33D_II	Differential SSTL_3 class II	-0.31	-0.02	0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.25	0.02	0.30	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.28	0.00	0.28	ns
SSTL18_I	SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.17	0.13	0.43	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.18	0.12	0.42	ns
LVTTTL33_4mA	LVTTTL 4mA drive	-0.37	-0.05	0.26	ns
LVTTTL33_8mA	LVTTTL 8mA drive	-0.45	-0.18	0.10	ns
LVTTTL33_12mA	LVTTTL 12mA drive	-0.52	-0.24	0.04	ns
LVTTTL33_16mA	LVTTTL 16mA drive	-0.43	-0.14	0.14	ns
LVTTTL33_20mA	LVTTTL 20mA drive	-0.46	-0.18	0.09	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	-0.37	-0.05	0.26	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	-0.45	-0.18	0.10	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	-0.52	-0.24	0.04	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	-0.43	-0.14	0.14	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	-0.46	-0.18	0.09	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	-0.42	-0.15	0.13	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	-0.48	-0.21	0.05	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	-0.45	-0.18	0.08	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	-0.49	-0.22	0.04	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	-0.46	-0.18	0.10	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	-0.52	-0.25	0.02	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.56	-0.30	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	-0.50	-0.24	0.03	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate	-0.45	-0.17	0.11	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate	-0.53	-0.26	0.00	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate	-0.46	-0.19	0.08	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate	-0.55	-0.29	-0.02	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate	0.98	1.41	1.84	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate	0.74	1.16	1.58	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate	0.56	0.97	1.38	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate	0.77	1.19	1.61	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate	0.57	0.98	1.40	ns

On-Chip Oscillator and Configuration Master Clock Characteristics

Over Recommended Operating Conditions

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value -30%	Selected value +30%	MHz
Duty Cycle	40	60	%

Figure 3-9. Master SPI Configuration Waveforms



FlashBAK Time (from EBR to Flash)

Over Recommended Operating Conditions

Device	EBR Density (Bits)	Time (Typ.)	Units
XP2-5	166K	1.5	s
XP2-8	221K	1.5	s
XP2-17	276K	1.5	s
XP2-30	387K	2.0	s
XP2-40	885K	3.0	s

JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK Clock Frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
For Top and Bottom Edges of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
P[Edge] [n+4]	A	DQ
	B	DQ

Notes:

1. "n" is a row PIC number.
2. The DDR interface is designed for memories that support one DQS strobe up to 16 bits of data for the left and right edges and up to 18 bits of data for the top and bottom edges. In some packages, all the potential DDR data (DQ) pins may not be available. PIC numbering definitions are provided in the "Signal Names" column of the Signal Descriptions table.

Pin Information Summary (Cont.)

Pin Type		XP2-5				XP2-8				XP2-17			XP2-30			XP2-40	
		132 csBGA	144 TQFP	208 PQFP	256 ftBGA	132 csBGA	144 TQFP	208 PQFP	256 ftBGA	208 PQFP	256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
PCI capable I/Os Bonding Out per Bank	Bank0	18	20	20	26	18	20	20	28	20	28	52	28	52	70	52	70
	Bank1	4	6	18	18	4	6	18	22	18	22	36	22	36	54	36	70
	Bank2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank4	8	8	18	18	8	8	18	26	18	26	36	26	38	54	38	70
	Bank5	14	18	20	24	14	18	20	24	20	24	52	24	53	70	53	70
	Bank6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

Logic Signal Connections

Package pinout information can be found under “Data Sheets” on the LatticeXP2 product page of the Lattice website www.latticesemi.com/products/fpga/xp2 and in the Lattice Diamond design software.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Lattice [Thermal Management](#) document to find the device/package specific thermal values.

For Further Information

- TN1139, [Power Estimation and Management for LatticeXP2 Devices](#)
- Power Calculator tool is included with the Lattice Diamond design tool or as a standalone download from www.latticesemi.com/products/designsoftware

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-30E-5FTN256C	1.2V	-5	Lead-Free ftBGA	256	COM	30
LFXP2-30E-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	30
LFXP2-30E-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	30
LFXP2-30E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	30
LFXP2-30E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	30
LFXP2-30E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	30
LFXP2-30E-5FN672C	1.2V	-5	Lead-Free fpBGA	672	COM	30
LFXP2-30E-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	30
LFXP2-30E-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	30

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5FN484C	1.2V	-5	Lead-Free fpBGA	484	COM	40
LFXP2-40E-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	40
LFXP2-40E-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	40
LFXP2-40E-5FN672C	1.2V	-5	Lead-Free fpBGA	672	COM	40
LFXP2-40E-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	40
LFXP2-40E-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	40

Industrial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5MN132I	1.2V	-5	Lead-Free csBGA	132	IND	5
LFXP2-5E-6MN132I	1.2V	-6	Lead-Free csBGA	132	IND	5
LFXP2-5E-5TN144I	1.2V	-5	Lead-Free TQFP	144	IND	5
LFXP2-5E-6TN144I	1.2V	-6	Lead-Free TQFP	144	IND	5
LFXP2-5E-5QN208I	1.2V	-5	Lead-Free PQFP	208	IND	5
LFXP2-5E-6QN208I	1.2V	-6	Lead-Free PQFP	208	IND	5
LFXP2-5E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	5
LFXP2-5E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5MN132I	1.2V	-5	Lead-Free csBGA	132	IND	8
LFXP2-8E-6MN132I	1.2V	-6	Lead-Free csBGA	132	IND	8
LFXP2-8E-5TN144I	1.2V	-5	Lead-Free TQFP	144	IND	8
LFXP2-8E-6TN144I	1.2V	-6	Lead-Free TQFP	144	IND	8
LFXP2-8E-5QN208I	1.2V	-5	Lead-Free PQFP	208	IND	8
LFXP2-8E-6QN208I	1.2V	-6	Lead-Free PQFP	208	IND	8
LFXP2-8E-5FTN256I	1.2V	-5	Lead-Free ftBGA	256	IND	8
LFXP2-8E-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-40E-5F484C	1.2V	-5	fpBGA	484	COM	40
LFXP2-40E-6F484C	1.2V	-6	fpBGA	484	COM	40
LFXP2-40E-7F484C	1.2V	-7	fpBGA	484	COM	40
LFXP2-40E-5F672C	1.2V	-5	fpBGA	672	COM	40
LFXP2-40E-6F672C	1.2V	-6	fpBGA	672	COM	40
LFXP2-40E-7F672C	1.2V	-7	fpBGA	672	COM	40

Industrial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-5E-5M132I	1.2V	-5	csBGA	132	IND	5
LFXP2-5E-6M132I	1.2V	-6	csBGA	132	IND	5
LFXP2-5E-6FT256I	1.2V	-6	ftBGA	256	IND	5

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-8E-5M132I	1.2V	-5	csBGA	132	IND	8
LFXP2-8E-6M132I	1.2V	-6	csBGA	132	IND	8
LFXP2-5E-5FT256I	1.2V	-5	ftBGA	256	IND	5
LFXP2-8E-5FT256I	1.2V	-5	ftBGA	256	IND	8
LFXP2-8E-6FT256I	1.2V	-6	ftBGA	256	IND	8

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-17E-5FT256I	1.2V	-5	ftBGA	256	IND	17
LFXP2-17E-6FT256I	1.2V	-6	ftBGA	256	IND	17
LFXP2-17E-5F484I	1.2V	-5	fpBGA	484	IND	17
LFXP2-17E-6F484I	1.2V	-6	fpBGA	484	IND	17

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (k)
LFXP2-30E-5FT256I	1.2V	-5	ftBGA	256	IND	30
LFXP2-30E-6FT256I	1.2V	-6	ftBGA	256	IND	30
LFXP2-30E-5F484I	1.2V	-5	fpBGA	484	IND	30
LFXP2-30E-6F484I	1.2V	-6	fpBGA	484	IND	30
LFXP2-30E-5F672I	1.2V	-5	fpBGA	672	IND	30
LFXP2-30E-6F672I	1.2V	-6	fpBGA	672	IND	30